



Integrated
Circuit
Systems, Inc.

Preliminary Information

M685

DUAL SAW, SELECTABLE FREQUENCY VCSO

GENERAL DESCRIPTION



The M685 is a dual SAW, selectable frequency VCSO frequency source for low-jitter clock generation. An integrated SAW (surface acoustic wave) delay line implements the high-Q VCO (voltage controlled oscillator) function, which results in low output phase noise and very low jitter. The M685-01 is available in a range of center frequencies from 125 to 175 MHz. The M685-02 provides 500 to 700 MHz. Guaranteed minimum pull-range of ± 120 ppm meets GbE requirements. (It also fully satisfies ± 50 ppm minimum pull-range specification commonly required.) Industry-standard K_{vco} (VCO Gain) provides full replacement compatibility. The M685 is well suited for phase-locked loop implementations, clock and data recovery circuits, and other timing applications in telecom and optical fiber networking systems (e.g., OC-48).

FEATURES

- ◆ Two integrated SAW devices and selectable output frequency; supports multi-rate optical interfaces
- ◆ M685-01 output frequencies from 125 to 175 MHz
M685-02 output frequencies from 500 to 700 MHz
(Specify center frequencies at time of order)
- ◆ Industry-standard K_{vco} for full compatibility
- ◆ Low phase jitter 0.2ps rms typical for the M685-02 (50kHz to 80MHz)
- ◆ Differential 3.3V LVPECL output
- ◆ Single 3.3V power supply
- ◆ Small 5 x 7.5mm SMT (surface mount) package

BLOCK DIAGRAM

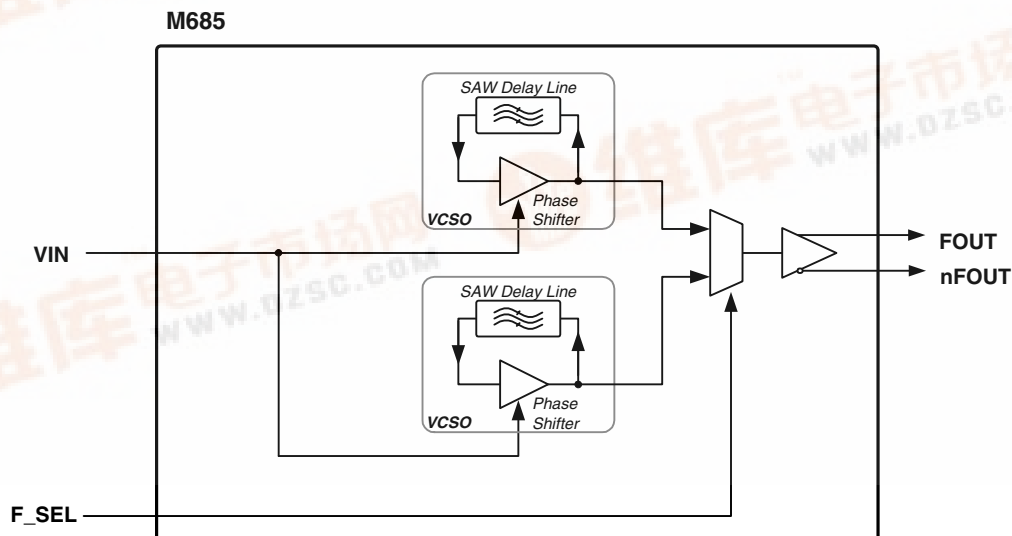


Figure 2: Block Diagram

PIN ASSIGNMENT (5 x 7.5mm SMT)

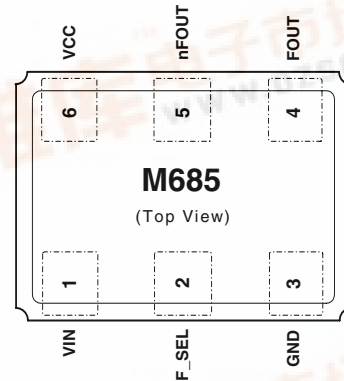


Figure 1: Pin Assignment

Sample of Available Output Frequencies

VCSO Center Frequencies ¹ (MHz)	Applications
155.5200, 167.3316	SONET/SDH, SONET/SDH FEC
156.2500, 161.1328	Gigabit Ethernet, GbE FEC
622.0800, 669.3266	SONET/SDH, SONET/SDH FEC
625.0000, 644.5313	Gigabit Ethernet, GbE FEC

Table 1: Sample of Available Output Frequencies

Note 1: Specify VCSO center frequencies at time of order



PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1	VIN	Input		Frequency control input.
2	F_SEL	Input	Internal pull-down resistor ¹	Frequency select: Logic 1 selects Frequency 2. Logic 0 selects Frequency 1.
3	GND	Ground		Power supply ground connection.
4	FOUT	Output	No internal terminator	Clock output pair. Differential LVPECL.
5	nFOUT	Output		
6	VCC	Power		Power supply connection, connect to +3.3V.

Table 2: Pin Descriptions

Note 1: See "Frequency Select" in Table 5 (DC Characteristics for M685-01 on pg. 3) and Table 7 (DC Characteristics for M685-02 on pg. 4).

ABSOLUTE MAXIMUM RATINGS¹

Symbol	Parameter	Rating	Unit
V _I	Inputs	-0.5 to V _{CC} +0.5	V
V _O	Outputs	-0.5 to V _{CC} +0.5	V
V _{CC}	Power Supply Voltage	4.6	V
T _S	Storage Temperature	-55 to +125	°C

Table 3: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Positive Supply Voltage	2.97	3.3	3.63	V
T _A	Ambient Operating Temperature	-40	25	+85	°C

Table 4: Recommended Conditions of Operation



ELECTRICAL SPECIFICATIONS FOR M685-01

DC Characteristics for M685-01

Unless stated otherwise, $V_{CC} = 3.3 \text{ Volts} \pm 10\%$, $T_A = 0 \text{ to } 85^\circ\text{C}$, VCSO Freq.'s = 155.52, 167.3316MHz, Outputs terminated into 180Ω to ground

	Symbol	Parameter	Pin	Min	Typ	Max	Unit
Power Supply	V_{CC}	Positive Supply Voltage	VCC	2.97	3.3	3.63	V
	I_{CC}	Power Supply Current			90	125	mA
Control Voltage	V_{IN}	Input Control Voltage Range	VIN	0		3.3	V
		V_{IN} Input Impedance			100		k Ω
Frequency Select ¹	V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
	V_{IL}	Input Low Voltage		-0.3		0.8	V
	I_{IH}	Input High Current	F_SEL			5	μA
	I_{IL}	Input Low Current		-150			μA
	$R_{pull\downarrow}$	Internal Pull-down Resistor			51		k Ω
Differential Outputs	V_{OH}	Output High Voltage		$V_{CC} - 0.98$		$V_{CC} - 0.75$	V
	V_{OL}	Output Low Voltage		$V_{CC} - 1.95$		$V_{CC} - 1.63$	V
	V_{P-P}	Peak to Peak Output Voltage ²	FOUT, nFOUT	0.450	0.625	0.85	V_{P-P}
	I_{OUT}	Output Current				20	mA

Note 1: Internally pulled down to Logic 0 (Frequency 1) if left unselected.

Note 2: Single-ended measurement. See Figure 3, Output Rise and Fall Time, on pg. 5.

Table 5: DC Characteristics for M685-01

AC Characteristics for M685-01

Unless stated otherwise, $V_{CC} = 3.3 \text{ Volts} \pm 10\%$, $T_A = 0 \text{ to } 85^\circ\text{C}$, VCSO Freq.'s = 155.52, 167.3316MHz, Outputs terminated into 180Ω to ground

	Symbol	Parameter		Min	Typ	Max	Unit	Notes
Control Voltage	V_{IN}	Modulation Bandwidth	VIN		600		kHz	
Output	F_{OUT}	Output Center Frequency Range	M685-01	125		175	MHz	
	APR	Absolute (Guaranteed) Pull-Range ¹		± 120			ppm	
	f_{STAB}	Frequency Stability			100		ppm p-p	At any given V_{IN}
	L_{IN}	Tuning Linearity			6		%	$V_{IN} = 0.3 \text{ to } 3.0\text{V}$ Best fit straight line
	K_{VCO}	VCO Gain	@ 155.52MHz		400		ppm/V	$V_{IN} = 0.3 \text{ to } 3.0\text{V}$
		Non-harmonic Spurious		-50	-77		dBc	
	Φ_n	SSB (single sideband)	100Hz Offset		-48		dBc/Hz	
		Phase Noise, offset	1kHz Offset		-75		dBc/Hz	
		from carrier	10kHz Offset		-99		dBc/Hz	
		@ 155.52MHz	100kHz Offset		-124		dBc/Hz	
			1MHz Offset		-142		dBc/Hz	
	J(t)	Jitter (rms)	12kHz to 20MHz		0.30		ps rms	
		@ 155.52MHz	50kHz to 80MHz		0.18		ps rms	
	odc	Output Duty Cycle ²		45		55	%	
	t_R	Output Rise Time ² for FOUT, nFOUT			275	425	ps	20% to 80%
	t_F	Output Fall Time ² for FOUT, nFOUT			275	425	ps	20% to 80%

Note 1: Also fully meets ± 50 ppm minimum pull-range specification that is commonly required.

Note 2: See Parameter Measurement Information on pg. 5.

Table 6: AC Characteristics for M685-01



ELECTRICAL SPECIFICATIONS FOR M685-02

DC Characteristics for M685-02

Unless stated otherwise, $V_{CC} = 3.3 \text{ Volts} \pm 10\%$, $T_A = 0 \text{ to } 85^\circ\text{C}$, VCSO Freq.'s = 622.08, 669.3266MHz, Outputs terminated into 180Ω to ground

	Symbol	Parameter	Pin	Min	Typ	Max	Unit
Power Supply	V_{CC}	Positive Supply Voltage	VCC	2.97	3.3	3.63	V
	I_{CC}	Power Supply Current			90	125	mA
Control Voltage	V_{IN}	Input Control Voltage Range	VIN	0		3.3	V
		V_{IN} Input Impedance			100		k Ω
Frequency Select ¹	V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
	V_{IL}	Input Low Voltage		-0.3		0.8	V
	I_{IH}	Input High Current	F_SEL			5	μA
	I_{IL}	Input Low Current		-150			μA
	$R_{pull\downarrow}$	Internal Pull-down Resistor			51		k Ω
Differential Outputs	V_{OH}	Output High Voltage		$V_{CC} - 0.98$		$V_{CC} - 0.75$	V
	V_{OL}	Output Low Voltage		$V_{CC} - 1.95$		$V_{CC} - 1.63$	V
	V_{P-P}	Peak to Peak Output Voltage ²	FOUT, nFOUT	0.450	0.625	0.85	V_{P-P}
	I_{OUT}	Output Current				20	mA

Note 1: Internally pulled down to Logic 0 (Frequency 1) if left unselected.

Note 2: Single-ended measurement. See Figure 3, Output Rise and Fall Time, on pg. 5.

Table 7: DC Characteristics for M685-02

AC Characteristics for M685-02

Unless stated otherwise, $V_{CC} = 3.3 \text{ Volts} \pm 10\%$, $T_A = 0 \text{ to } 85^\circ\text{C}$, VCSO Freq.'s = 622.08, 669.3266MHz, Outputs terminated into 180Ω to ground

	Symbol	Parameter		Min	Typ	Max	Unit	Notes
Control Voltage	V_{IN}	Modulation Bandwidth	VIN		600		kHz	
Output	F_{OUT}	Output Center Frequency Range	M685-02	500		700	MHz	
	APR	Absolute (Guaranteed) Pull-Range ¹		± 120			ppm	
	f_{STAB}	Frequency Stability			100		ppm p-p	At any given V_{IN}
	L_{IN}	Tuning Linearity			6		%	$V_{IN} = 0.3 \text{ to } 3.0\text{V}$ Best fit straight line
	K_{VCO}	VCO Gain	@622.08MHz		400		ppm/V	$V_{IN} = 0.3 \text{ to } 3.0\text{V}$
		Non-harmonic Spurious		-50	-77		dBc	
	Φ_n	SSB (single sideband)	100Hz Offset		-42		dBc/Hz	
		Phase Noise, offset from carrier @ 622.08MHz	1kHz Offset		-72		dBc/Hz	
			10kHz Offset		-102		dBc/Hz	
			100kHz Offset		-127		dBc/Hz	
			1MHz Offset		-146		dBc/Hz	
	J(t)	Jitter (rms)	12kHz to 20MHz		0.22		ps rms	
		@ 622.08MHz	50kHz to 80MHz		0.16		ps rms	
	odc	Output Duty Cycle ²		45		55	%	
	t_R	Output Rise Time ² for FOUT, nFOUT			275	400	ps	20% to 80%
	t_F	Output Fall Time ² for FOUT, nFOUT			275	400	ps	20% to 80%

Note 1: Also fully meets ± 50 ppm minimum pull-range specification that is commonly required.

Note 2: See Parameter Measurement Information on pg. 5.

Table 8: AC Characteristics for M685-02



PARAMETER MEASUREMENT INFORMATION

Output Rise and Fall Time

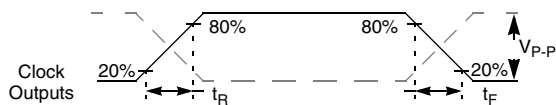


Figure 3: Output Rise and Fall Time

Output Duty Cycle

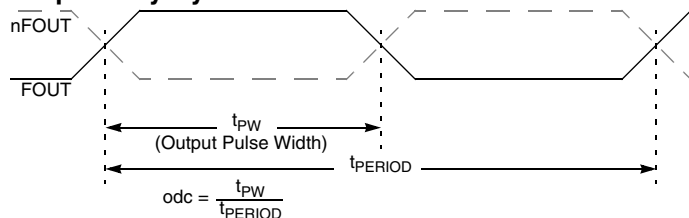


Figure 4: Output Duty Cycle

DEVICE PACKAGE - 5 x 7.5mm SMT (Surface Mount) Package

Mechanical Dimensions:

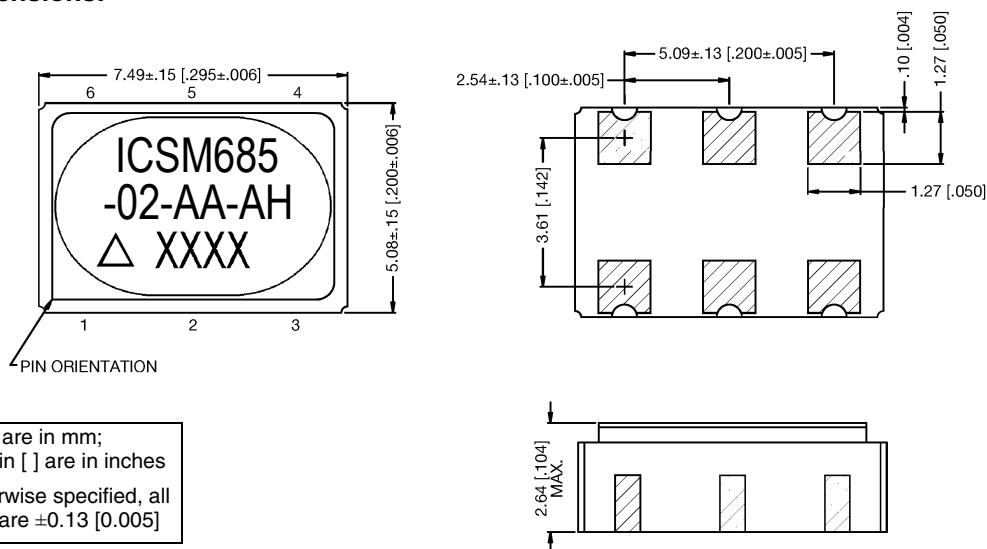


Figure 5: Device Package - 5 x 7.5mm SMT (Surface Mount) Package



ORDERING INFORMATION

Part Numbering Scheme

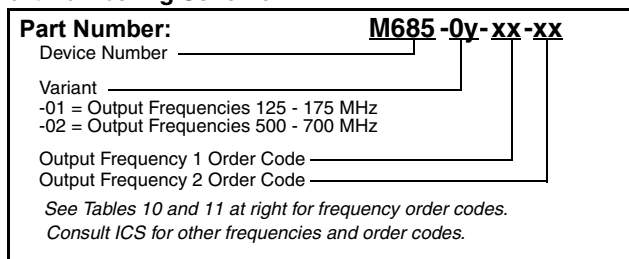


Figure 6: Part Numbering Scheme

Example Order Numbers

For Output Frequencies (MHz) Frequency 1, Frequency 2	Order Part Number M685-0y-xx-xx
155.5200, 167.3316	M685-01-BA-BH
156.2500, 161.1328	M685-01-BB-BD
622.0800, 669.3266	M685-02-AA-AH
625.0000, 644.5313	M685-02-AB-AD

Table 9: Example Order Numbers

M685-01 Standard Output Frequencies & Order Codes

153.6000 BO	167.2820 BF
155.5200 BA	167.3280 BG
156.2500 BB	167.3316 BH
156.8324 BC	167.7097 BI
161.1328 BD	168.0400 BJ
164.3555 BM	172.6423 BK
166.6286 BE	173.3708 BL

Table 10: M685-01 Standard Output Frequencies & Order Codes

M685-02 Standard Output Frequencies & Order Codes

614.4000 AO	669.1281 AF
622.0800 AA	669.3120 AG
625.0000 AB	669.3266 AH
627.3296 AC	670.8386 AI
644.5313 AD	672.1600 AJ
657.4219 AM	690.5692 AK
666.5143 AE	693.4830 AL

Table 11: M685-02 Standard Output Frequencies & Order Codes

Consult ICS for the availability of other frequencies

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PRODUCT APPLICATION CAUTION

F_SEL Change During Power-Up Can Affect Output Frequency Accuracy

M685E1

The M685 features an F_SEL input which is used to select the internal VCSO frequency.

The F_SEL input logic level should not be changed while the M685 device is in operation (that is, voltage is applied to the pin VCC), particularly when the pin VIN (the control voltage input) is above 2.0V.

Changing the F_SEL input logic level during operation may result in an erroneous output frequency.

It is safe to change F_SEL during operation if pin VIN can be held low, or at least below 2.0V.