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MITSUBISHI LSIs

M6MF16S2AVP

16777216-BIT (2097152-WORD BY 8-BIT) CMOS 3.3V-ONLY FLASH MEMORY &
2097152-BIT (262144-WORD BY 8-BIT) CMOS STATIC RAM
Stacked-MCP (Multi Chip Package)

PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

DESCRIPTION

The MITSUBISHI M6MF16S2AVP is a Stacked Muti Chip Package (S-MCP) that contents 16M-bit flash memory and 2M-bit Static RAM in a 48-pin TSOP (TYPE-I).

16M-bit Flash memory is a 2097152 bytes, 3.3V-only, and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR(DIvided bit-line NOR) architecture for the memory cell.
2M-bit SRAM is a 262144 bytes unsynchronous SRAM fabricated by silicon-gate CMOS technology.

M6MF16S2AVP is suitable for the application of the mobile-communication-system to reduce both the mount space and weight .

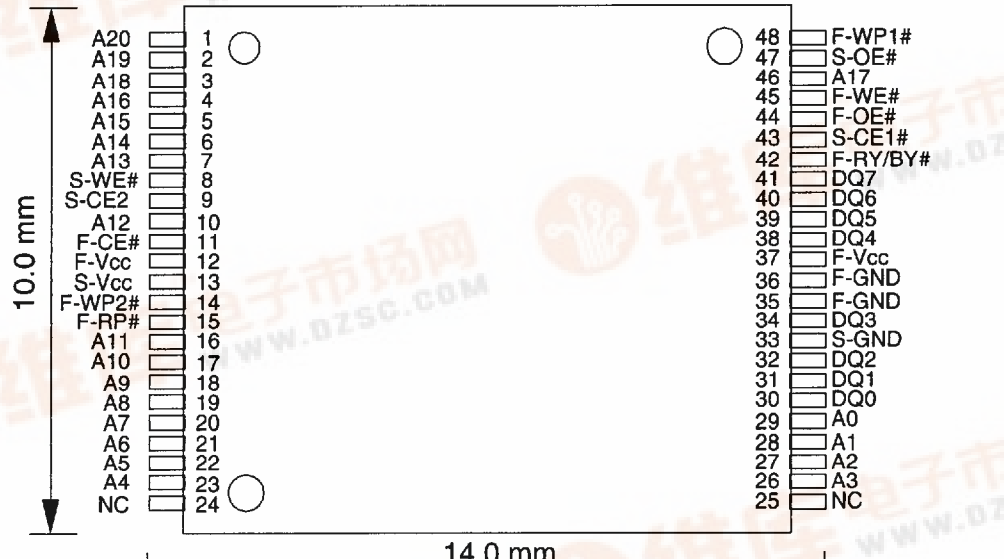
FEATURES

- Access time (Flash Memory, SRAM)
  ---------- 110ns (Max.)
- Supply voltage ---------- Vcc=2.7 ~ 3.6V
- Ambient temperature ---------- Ta=-20 ~ 85°C
- Package : 48-pin TSOP (Type-I) , 0.4mm lead pitch

APPLICATION

Mobile communication products

PIN CONFIGURATION (TOP VIEW)



NC:Non Connection

F-Vcc	:Vcc for Flash
F-GND	:GND for Flash
S-Vcc	:Vcc for SRAM
S-GND	:GND for SRAM
A0-A17	:Flash/SRAM common Address
A18-A20	:Address for Flash
DQ0-DQ7	:Data I/O
F-CE#	:Flash Chip Enable
F-OE#	:Flash Output Enable
F-WE#	:Flash Write Enable
F-WP1#,WP2#	:Flash Write Protect
F-RP#	:Flash Reset Power Down
F-RY/BY#	:Flash Ready /Busy
S-CE1#,CE2	:SRAM Chip Enable
S-OE#	:SRAM Output Enable
S-WE#	:SRAM Write Enable

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PRELIMINARY

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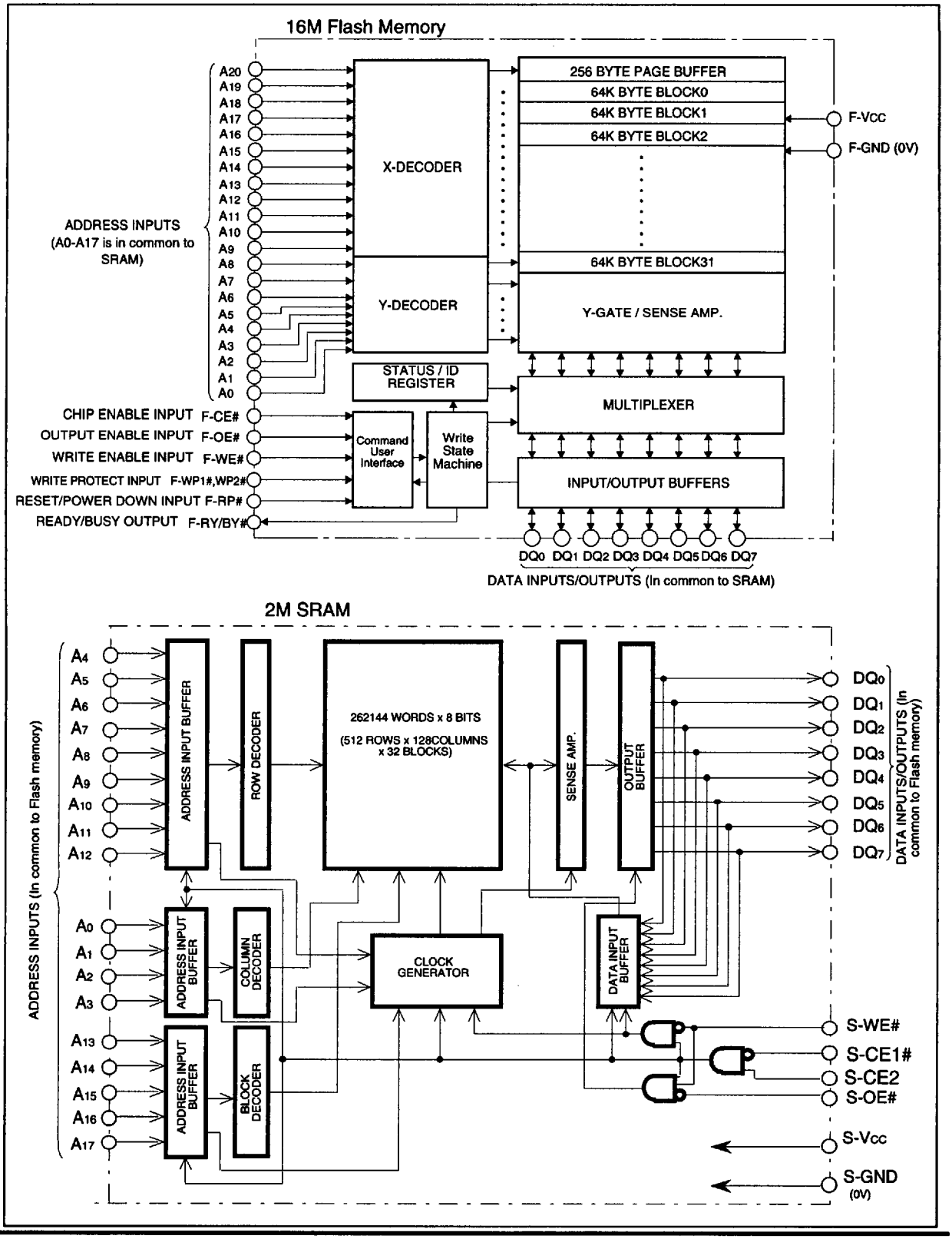
BLOCK DIAGRAM



1. Flash Memory

FUNCTION

The Flash Memory of M6MF16S2AVP includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase, page (256byte) program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.
A Deep Powerdown mode is enabled when the RP# pin is at GND, minimizing power consumption.

Read
The Flash Memory of M6MF16S2AVP has three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the Flash Memory automatically resets to read array mode. In the read array mode, low level input to CE# and OE#, high level input to WE# and RP#, and address signals to the address inputs (A0-A20) output the data of the addressed location to the data input/output(D0-D7).

Write
Writes to the CUI enable reading of memory array data, device identifiers and reading and clearing of the Status Register. they also enable block erase and program. The CUI is written by bringing WE# to low level, while CE# is at low level and OE# is at high level. Addresses and data are latched on the earlier rising edge of WE# and CE#. Standard micro-processor write timings are used.

Output Disable
When OE# is at VIH, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

Standby
When CE# is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

Deep Power-Down
When RP# is at VIL, the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance(High-Z) state. After return from powerdown, the CUI is reset to Read Array , and the Status Register is cleared to value 80H.
During block erase or program modes, RP# low will abort either operation. Memory array data of the block being altered become invalid.

SOFTWARE COMMAND DEFINITIONS

The device operations are selected by writing specific software command into the CUI.

Read Array Command (FFH)
The device is in Read Array mode on initial device powerup and after exit from deep powerdown, or by writing FFH to the CUI. The device remains in Read Array mode until the other commands are written.

Read Device Identifier Command (90H)
The Device Identifier is read after writing the Read Device Identifier command of 90H to the Command User Interface. Following the command write, the manufacturer code and the device code can be read from address 000000H and 000001H, respectively.

Read Status Register Command (70H)
The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface.
The contents of Status Register are latched on the later falling edge of OE# or CE#. So CE# or OE# must be toggled every status read.

Clear Status Register Command (50H)
The Erase Status and Program Status bits are set to "1"s by the Write State Machine and can be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

Block Erase / Confirm Command (20H/D0H)
Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Suspend/Resume Command (B0H/D0H)
Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

Program Command
Program consists of data load sequence to page buffer and data program sequence to flash memory array.

A) Start Load Page Buffer (DBH/XXH/XXH)
Writing Start Load Page Buffer command allows data load to page buffer. DBH is written to the CUI, follwed by two write cyclle of a certain command except for Block Erase Command(20H/D0H) and Lock Bit Program Command(77H/D0H).

B) Sequential Load to Page Buffer (DBH/FFH/00H)
Writing Sequential Load to Page Buffer command allows 256 bytes data load to page buffer sequentially. Follwing a three - command sequence(DBH/FFH/00H) , 256 writes cycle specifying the address and data executes loading to page buffer. In this mode, only A0-7 is used and A8-A20 is a don't care.

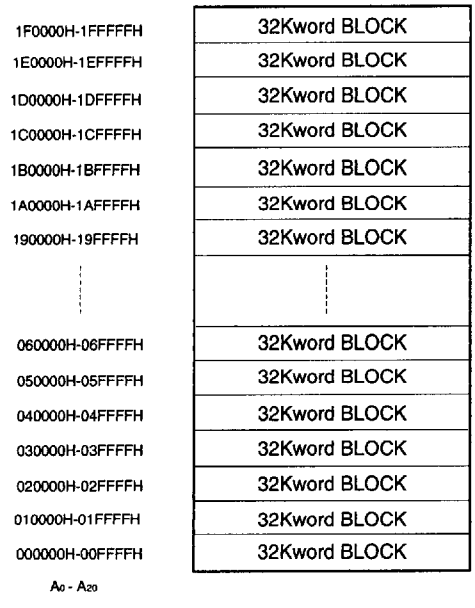
C) End Load Page Buffer (5FH/XXH/XXH)
Writing End Load Page Buffer command ends data load to page buffer. 5FH is written to the CUI, follwed by two write cyclle of a certain command except for Block Erase Command(20H/D0H) and Lock Bit Program command(77H/D0H). The data of page command is stored while Vcc power is on or until writing Page Buffer Write to Flash command or Page Buffer Clear command.The stored data in page buffer can be changed by data load sequence follwed by re-start load page buffer.

D) Page Buffer Write to Flash (0EH/D0H)
Programming to flash memory array from page buffer is executed by Page Buffer Write to Flash command. The Page Buffer Write to Flash setup command (0EH) is witten to the CUI, followed by the confirm commasnd (D0H). In this mode, A8-A20 is used. The WSM controls the program pulse application and verify operation. After programming, each page buffer is cleared to "FFH". And the page buffer data is invaid in the suspend mode.
Basically re-program must not be done on a page which has already programmed.

DATA PROTECTION
The Flash Memory of M6MF16S2AVP provides hardware-locking of memory blocks. Each block has an associated nonvolatile lock-bit which determines the lock status of the block.In addition, this flash memory has a master Write Protect pin (WP) which prevents any modifications to memory blocks.
When WP2# is at low, all memory blocks are locked. And when both WP1# and WP2# are at low, this part is in read array only mode.(not be accepted any write command)
When WP1# is at low and WP2# is at high, the memory blocks whose lock-bits are set to "0" are locked.
When both WP1# and WP2# are at high, lock-bits can be programmed (to "0"), all blocks can be programmed or erased regardless of the state of the lock-bits, and lock-bits are cleared to "1" by this erase. See the BLOCK LOCKING table on P.6 for details.

Power Supply Voltage
When the power supply voltage (Vcc) is less than 2.2V, the device is set to the Read-only mode.
A delay time of 2 us is required before any device operation is initiated. The delay time is measured from the time Vcc reaches Vccmin.
During power up, F-RP#=GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

MEMORY MAP



Flash Memory Memory Map

BUS OPERATIONS

Mode \ Pins		F-CE#	F-OE#	F-WE#	F-RP#	DQ0-7	F-RY/BY#
Read	Array	VIL	VIL	VIH	VIH	Data out	VOH(Hi - Z)
	Status Register	VIL	VIL	VIH	VIH	Status Register Data	X 1)
	Lock Bit Status	VIL	VIL	VIH	VIH	Lock Bit Data (DQ6)	X
	Identifier Code	VIL	VIL	VIH	VIH	Identifier Code	VOH(Hi - Z)
Output Disable		VIL	VIH	VIH	VIH	Hi-Z	X
Stand by		VIH	X 2)	X	VIH	Hi-Z	X
Write	Program	VIL	VIH	VIL	VIH	Command/Data in	X
	Erase	VIL	VIH	VIL	VIH	Command	X
	Others	VIL	VIH	VIL	VIH	Command	X
Deep Power Down		X	X	X	VIL	Hi-Z	VOH(Hi - Z)

1) X at RY/BY# is VOL or VOH(Hi-Z).
*The RY/BY# is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation.
A pull-up resistor of 10K-100K Ohms is required to allow the RY/BY# signal to transition high indicating a Ready WSM condition.
2) X can be VIH or VIL for control pins.

PRELIMINARY

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M6MF16S2AVP

16777216-BIT (2 M x 8-BIT)
CMOS 3.3V-ONLY FLASH MEMORY

SOFTWARE COMMAND DEFINITION

Command	1st bus cycle			2nd bus cycle			3rd bus cycle		
	Mode	Address	Data	Mode	Address	Data	Mode	Address	Data
Read Array	Write	X	FFH						
Device Identifier	Write	X	90H	Read	IA 1)	ID 1)			
Read Status Register	Write	X	70H	Read	X	SRD 2)			
Clear Status Register	Write	X	50H						
Block Erase / Confirm	Write	X	20H	Write	BA 3)	D0H			
Suspend	Write	X	B0H						
Resume	Write	X	D0H						
Start Load Page Buffer 4)	Write	X	DBH	Write	X	X	Write	X	X
Sequential Load Page Buffer	Write	X	E0H	Write	X	FFH	Write	X	00H 5)
End Load Page Buffer	Write	X	5FH	Write	X	X	Write	X	X
Page Buffer Write to Flash	Write	X	0EH	Write	WA 6)	D0H			
Read Lock Bit Status	Write	X	71H	Read	BA	D6 7)			
Lock Bit Program / Confirm	Write	X	77H	Write	BA	D0H			
Erase All Unlocked Blocks / Confirm	Write	X	A7H	Write	X	D0H			
Sleep 8)	Write	X	F0H						

1) IA=ID Code Address : A0=VIL (Manufacture's Code) : A0=VIH (Device Code), ID=ID Code, A1-A20=VIL
2) SRD=Status Register Data
3) BA=Block Address (A16-A20)
4) Two dummy write cycle is necessary,except for Block Erase/Confirm command(20H/D0H) and Lock Bit Program/Confirm command(77H/D0H), after Start Page Buffer Load command and End Load Page Buffer command.
6) WA=Write Address : Page Buffer Data is programmed to the same page address in the memory arrary, and address A0-7 is ignored.
7) DQ6 provides Block Lock Bit Status, DQ6=1 : Block Unlock , DQ6=0 : Block Locked.
8) Sleep command (F0H) put the device into the sleep mode after completing the current operation. The active current is reduced to deep power -down levels. The Read Array command (FFH) must be written to get the device out of sleep mode.

BLOCK LOCKING

RP#	WP1#	WP2#	Erase/Program Operation		Write Protection Provided
			Memory Block	Lock Bit	
VHH	X	X	Unlock	Unlock	All Blocks/Lock Bits Unlocked (Erase/Program enable)
VIH	VIH	VIH	Unlock	Unlock	All Blocks/Lock Bits Unlocked (Erase/Program enable)
		VIL	Lock	Lock	All Blocks/Lock Bits Locked
	VIL	VIH	Depend on Lock Bit Data 1)	Lock	Locked by Lock Bit
		VIL	Lock	Lock	Alll Blocks/Lock Bits Locked (Read Array Only Mode) 4)
VIL	X	X	Lock	Lock	All Blocks/Lock Bits Locked (Deep Power Down Mode)

1) When the Lock bit is "0" ,its block cannot be programed and erased.
Lock bit is set to "0" by LOCK BIT PROGRAM.
Locked bit("0") is cleared to "1" with block memory by BLOCK ERASE on setting unlock mode.
2) DQ6 provides Lock Bit Status of each block after writing the Read Lock Status command (71H).
3) WP# pin must not be switched during performing Read / Write operations or WSM Busy (WSMS = 0).
4) The device prpvides a complete read array only mode.
(not be accepted any write command, including read mode command, ex:device identifier, read status register.)
5) X can be VIH or VIL for control pins.

STATUS REGISTER DATA (SRD)

Symbol	Status	Definition	
		"1"	"0"
SR.7 (D7)	Write State Machine Status	Ready	Busy
SR.6 (D6)	Suspend Status	Suspended	Operation in Progress / Completed
SR.5 (D5)	Erase Status	Error	Successful
SR.4 (D4)	Program Status	Error	Successful
SR.3 (D3)	Block Status after Program	Error	Successful
SR.2 (D2)	Reserved	-	-
SR.1 (D1)	Reserved	-	-
SR.0 (D0)	Device Sleep Status	Device in Sleep	Device Not in Sleep

*DQ3 indicates the block status after the page programming. When DQ3 is "1", the page has the over-programed cell . If over-program occurs, the device is block fail. However if DQ3 is "1", please try the block erase to the block. The block may revive.

PRELIMINARY

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M6MF16S2AVP

16777216-BIT (2 M x 8-BIT)
CMOS 3.3V-ONLY FLASH MEMORY

DEVICE IDENTIFIER CODE

Code \ Pins	A0	D7	D6	D5	D4	D3	D2	D1	D0	Hex. Data
Manufacturer Code	VIL	0	0	0	1	1	1	0	0	1CH
Device Code	VIH	0	1	1	0	1	0	0	1	69H

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Unit
F-Vcc	Vcc voltage (Flash Memory)	with respect to Ground	-0.2	4.6	V
VI1	All input or output voltage except for Vcc,RP# [1]		-0.2	4.6	V
VI2	RP# supply voltage		-0.6	14.0	V
Ta	Ambient temperature		-20	85	°C
Tbs	Temperature under bias		-30	85	°C
Tstg	Storage temperature		-65	125	°C
I OUT	Output short circuit current			100	mA

1) Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+1.5V for periods <20ns.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
CIN	Input capacitance (address, Control Pins)	Ta = 25°C, f=1MHz, VIN=VOUT=0V			8	pF
COUT	Output capacitance				12	pF

Note: The value of common pins to SRAM is the sum of Flash Memory and SRAM.

DC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
ILI	Input leakage current	0V ≤ VIN ≤ F-Vcc			±1.0	µA
ILO	Output leakage current	0V ≤ VOUT ≤ F-Vcc			±10	µA
ISB1	Vcc standby current	F-Vcc = 3.6V, VIN=VIL/VIH, F-CE#=F-RP#=F-WP1#,WP2#=VIH		50	200	µA
ISB2		F-Vcc=3.6V,VIN=F-GND or F-Vcc, F-CE#=F-RP#=F-WP1#,WP2#=Vcc±0.3V		0.1	5	µA
ISB3	Vcc deep powerdown current	F-Vcc = 3.6V, VIN=VIL/VIH, F-RP#= VIL		5	15	µA
ISB4		F-Vcc = 3.6V, VIN=F-GND or F-Vcc, F-RP#=F-GND±0.3V		0.1	5	µA
ICC1	Vcc read currenr	F-Vcc = 3.6V, VIN=VIL/VIH, F-CE# = VIL, F-RP#=F-OE#=VIH, f = 5MHz, IOUT = 0mA		7	25	mA
ICC2	Vcc write current	F-Vcc=3.6V,VIN=VIL/VIH,F-CE#=F-WE#=VIL,F-RP#=F-OE#=VIH			30	mA
ICC3	Vcc program currenrt	F-Vcc = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP1#,WP2# = VIH			30	mA
ICC4	Vcc erase current	F-Vcc = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP1#,WP2# = VIH			40	mA
ICC5	Vcc suspend current	F-Vcc = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP1#,WP2# = VIH			200	µA
I RP	RP# block unlock current	F-RP# = VHH max			500	µA
VIHH	RP# block unlock voltage		11.4	12.0	12.6	V
VIL	Input low voltage		– 0.5		0.8	V
VIH	Input high voltage		2.0		Vcc+0.5	V
VOL	Output low voltage	IOL = 4.0mA			0.45	V
VOH1	Output high voltage	IOH = –2.5mA	0.85Vcc			V
VOH2		IOH = –100µA	Vcc–0.4			V
VLKO	Low Vcc Lock-Out voltage 2)		1.5		2.5	V

All currents are in RMS unless otherwise noted.
1) Typical values at Vcc=3.3V, Ta=25°C
2) To protect against initiation of write cycle during Vcc power-up/ down, a write cycle is locked out for Vcc less than VLKO.
If Vcc is less than VLKO, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Vcc is less than VLKO, the alteration of memory contents may occur.

AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless othe

Read-Only Mode

Symbol		Parameter	Limits			Unit
			Min	Typ	Max	
tRC	tAVAV	Read cycle time	110			ns
ta (AD)	tAVQV	Address access time			110	ns
ta (CE)	tELQV	Chip enable access time			110	ns
ta (OE)	tGLQV	Output enable access time			55	ns
tCLZ	tELQX	Chip enable to output in low-Z	0			ns
tDF(CE)	tEHQZ	Chip enable high to output in high Z			30	ns
tOLZ	tGLQX	Output enable to output in low-Z	0			ns
tDF(OE)	tGHQZ	Output enable high to output in high Z			30	ns
tPHZ	tPLQZ	RP# low to output high-Z			300	ns
tOH	tOH	Output hold from CE#, OE#, addresses	0			ns
tOEH	tWHGL	OE# hold from WE# high	110			ns
tPS	tPHEL	RP# high recovery to CE# low	500			ns

Timing measurements are made under AC waveforms for read operations.

Read/Write Mode (WE# control)

Symbol		Parameter	Limits			Unit
			Min	Typ	Max	
tWC	tAVAV	Write cycle time	110			ns
tAS	tAVWL	Address set-up time	50			ns
tAH	tWLAX	Address hold time	10			ns
tDS	tDVWH	Data set-up time	50			ns
tDH	tWHDX	Data hold time	10			ns
tCS	tELWL	Chip enable set-up time	0			ns
tCH	tWHEH	Chip enable hold time	0			ns
tWP	tWLWH	Write pulse width	60			ns
tWPH	tWHWL	Write pulse width high	20			ns
tBLS / tWPS	tPHHWH	Block Lock set-up to write enable high	110			ns
tBLH / tWPH	tPHHWH	Block Lock hold from valid SRD	0			ns
tDAP	tWHRH1	Duration of auto-program operation		5	80	ms
tDAE	tWHRH2	Duraruin of auto-erase operation		50	600	ms
tWHRL	tWHRL	Write enable high to RY/BY# low			110	ns
tPS	tPHWL	F-RP# high recovery to F-WE# low	500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at Vcc=3.3V, Ta=25°C

Read/Write Mode (CE# control)

Symbol		Parameter	Limits			Unit
			Min	Typ	Max	
tWC	tAVAV	Write cycle time	110			ns
tAS	tAVWL	Address set-up time	50			ns
tAH	tWLAX	Address hold time	10			ns
tDS	tDVWH	Data set-up time	50			ns
tDH	tWHDX	Data hole time	10			ns
tWS	tELWL	Write enable set-up time	0			ns
tWH	tWHEH	Write enable hold time	0			ns
tCEP	tWLWH	CE# pulse width	60			ns
tCEPH	tWHWL	CE# pulse width high	20			ns
tBLS tWPS	tPHHWH	Block Lock set-up to write enable high	110			ns
tBLH tWPH	tPHHWH	Block lock hold from valid SRD	0			ns
tDAP	tWHRH1	Duration of auto-program operation		5	80	ms
tDAE	tWHRH2	Duration of auto-erase operation		50	600	ms
tEHRL	tEHRL	Chip enable high to RY/BY# low			110	ns
tPS	tPHWL	RP# high recovery to write enable low	500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at Vcc=3.3V, Ta=25°C

Erase and Program Performance

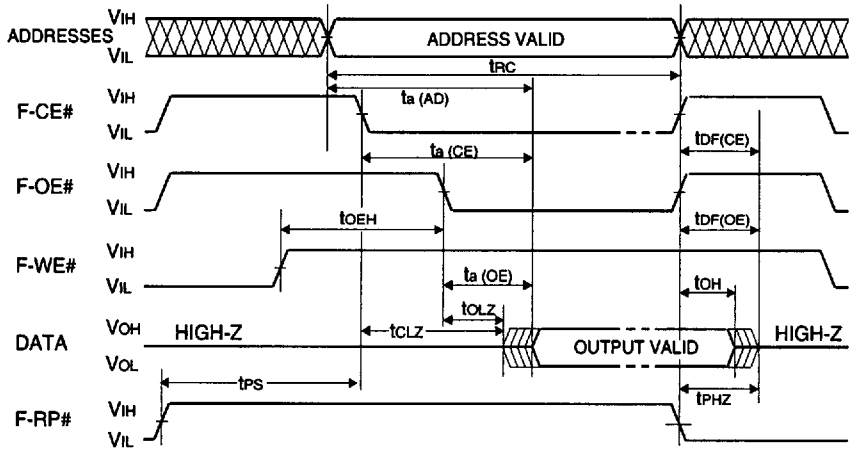
Parameter	Limits			Unit
	Min	Typ	Max	
Block Erase Time		40	600	ms
Block Program Time (Page Mode)		1.3	5	sec
Page Program Time		4	80	ms

Vcc Power UP/Down Timing

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
tVCS	RP# =VIH set-up time from Vcc at 2.7V	2			μs

During power up/down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming.
The device must be protected against initiation of write cycle for memory contents during power up/down.
The delay time of min.2usec is always required before read operation or write operation is initiated from the time Vcc reaches 2.7V during power up. By holding RP# VIL, the contents of memory is protected during Vcc power up/down.
During power up, RP# must be held VIL for min.2us from the time Vcc reaches 2.7V.
During power down, RP# must be held VIL until Vcc reaches GND.
RP# doesn't have latch mode ,so RP# must be held VIH during read operation or erase/program operation.

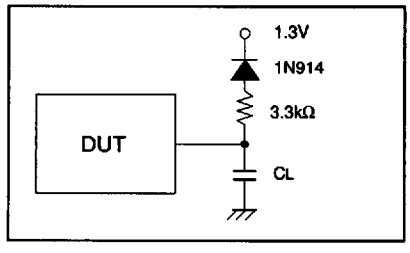
AC WAVEFORMS FOR READ OPERATION AND TEST CONDITIONS



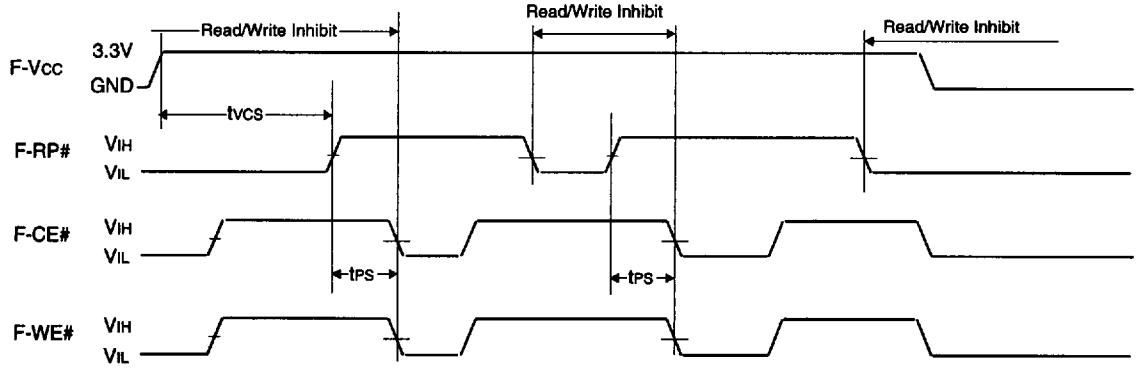
TEST CONDITIONS FOR AC CHARACTERISTICS

Test Configuration		Vcc=2.7V ~ 3.6V
Input voltage	VIL	0V
	VIH	3.0V
Input rise and fall times (10%-90%)		10ns
Reference voltage at timing measurement		1.5V
Capacitance load value	CL	100pF

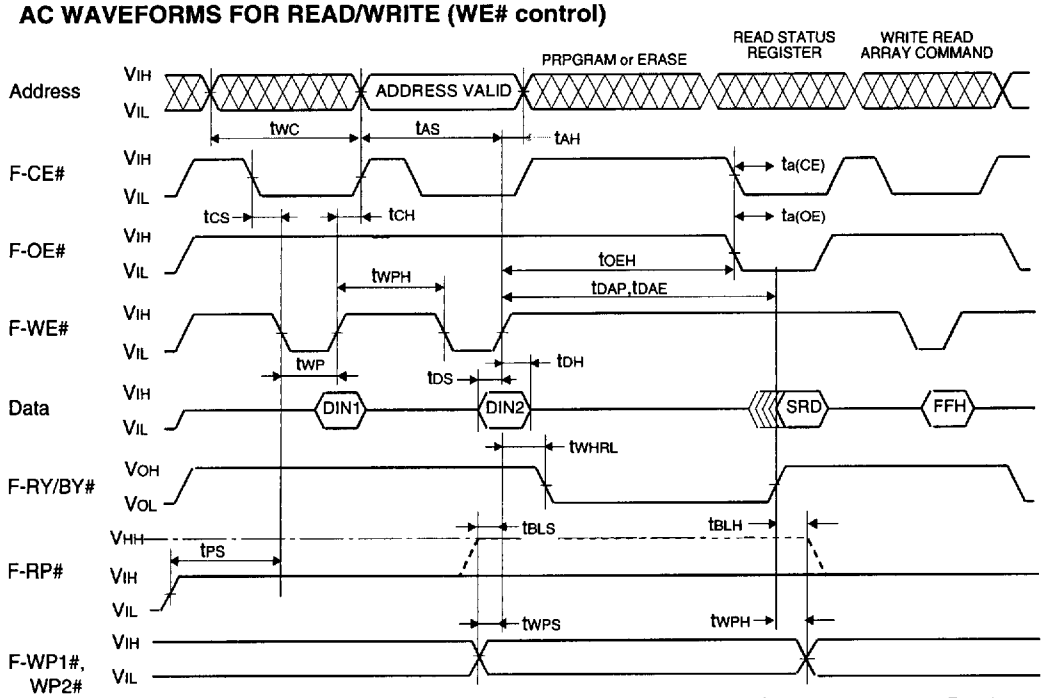
Output load : 1TTL gate + CL
or



Vcc POWER UP / DOWN TIMING

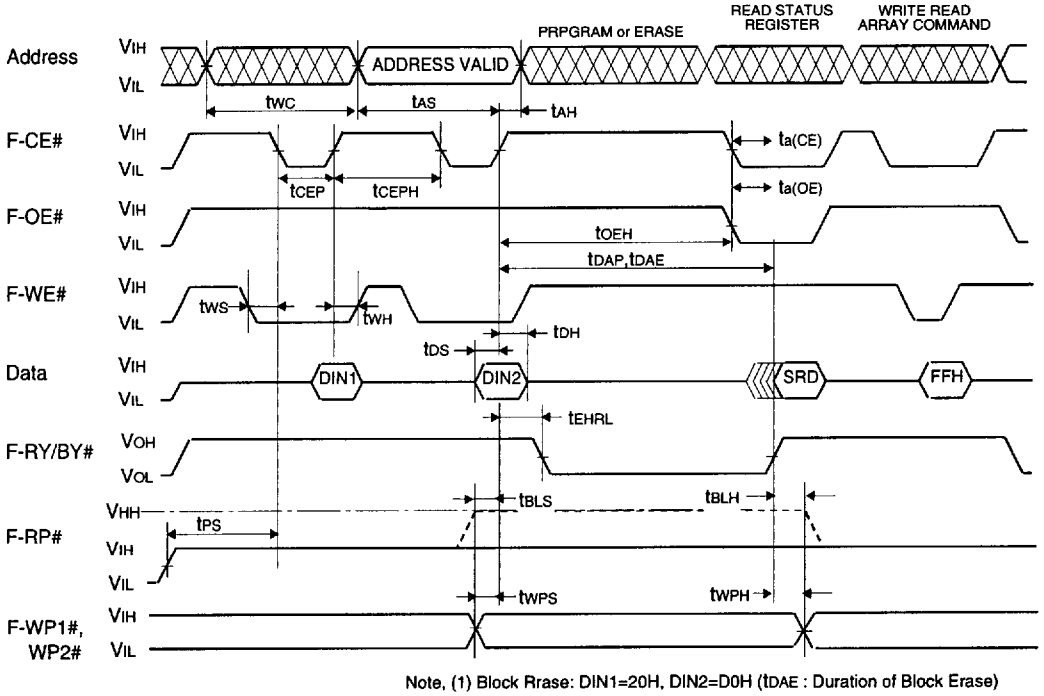


AC WAVEFORMS FOR READ/WRITE (WE# control)



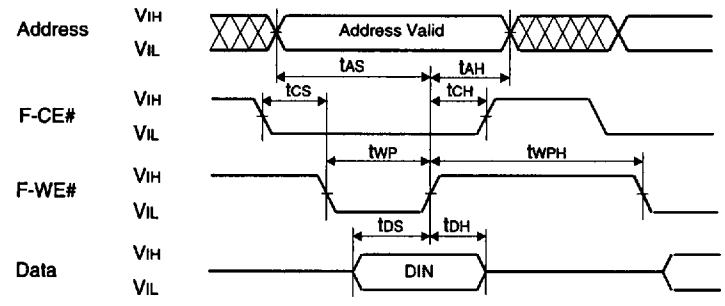
Note, (1) Block Rrase: DIN1=20H, DIN2=D0H (tDAE : Duration of Block Erase)
(2) Page Buffer Write to Flash : DIN1=0EH, DIN2=D0H (tDAP : Duration of program)
(3) Lock Bit Program / Confirm: DIN1=77H, DIN2=D0H (tDAP : Duration of program)
(4) Erase All Unlocked Blocks / Confirm : DIN1=A7H, DIN2=D0H (tFERS : Duration of Chip Erase)

AC WAVEFORMS FOR READ/WRITE (CE# control)

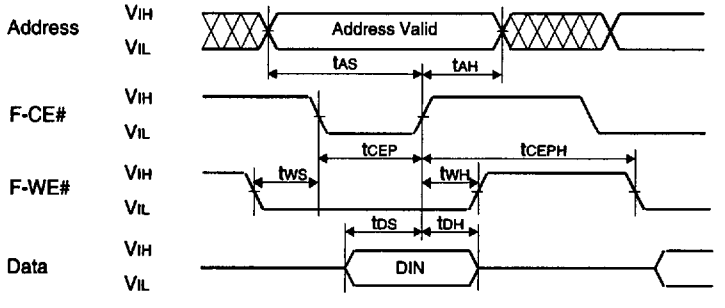


Note, (1) Block Rrase: DIN1=20H, DIN2=D0H (tDAE : Duration of Block Erase)
(2) Page Buffer Write to Flash : DIN1=0EH, DIN2=D0H (tDAP : Duration of program)
(3) Lock Bit Program / Confirm: DIN1=77H, DIN2=D0H (tDAP : Duration of program)
(4) Erase All Unlocked Blocks / Confirm : DIN1=A7H, DIN2=D0H (tFERS : Duration of Chip Erase)

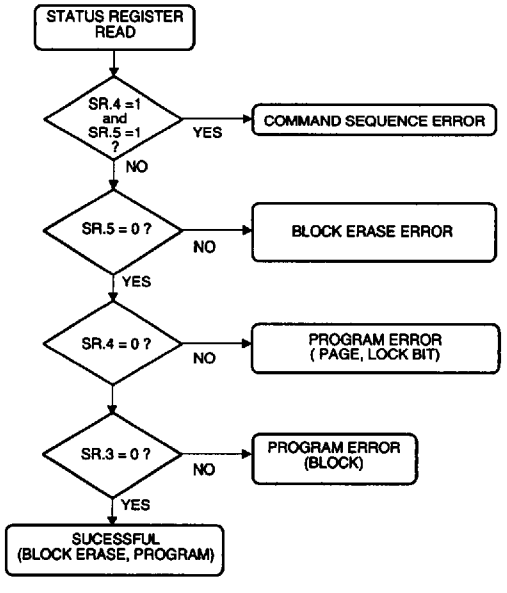
AC WAVEFORMS FOR PAGE BUFFER WRITE OPERATION (WE# control)



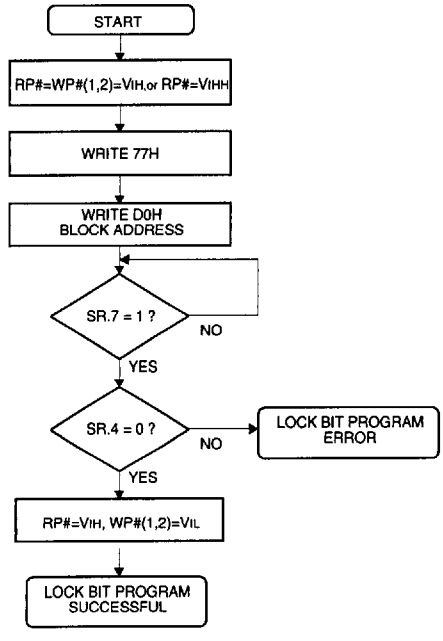
AC WAVEFORMS FOR PAGE BUFFER WRITE (CE# control)



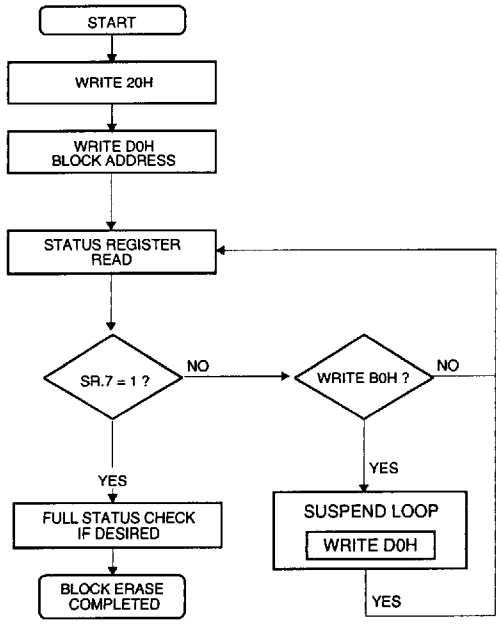
FULL STATUS CHECK PROCEDURE



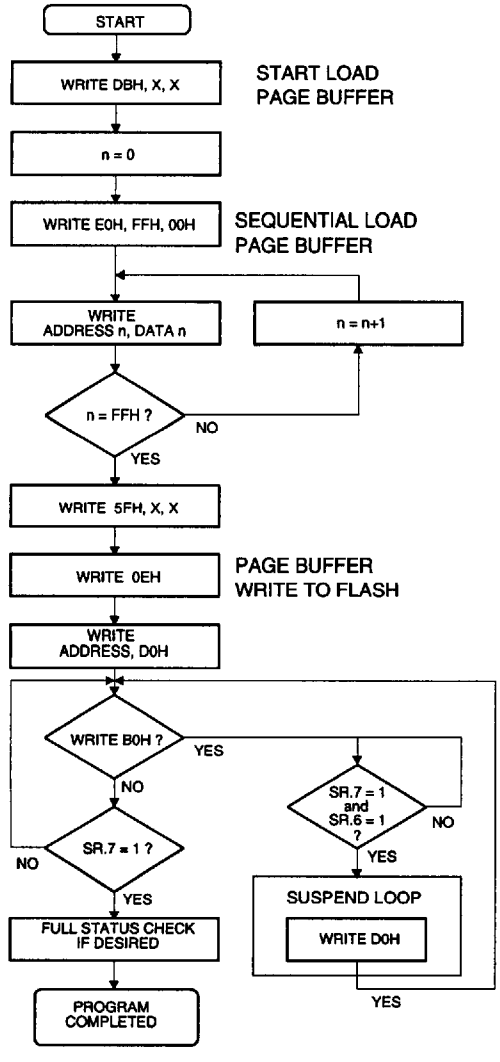
LOCK BIT PROGRAM FLOW CHART



BLOCK ERASE FLOW CHART

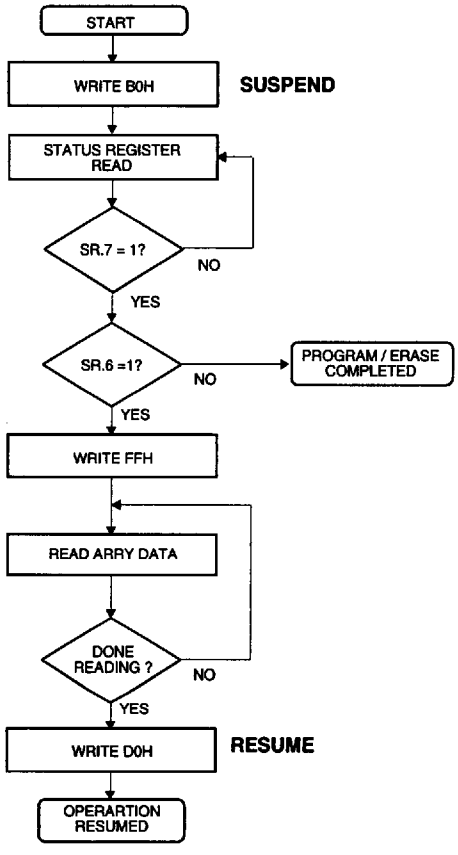


PROGRAM FLOW CHART
(PAGE BUFFER WRITE TO FLASH FLOW)



Note; Block Erase /Confirm command(20H/DOH) and Lock Bit Program /Confirm command is not allowed as two-dummy cycles after Start Page Buffer load command and End Page Buffer Load command is written.

SUSPEND / RESUME FLOW CHART



PRELIMINARY
Notice : This is not a final specification.
Some parametric limits are subject to change.

2. SRAM

FUNCTION

The SRAM of the M6MFT/B16S2TP is the same chip with M5M5V208 and its operation mode is determined by a combination of the device control inputs S-CE1#, S-CE2, S-WE# and S-OE#.

Each mode is summarized in the function table.

A write cycle is executed whenever the low level S-WE# overlaps with the low level S-CE1# and the high level S-CE2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of S-WE#,S-CE1# or S-CE2,whichever occurs first,requiring the set-up and hold time relative to these edge to be maintained. The output enable input S-OE# directly controls the output stage. Setting the S-OE# at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting S-WE# at a high level and S-OE# at a low level while S-CE1# and S-CE2 are in an active state(S-CE1#=L,S-CE2=H).

When setting S-CE1# at a high level or S-CE2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by S-CE1# and S-CE2. The power supply current is reduced as low as the stand-by current which is specified as ICC3 or ICC4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

S-CE1#	S-CE2	S-WE#	S-OE#	Mode	DQ	Icc
X	L	X	X	Non selection	High impedance	Standby
H	X	X	X	Non selection	High impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		High impedance	Active

PRELIMINARY
Notice : This is not a final specification.
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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
S-Vcc	Supply voltage (SRAM)	With respect to GND	− 0.3*~4.6	V
V_I	Inout voltage		− 0.3* ~ Vcc + 0.5 (Max 4.6)	V
V_O	Output voltage		0 ~ Vcc	V
P_d	Power dissipation	Ta=25°C	700	mW
T_{opr}	Operating temperature		-20 ~ 85	°C
T_{stg}	Storage temperature		− 65 ~150	°C

* -3.0V in case of AC (Pulse Width ≤ 30ns)

DC ELECTRICAL CHARACTERISRICS (Ta=-20~85°C, Vcc=2.7V~3.6V, Unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc +0.3V	V
V_{IL}	Low-level input voltage			−0.3		0.6	V
V_{OH1}	High-level output voltage1	I_{OH}= −0.5mA		2.4			V
V_{OH2}	High-level output voltage2	I_{OH}= −0.05mA		Vcc -0.5V			V
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	V
I_I	Input current	V_I=0 ~ Vcc				±1	µA
I_O	Output current in off-state	S-CE1#=VIH or S-CE2=V_{IL} or S-OE#=V_{IH} $V_{I/O}$=0 ~ Vcc				±1	µA
Icc1	Active supply current (MOS level input)	S-CE1#≤ 0.2V, S-CE2 ≥ S-Vcc-0.2V other inputs ≤ 0.2V or ≥ S-Vcc-0.2V Output-open(duty 100%)	10MHz	-	20	25	mA
			5MHz	-	10	13	
			1MHz	-	3	5	
Icc2	Active supply current (TTL level input)	S-CE1#=V_{IL}, S-CE2=V_{IH} other inputs = V_{IH} or V_{IL} Output-open(duty 100%)	10MHz	-	22	27	mA
			5MHz	-	12	15	
			1MHz	-	3	5	
Icc3	Stand-by current	1) S-CE2 ≤ 0.2V , other inputs = 0 ~ Vcc 2) S-CE1# ≥ Vcc-0.2V, S-CE2 ≥ Vcc-0.2V other inputs = 0 ~ Vcc	-20~+85°C	-	-	40	µA
			-20~+40°C	-	-	5	
			+25°C	-	0.3	2	
Icc4	Stand-by current	S-CE1# = V_{IH} or S-CE2 = V_{IL}, other inputs = 0 ~ Vcc		-	-	0.33	mA

* -3.0V in case of AC (Pulse Width ≤ 30ns)

CAPACITANCE (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			7	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			9	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc = 3V, Ta = 25°C
3: The value of common pins to Flash Memory is the sum of Flash Memory and SRAM.

PRELIMINARY
Notice : This is not a final specification.
Some parametric limits are subject to change.

AC ELECTRICAL CHARACTERISTICS (Ta=-20 ~ 85°C, Vcc=2.7V ~ 3.6V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Vcc ..... 2.7V ~ 3.6V
Input pulse level VIH=2.2V, VIL=0.4V
Input rise and fall time 5ns
Reference level ..... VOH=VOL=1.5V
Output loads ..... Fig.1,CL = 30pF
CL = 5pF (for ten,tdis)

Transition is measured ±500mV from steady state voltage. (for ten,tdis)

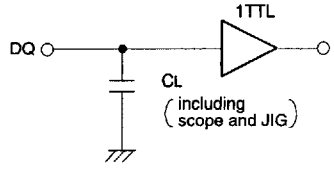


Fig.1 Output load

(2) READ CYCLE

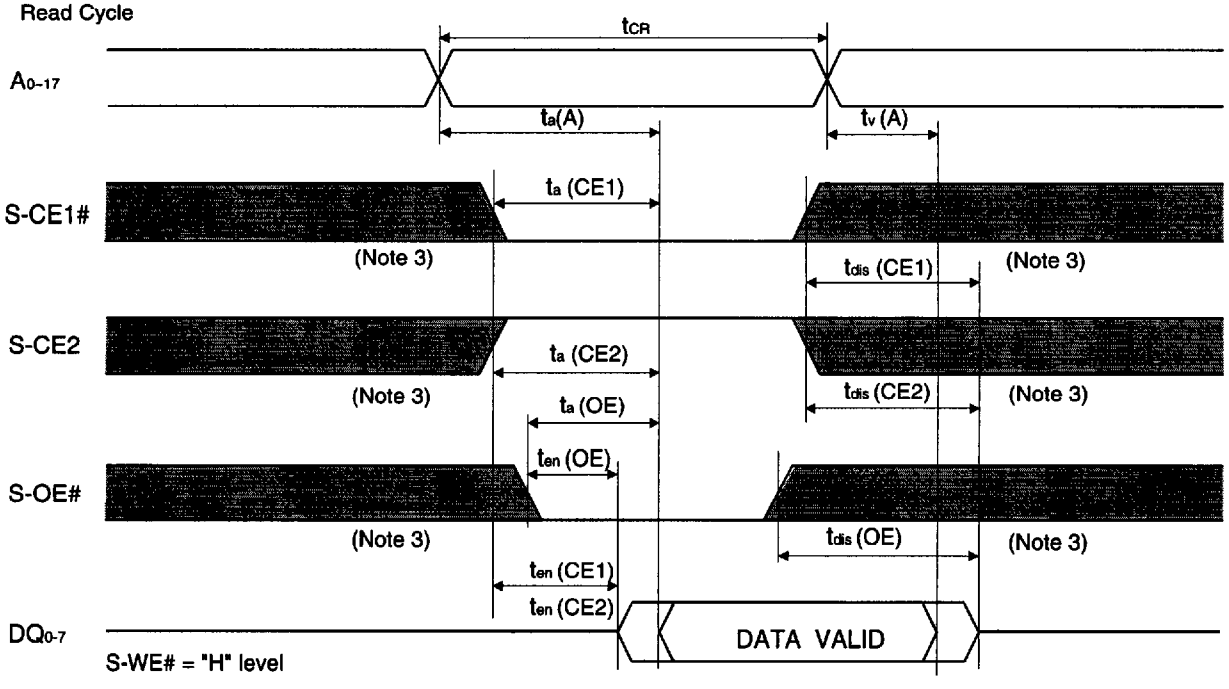
Symbol	Parameter	Limits		Unit
		Min	Max	
tCR	Read cycle time	110		ns
ta(A)	Address access time		110	ns
ta(CE1)	Chip select1 access time		110	ns
ta(CE2)	Chip select2 access time		110	ns
ta(OE)	Output enable access time		55	ns
tdis(CE1)	Output disable time after S-CE1# high		40	ns
tdis(CE2)	Output disable time after S-CE2 low		40	ns
tdis(OE)	Output disable time after S-OE# high		40	ns
ten(CE1)	Output enable time after S-CE1# low	10		ns
ten(CE2)	Output enable time after S-CE2 high	10		ns
ten(OE)	Output enable time after S-OE# low	5		ns
tv(A)	Data valid time after address	10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits		Unit
		Min	Max	
tcw	Write cycle time	110		ns
tw(WE)	Write pulse width	85		ns
tsu(A)	Address setup time	0		ns
tsu(A-WH)	Address setup time with respect to S-WE#	100		ns
tsu(CE1)	Chip select1 setup time	100		ns
tsu(CE2)	Chip select2 setup time	100		ns
tsu(D)	Data setup time	45		ns
th(D)	Data hold time	0		ns
trec(WE)	Write recovery time	0		ns
tdis(WE)	Output disable time from S-WE# low		40	ns
tdis(OE)	Output disable time from S-OEh# hig		40	ns
ten(WE)	Output enable time from S-WE# high	5		ns
ten(OE)	Output enable time from S-OE# low	5		ns

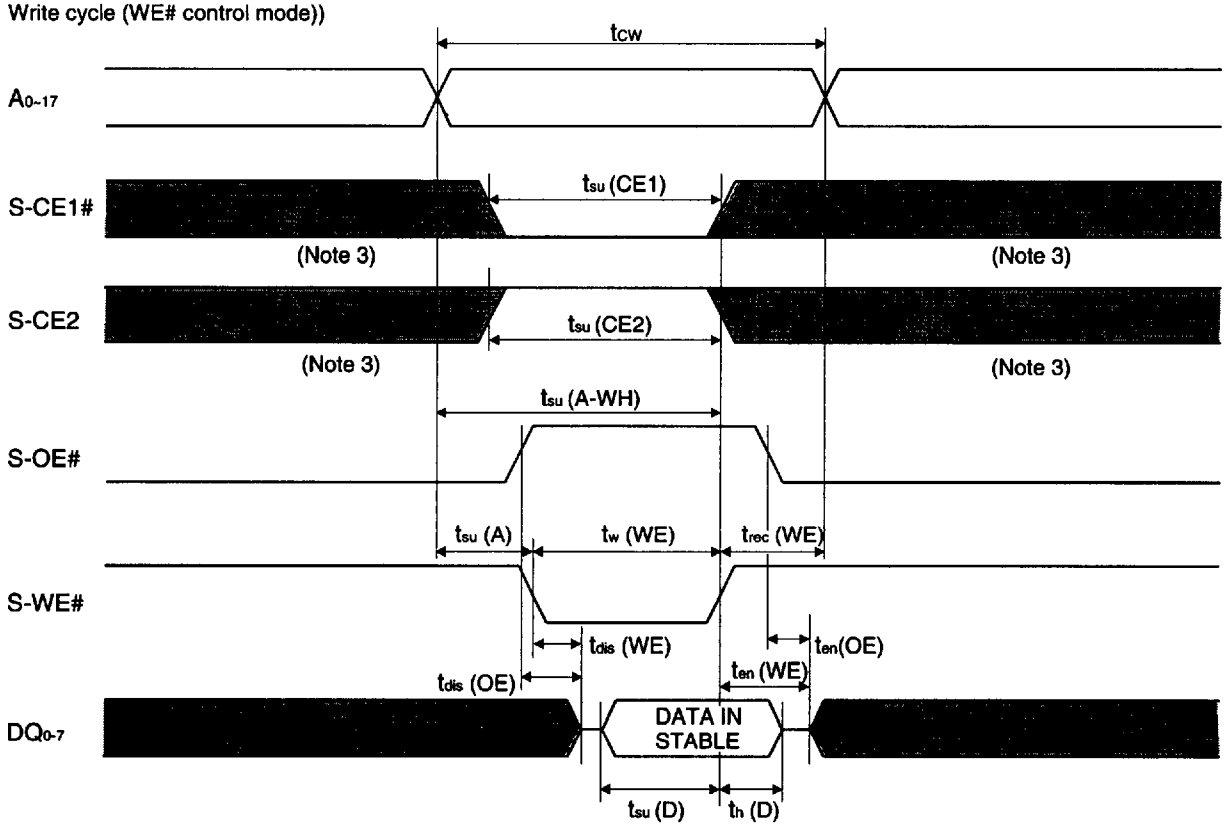
(4) TIMING DIAGRAMS

Read Cycle



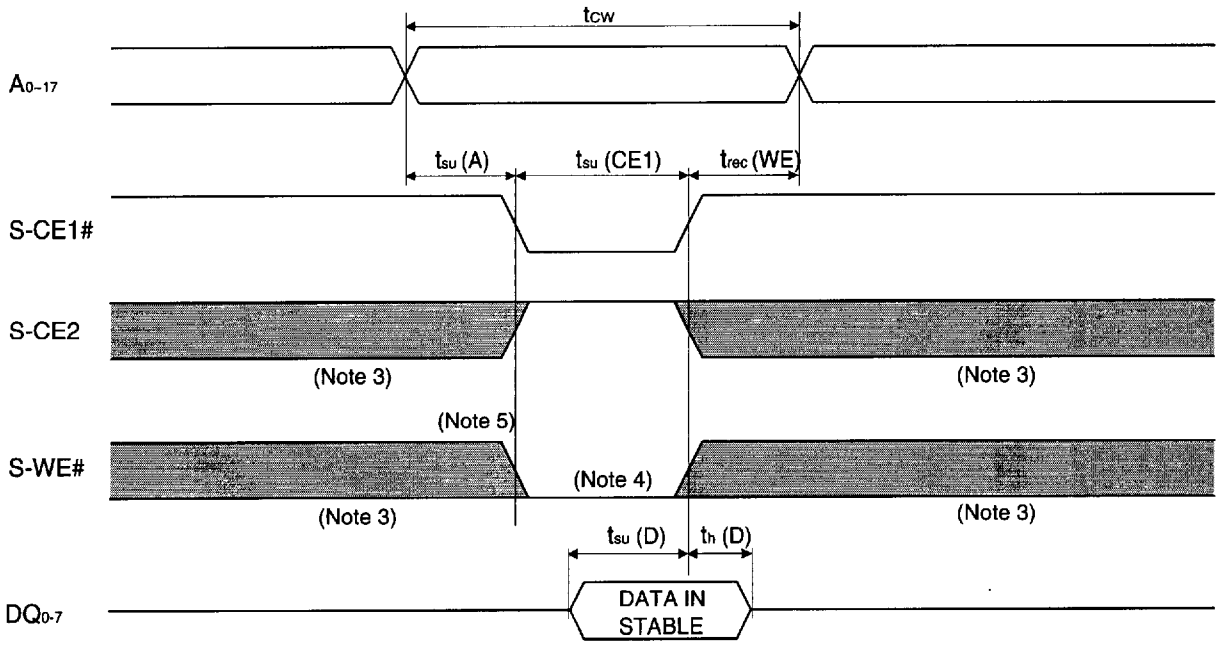
S-WE# = "H" level

Write cycle (WE# control mode))

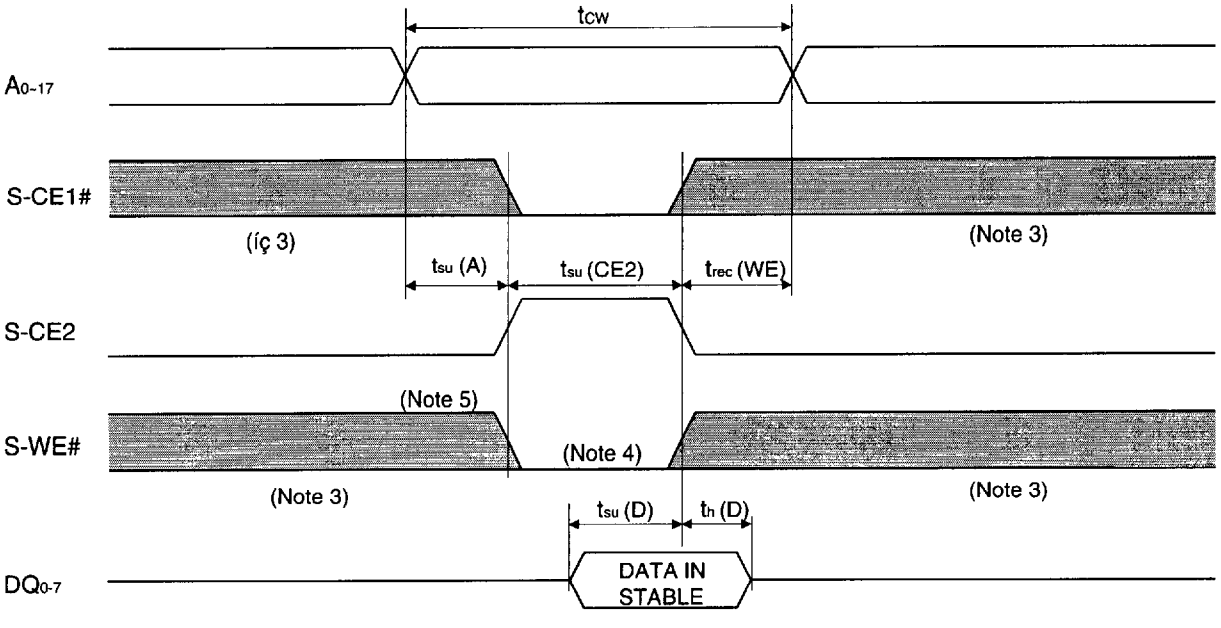


PRELIMINARY
Notice : This is not a final specification.
Some parametric limits are subject to change.

Write cycle (CE1# control mode)



Write cycle (CE2 control mode)



Note 3: Hatching indicates the state is "don't care".
4: Writing is executed while S-CE2 high overlaps S-CE1# and S-WE# low.
5: When the falling edge of S-WE# is simultaneously or prior to the falling edge of S-CE1# or rising edge of S-CE2, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRIAL CHARACTERISTICS (Ta=-20 ~ 85°C, unless otherwise noted)

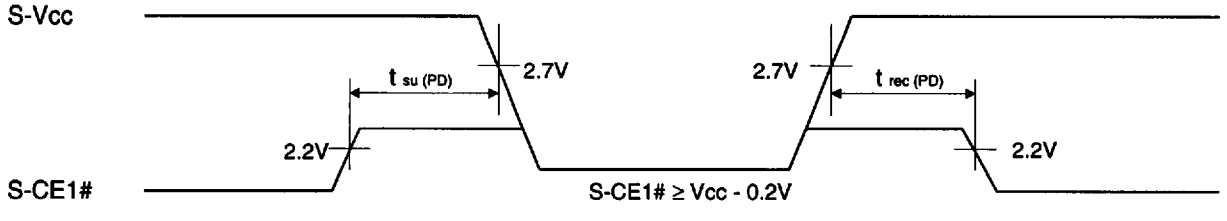
Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (CE1\#)}$	Chip select input S-CE1#			2.0			V
$V_{I\ (CE2)}$	Chip select input S-CE2					0.2	V
$I_{CC\ (PD)}$	Power down supply current	S-Vcc = 3V 1) S-CE2 ≤ 0.2V, other input = 0 ~ Vcc	-20~+85°C			30	μA
		2) S-CE1# ≥ Vcc-0.2V,S-CE2 ≥ Vcc-0.2V	-20~+40°C			3	
		other inputs = 0 ~ Vcc	+25°C		0.3	1	

(2) TIMING REQUIREMENTS (Ta=-20 ~ 85°C, unless otherwise noted)

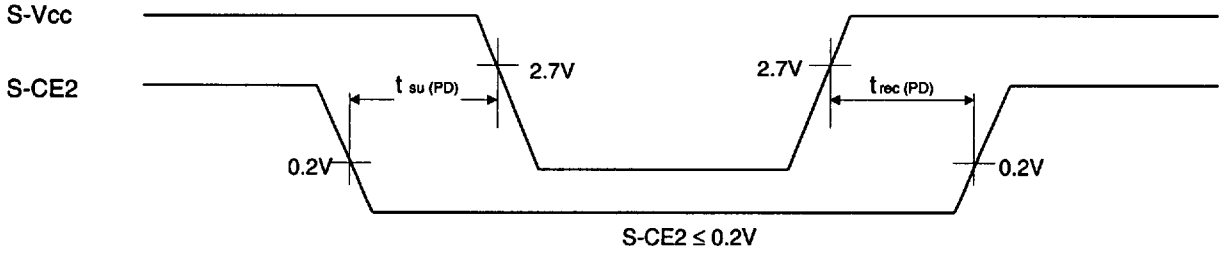
Symbol	Paramwter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

CE1# control mode



CE2 control mode

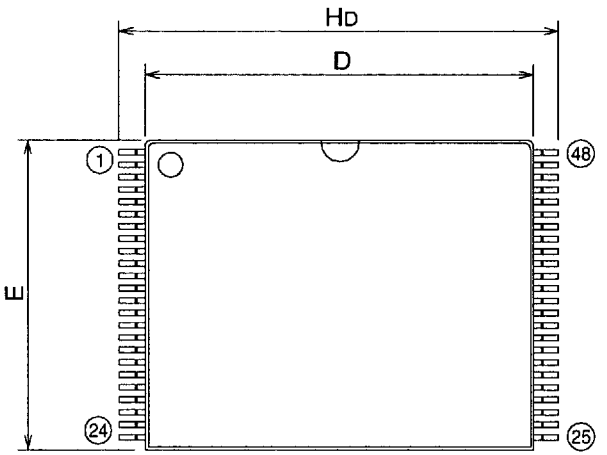


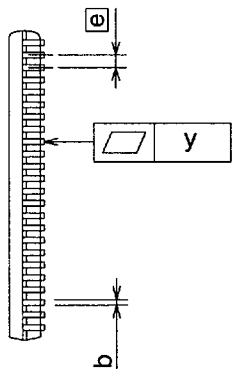
48PTC-B

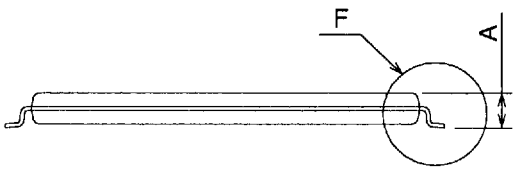
Plastic 48pin 10×14mm TSOP(I)

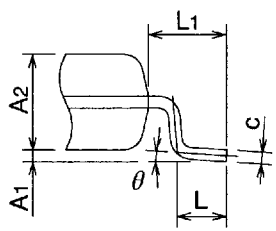
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP I 48-P-1014-0.40	–		Cu Alloy

Under Planning

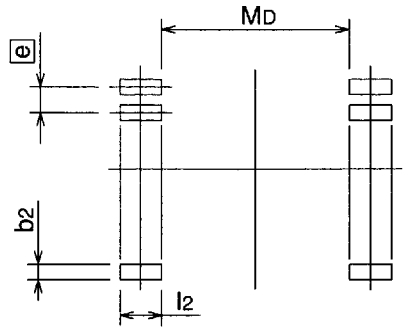








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A1	0.05	0.125	0.2
A2	–	1.0	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	12.3	12.4	12.5
E	9.9	10.0	10.1
e	–	0.4	–
HD	13.8	14.0	14.2
L	0.4	0.5	0.6
L1	–	0.8	–
y	–	–	0.08
θ	0°	–	10°
b2	–	0.2	–
l2	0.9	–	–
MD	–	12.6	–