M74DW66500B

2x 64Mbit (x8/ x16, Multiple Bank, Boot Block) Flash Memory and 32Mbit Pseudo SRAM, 3V Supply, Multiple Memory Product

PRELIMINARY DATA

FEATURES SUMMARY

- MULTIPLE MEMORY PRODUCT
  - Two 64Mbit (8M x8 or 4M x16), Multiple Bank, Page, Boot Block, Flash Memories
  - 32Mbit (2M x 16) Pseudo Static RAM
- SUPPLY VOLTAGE
  - V_{CCF} = V_{CCP} = 2.7 to 3.3V
  - V_{PPF} = 12V for Fast Program (optional)
- ACCESS TIME: 70, 90ns
- LOW POWER CONSUMPTION
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code: 227Eh + 2202h + 2201h

EACH FLASH MEMORY

- ASYNCHRONOUS PAGE READ MODE
  - Page Width: 4 Words
  - Page Access: 25, 30ns
  - Random Access: 70, 90ns
- PROGRAMMING TIME
  - 10µs per Byte/Word typical
  - 4 Words/ 8 Bytes at-a-time Program
- MEMORY BLOCKS
  - Quadruple Bank Memory Array: 8Mbits + 24Mbits + 24Mbits + 8Mbits
  - Parameter Blocks (at both Top and Bottom)
- DUAL OPERATIONS
  - While Program or Erase in a group of banks (from 1 to 3), Read in any of the other banks
- PROGRAM/ERASE SUSPEND and RESUME MODES
  - Read from any Block during Program Suspend
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming

Figure 1. Package

LFBGA73 (ZA)
8 x 11.6mm

- V_{PP}/$\overline{WP}$ PIN for FAST PROGRAM and WRITE PROTECT
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- EXTENDED MEMORY BLOCK
  - Extra block used as security block or to store additional information
- 100,000 PROGRAM/ERASE CYCLES per BLOCK

PSRAM

- ACCESS TIME: 70ns
- BYTE CONTROL: $\overline{UB}$/$\overline{LB}$
- PROGRAMMABLE PARTIAL ARRAY
- 8 WORD PAGE ACCESS CAPABILITY: 18ns (max)
- LOW STANDBY CURRENT: 100µA

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SUMMARY DESCRIPTION

The M74DW66500B is a low voltage Multiple Memory Product which combines two memory devices; a 64 Mbit Multiple Bank, Boot Block Flash memory (M29DW640D) and a 32 Mbit Pseudo SRAM. This document should be read in conjunction with the M29DW640D and M69AW048B datasheets.

Recommended operating conditions do not allow more than one of the internal memory devices to be active at the same time.

The memory is offered in an LFBGA73 (8 x 11.6mm, 0.8 mm pitch) package and is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

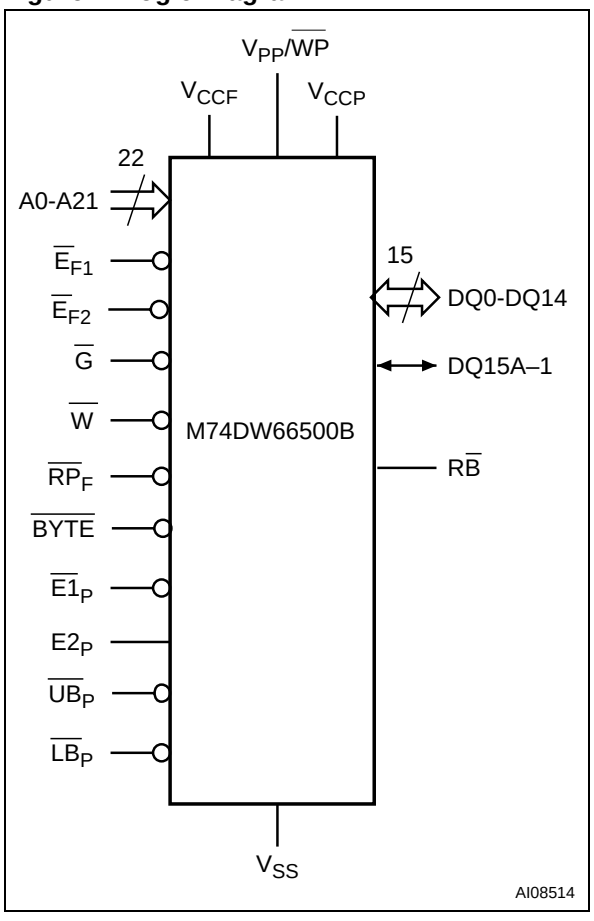
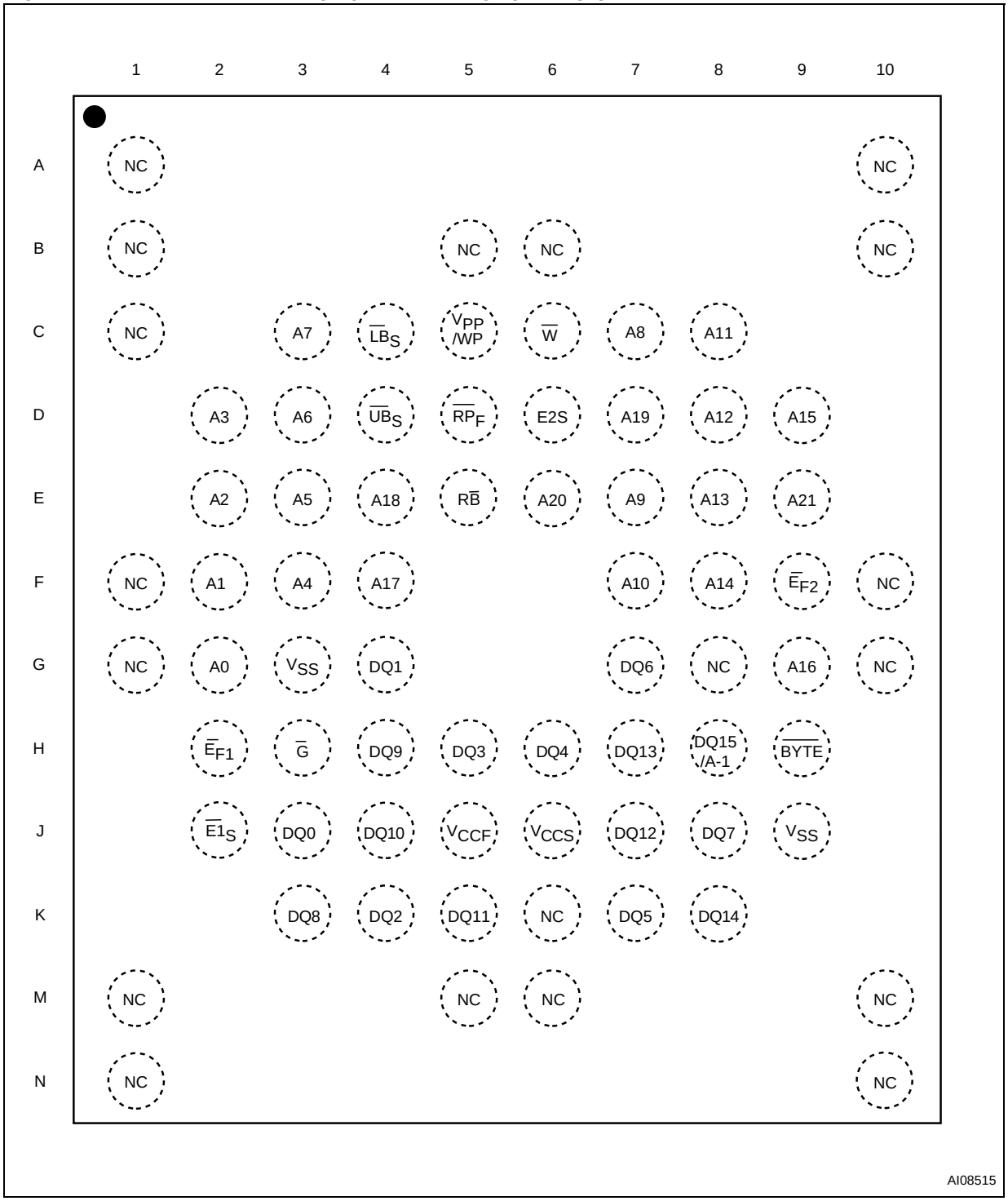


Table 1. Signal Names

A0-A20	Address Inputs common to the Flash Memory and PSRAM Components
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{G}$	Output Enable Input
$\overline{W}$	Write Enable Input
V_{CCF}	Flash Memory Power Supply
$V_{PP}/\overline{WP}$	V_{PP}/Write Protect
V_{SS}	Ground
V_{CCP}	PSRAM Power Supply
NC	Not Connected Internally
Flash Memory Control Functions	
A21	Address Input common to the two Flash Memory Devices
$\overline{E}_{F1}$	Flash-1 Chip Enable Input
$\overline{E}_{F2}$	Flash-2 Chip Enable Input
$\overline{RP}_F$	Reset/Block Temporary Unprotect
$\overline{RB}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organization Select
PSRAM Control Functions	
$\overline{E1}_P$, $E2_P$	Chip Enable Inputs
$\overline{UB}_P$	Upper Byte Enable Input
$\overline{LB}_P$	Lower Byte Enable Input

Figure 3. LFBGA Connections (Top view through package)



SIGNAL DESCRIPTION

See Figure 2 Logic Diagram and Table 1,Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A21). Address lines A0-A20 are common inputs for the Flash Memory and PSRAM components. Address line A21 is an input that is common for the two Flash Memory components. The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. The Flash memory is accessed through the Chip Enable ($\overline{E}_F$) and Write Enable ($\overline{W}$) signals, while the PSRAM is accessed through two Chip Enable signals ($\overline{E1}_S$ and $E2_S$) and the Write Enable signal ($\overline{W}$).

Data Inputs/Outputs (DQ0-DQ7). The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the Program/Erase Controller.

Data Inputs/Outputs (DQ8-DQ14). The Data I/O outputs the data stored at the selected address during a Bus Read operation when $\overline{BYTE}$ is High, V_{IH}. When $\overline{BYTE}$ is Low, V_{IL}, these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

Data Input/Output or Address Input (DQ15A–1). When $\overline{BYTE}$ is High, V_{IH}, this pin behaves as a Data Input/Output pin (as DQ8-DQ14). When $\overline{BYTE}$ is Low, V_{IL}, this pin behaves as an address pin; DQ15A–1 Low will select the LSB of the addressed Word, DQ15A–1 High will select the MSB. Throughout the text consider references to the Data Input/Output to include this pin when $\overline{BYTE}$ is High and references to the Address Inputs to include this pin when $\overline{BYTE}$ is Low except when stated explicitly otherwise.

Flash-1 Chip Enable ($\overline{E}_{F1}$) and Flash-2 Chip Enable ($\overline{E}_{F2}$). The Chip Enable input activates the memory to which it is attached, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, controls the Bus Read operation of the Flash Memory and PSRAM components.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the Flash Memory and PSRAM components.

V_{PP}/Write Protect (V_{PP}/$\overline{WP}$). The V_{PP}/Write Protect pin provides two functions. The V_{PP} function allows the Flash memory to use an external high voltage power supply to reduce the time required for Program operations. This is achieved by bypassing the unlock cycles and/or using the multiple Word (2 or 4 at-a-time) or multiple Byte Program (2, 4 or 8 at-a-time) commands. The Write Protect function provides a hardware method of protecting the four outermost boot blocks (two at the top, and two at the bottom of the address space).

When V_{PP}/Write Protect is Low, V_{IL}, the memory protects the four outermost boot blocks; Program and Erase operations in these blocks are ignored while V_{PP}/Write Protect is Low, even when $\overline{RP}_F$ is at V_{ID}.

When V_{PP}/Write Protect is High, V_{IH}, the memory reverts to the previous protection status of the four outermost boot blocks (two at the top, and two at the bottom of the address space). Program and Erase operations can now modify the data in these blocks unless the blocks are protected using Block Protection.

When V_{PP}/Write Protect is raised to V_{PP} the memory automatically enters the Unlock Bypass mode. When V_{PP}/Write Protect returns to V_{IH} or V_{IL} normal operation resumes. During Unlock Bypass Program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the Command Interface section. The transitions from V_{IH} to V_{PP} and from V_{PP} to V_{IH} must be slower than t_{VHVPP}. See the M29DW640D datasheet for more details.

Never raise V_{PP}/Write Protect to V_{PP} from any mode except Read mode, otherwise the memory may be left in an indeterminate state.

The V_{PP}/Write Protect pin must not be left floating or unconnected or the device may become unreliable. A 0.1µF capacitor should be connected between the V_{PP}/Write Protect pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program, I_{PP}.

Reset/Block Temporary Unprotect ($\overline{RP}_F$). The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all Blocks that have been protected.

Note that if $V_{PP}/\overline{WP}$ is at V_{IL}, then the two outermost boot blocks will remain protected even if $\overline{RP}_F$ is at V_{ID}.

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low, V_{IL}, for at least t_{PLPX}. After Reset/Block Temporary Unprotect goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or

t_{RHEL}, whichever occurs last. See the M29DW640D datasheet for more details.

Holding $\overline{RP}_F$ at V_{ID} will temporarily unprotect the protected Blocks in the memory. Program and Erase operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than t_{PHPHH}.

Ready/Busy Output ($\overline{RB}$). The Ready/Busy pin is an open-drain output that can be used to identify when the Flash memory is performing a Program or Erase operation. During Program or Erase operations Ready/Busy is Low, V_{OL}. Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Byte/Word Organization Select ($\overline{BYTE}$). The Byte/Word Organization Select pin is used to switch between the x8 and x16 Bus modes of the Flash memory. When Byte/Word Organization Select is Low, V_{IL}, the Flash memory is in x8 mode, when it is High, V_{IH}, the Flash memory is in x16 mode.

PSRAM Chip Enable inputs ($\overline{E1}_P$, $E2_P$). The Chip Enable inputs activate the PSRAM control logic, input buffers and decoders. $\overline{E1}_P$ at V_{IH} with $E2_P$ at V_{IH} deselects the memory, reducing the power consumption to the standby level, whereas $E2_P$ at V_{IL} deselects the memory and reduces the power consumption to the Power-down level, regardless of the level of $\overline{E1}_P$. $\overline{E1}_P$ and $E2_P$ can also be used to control writing to the PSRAM memory array, while $\overline{W}_P$ remains at V_{IL}. It is not allowed to set $\overline{E}_{F1}$ or $\overline{E}_{F2}$ at V_{IL}, $\overline{E1}_P$ at V_{IL} and $E2_P$ at V_{IH} at the same time.

PSRAM Upper Byte Enable ($\overline{UB}_P$). The Upper Byte Enable input enables the upper byte for PSRAM (DQ8-DQ15). $\overline{UB}_P$ is active low.

PSRAM Lower Byte Enable ($\overline{LB}_P$). The Lower Byte Enable input enables the lower byte for PSRAM (DQ0-DQ7). $\overline{LB}_P$ is active low.

V_{CCF} Supply Voltage (2.7 to 3.3V). V_{CCF} provides the power supply for Flash memory operations (Read, Program and Erase).

The Command Interface is disabled when the V_{CCF} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CCF} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Program and Erase operations, I_{CC3}.

V_{CCP} Supply Voltage (2.7 to 3.3V). V_{CCP} provides the power supply for the PSRAM.

V_{SS} Ground. V_{SS} is the ground reference for all voltage measurements in the Flash and PSRAM chips.

FUNCTIONAL DESCRIPTION

The Flash Memory and PSRAM components have a common power supply. The components are distinguished by four chip enable inputs: $\overline{E}_{F1}$ for one Flash memory, $\overline{E}_{F2}$ for the other, and $\overline{E1}_S$ and $E2_S$ for the PSRAM.

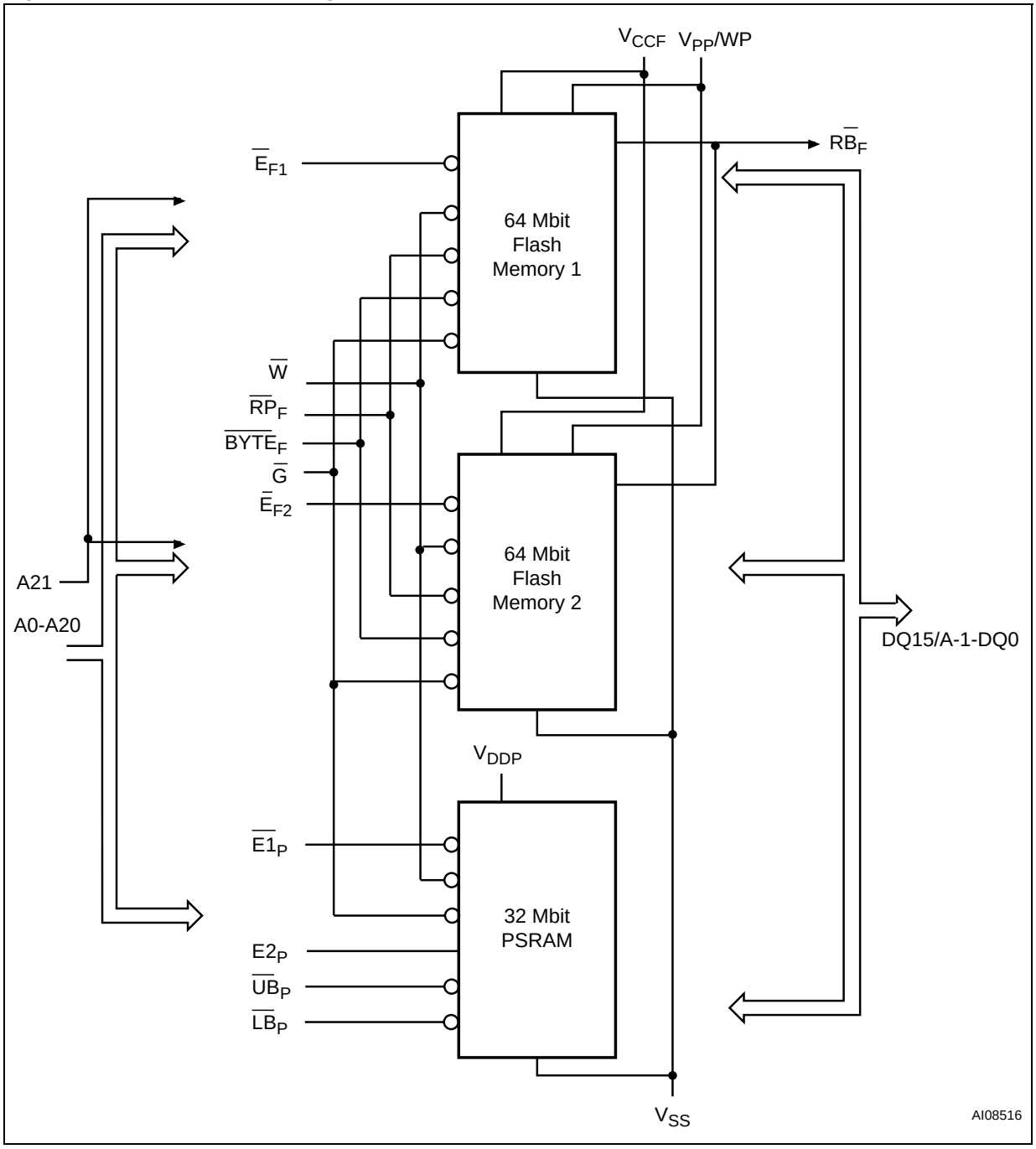
Recommended operating conditions do not allow more than one of the Flash Memory or PSRAM component to be in active mode at the same time. The most common example is simultaneous read operations on the Flash Memory and PSRAM components which would result in a data bus contention. Therefore it is recommended to put two of the components in the high impedance state when reading from the third (see Table 2 Main Operation Modes for details).

Table 2. Main Operation Modes

Operation Mode[3]		$\overline{E}_{F1}$	$\overline{E}_{F2}$	$\overline{RP}_F$	$\overline{G}$	$\overline{W}$	$\overline{E1}_P$	$E2_P$	$\overline{UB}_P$, $\overline{LB}_P$[2]	DQ15-DQ0
Flash Memory 1	Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	Flash Memory 2 and PSRAM must both be in Standby			Flash Memory 1 Data Output
	Write	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}				Flash Memory 1 Data Input
	Output Disable	X	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Any Flash Memory 2 or PSRAM mode is allowed			Flash Memory 1 Hi-Z
	Standby	V_{IH}	V_{IH}	V_{CC} ±0.3	X	X				
	Reset	X	V_{IH}	V_{IL}	X	X				
Flash Memory 2	Read	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Flash Memory 1 and PSRAM must both be in Standby			Flash Memory 2 Data Output
	Write	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}				Flash Memory 2 Data Input
	Output Disable	V_{IH}	X	V_{IH}	V_{IH}	V_{IH}	Any Flash Memory 1 or PSRAM mode is allowed			Flash Memory 2 Hi-Z
	Standby	V_{IH}	V_{IH}	V_{CC} ±0.3	X	X				
	Reset	V_{IH}	X	V_{IL}	X	X				
PSRAM	Read	Both Flash Memories must be in Standby			V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	PSRAM Data Output
	Write				V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	PSRAM Data Input
	Output Disable	Any One Flash Memory mode is allowable			V_{IH}	V_{IH}	V_{IL}	V_{IH}	X	PSRAM Hi-Z
	Standby				X	X	V_{IH}	V_{IH}	X	
	Deep Power Down				X	X	X	V_{IL}	X	

Note: 1. X = Don't Care (V_{IL} or V_{IH}).
2. $\overline{UB}_P$ and $\overline{LB}_P$ are tied together.
3. This table is valid when $\overline{BYTE}$ = V_{IH}. This table is also valid when $\overline{BYTE}$ = V_{IL}, with the only difference that DQ15-DQ8 are always high impedance when the Flash Memory components are being accessed.
4. For the Block Protect and Unprotect features, refer to the M29DW640D datasheet. Only the In-System Technique is available in the stacked product.
5. To read the Manufacturer Code, the Device Code, the Block Protection Status and the Extended Block indicator bit, refer to the "Auto Select Command" in the M29DW640D datasheet.

Figure 4. Functional Block Diagram



FLASH MEMORY DEVICES

The M74DW66500B contains two 64Mbit Flash memories. For detailed information on how to use these, see the M29DW640D datasheet, which is available on the STMicroelectronics web site, www.st.com.

PSRAM DEVICE

The M74DW66500B contains a 32Mbit Pseudo SRAM. For detailed information on how to use it, see the M69AW048B datasheet, which is available from your local STMicroelectronics distributor.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature (1)	–40	85	°C
T_{BIAS}	Temperature Under Bias	–50	125	°C
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input or Output Voltage	–0.5	V_{CCF} +0.3	V
V_{CCF}	Flash Supply Voltage	–0.6	4	V
V_{ID}	Identification Voltage	–0.6	13.5	V
V_{PPF}	Program Voltage	–0.6	13.5	V
V_{CCP}	PSRAM Supply Voltage	–0.5	3.6	V

Note: 1. Depends on range.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 4, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

The operating and AC measurement parameters given in this section (see Table 4 below) correspond to those of the stand-alone Flash Memory and PSRAM components. For compatibility purposes, the M29DW640D voltage range is restricted to V_{CCS} in the stacked product.

Table 4. Operating and AC Measurement Conditions

Parameter	Flash Memories		PSRAM		Units
	Min	Max	Min	Max	
V_{CCF} Supply Voltage	2.7	3.6	–	–	V
V_{CCS} Supply Voltage	–	–	2.7	3.3	V
Ambient Operating Temperature	–40	85	–30	85	°C
Load Capacitance (C_L)	30		30		pF
Input Rise and Fall Times		10		5	ns
Input Pulse Voltages	0 to V_{CCF}		0 to V_{CCP}		V
Input and Output Timing Ref. Voltages	$V_{CCF}/2$		$V_{CCP}/2$		V

Figure 5. AC Measurement I/O Waveform

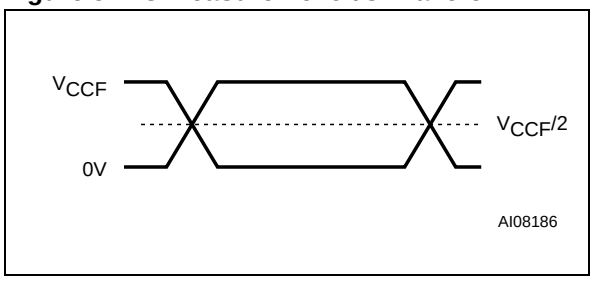


Figure 6. AC Measurement Load Circuit

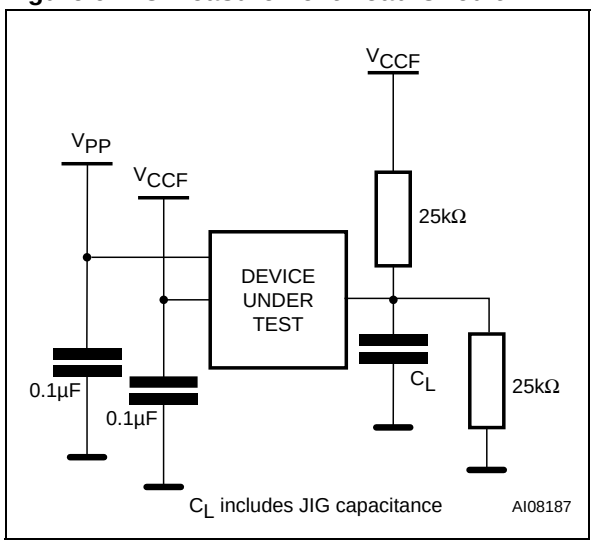


Table 5. Device Capacitance

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f=1 MHz		12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f=1 MHz		15	pF

Note: Sampled only, not 100% tested.

Table 6. Flash DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1} (2)	Supply Current (Read)	$\overline{E}_F = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz			10	mA
I_{CC2}	Supply Current (Standby)	$\overline{E}_F = V_{CC} \pm 0.2V$, $\overline{RP}_F = V_{CC} \pm 0.2V$			100	µA
I_{CC3} (1,2)	Supply Current (Program/ Erase)	Program/Erase Controller active	$V_{PP}/\overline{WP}$ = V_{IL} or V_{IH}		20	mA
			$V_{PP}/\overline{WP} = V_{PP}$		20	mA
V_{IL}	Input Low Voltage			–0.5	0.8	V
V_{IH}	Input High Voltage			$0.7V_{CC}$	V_{CC} +0.3	V
V_{PP}	Voltage for $V_{PP}/\overline{WP}$ Program Acceleration	V_{CC} = 3.0V ±10%		11.5	12.5	V
I_{PP}	Current for $V_{PP}/\overline{WP}$ Program Acceleration	V_{CC} = 3.0V ±10%			15	mA
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA		V_{CC} –0.4		V
V_{ID}	Identification Voltage			11.5	12.5	V
V_{LKO}	Program/Erase Lockout Supply Voltage			1.8	2.3	V

Note: 1. Sampled only, not 100% tested.
2. In Dual operations the Supply Current will be the sum of I_{CC1}(read) and I_{CC3} (program/erase).

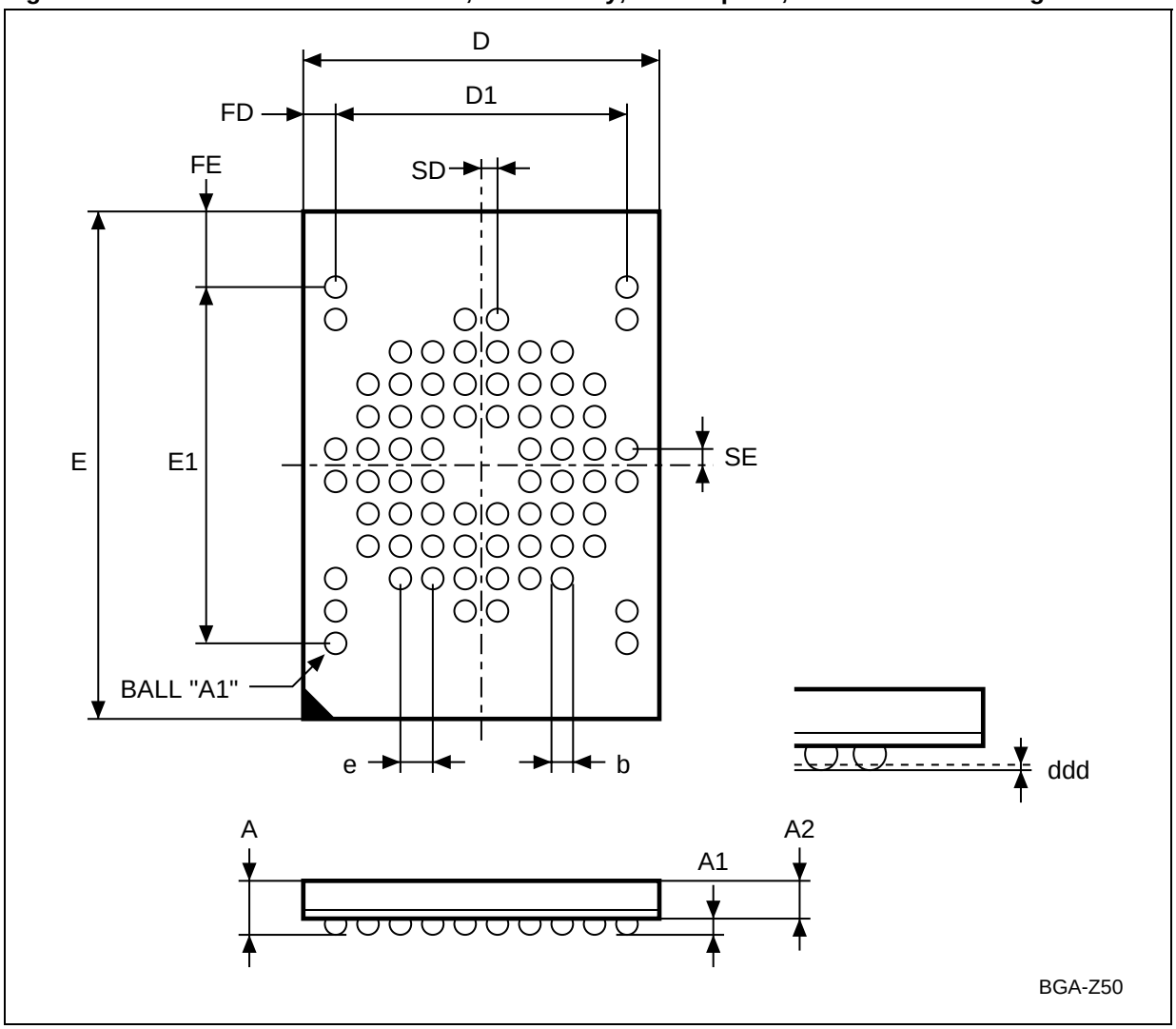
Table 7. PSRAM DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{CC1}	V_{CC} Active Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1} = V_{IL}$ and E2 = V_{IH}, I_{OUT} = 0mA	t_{RC} / t_{WC} = minimum		30	mA
I_{CC2}			t_{RC} / t_{WC} = 1 µs		3	mA
I_{CC3}	V_{CC} Page Read Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1} = V_{IL}$ and E2 = V_{IH}, I_{OUT} = 0mA, t_{PRC} = min.			10	mA
I_{CCPD}	V_{CC} Power Down Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, E2 ≤ 0.2V	Sleep		10	µA
I_{CCP4}			4M partial		40	µA
I_{CCP8}			8M partial		50	µA
I_{CCP16}			16M partial		65	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1}$ = E2 = V_{IH}			1.5	mA
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		–1	1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		–1	1	µA
I_{SB}	Standby Supply Current CMOS	V_{CC} = 3.3V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} –0.2V, $\overline{E1}$ = E2 ≥ V_{CC} –0.2V			100	µA
V_{IH} (1)	Input High Voltage			0.8V_{CC}	V_{CC} + 0.2	V
V_{IL} (2)	Input Low Voltage			–0.3	0.2V_{CC}	V
V_{OH}	Output High Voltage	V_{CC} = 2.7V, I_{OH} = –0.5mA		1.4		V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.4	V

Note: 1. Maximum DC voltage on input and I/O pins is V_{CC} + 0.2V.
During voltage transitions, input may positive overshoot to V_{CC} + 1.0V for a period of up to 5ns.
2. Minimum DC voltage on input or I/O pins is –0.3V.
During voltage transitions, input may positive overshoot to V_{SS} + 1.0V for a period of up to 5ns.

PACKAGE MECHANICAL

Figure 7. Stacked LFBGA73 8x11.6mm, 10x12 array, 0.8mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 8. Stacked LFBGA73 8x11.6mm, 10x12 array, 0.8mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.400			0.0551
A1		0.250			0.0098	
A2	0.910			0.0358		
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	7.200			0.2835		
ddd			0.100			0.0039
E	11.600	11.500	11.700	0.4567	0.4528	0.4606
E1	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	0.400			0.0157		
FE	1.400			0.0551		
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

PART NUMBERING

Table 9. Ordering Information Scheme

Example: M74DW 6 6 5 0 0 B 70 Z T

Device Type
M74 = MMP (Flash + PSRAM)

Architecture
D = Dual Operation

Operating Voltage
W = V_{CCF} = V_{CCP} = 2.7V to 3.3V

Flash Memory 1 Device Size (Die1 Density)
6 = 64 Mbit

Flash Memory 2 Device Size (Die2 Density)
6 = 64 Mbit

PSRAM Device Size (Die3 Density)
5 = 32 Mbit

Die4
0 = none present

Flash Memory Specification Details
0 = Multiple Bank

Stacked Specification Details
B=0.15µm Flash Memory and 0.18µm PSRAM

Speed
70 = 70ns
90 = 90ns

Package and Temperature Range
Z = LFBGA73: 8 x 11.6mm, 0.8mm pitch

Option
T = Tape & Reel packing

Note: This product is also available with the Extended Block factory locked. For further details and ordering information contact your nearest ST sales office.

Devices are shipped from the factory with the memory content bits erased to ’1’.
For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

REVISION HISTORY

Table 10. Document Revision History

Date	Version	Revision Details
19-May-2003	1.0	First Issue
24-Sep-2003	1.1	Voltage supply range extended 2.7V working at all speed options