

Am79231

Intelligent Subscriber Line Interface Circuit (ISLIC™)



DISTINCTIVE CHARACTERISTICS

- **Monitor of two-wire interface voltages and currents supports**
 - Voice transmission
 - Programmable DC feed characteristics
 - Independent of battery
 - Current limited
 - Selectable off-hook and ground-key thresholds
 - Subscriber line diagnostics
 - Leakage resistance
 - Loop resistance
 - Line capacitance
 - Bell capacitance
 - Foreign voltage sensing
 - Power cross and fault detection

- **+5 V and battery supplies**
- **Dual battery operation for system power saving**
 - Automatic battery switching
 - Intelligent thermal management
- **Compatible with inexpensive protection networks**
 - Accommodates low tolerance fuse resistors or PTC thermistors
- **Metering capable**
 - 12 kHz and 16 kHz
 - Smooth polarity reversal
- **Tip-open state supports ground start signaling**
- **Ring relay driver for external ringing**
- **Integrated test load switches/relay drivers**

BLOCK DIAGRAM

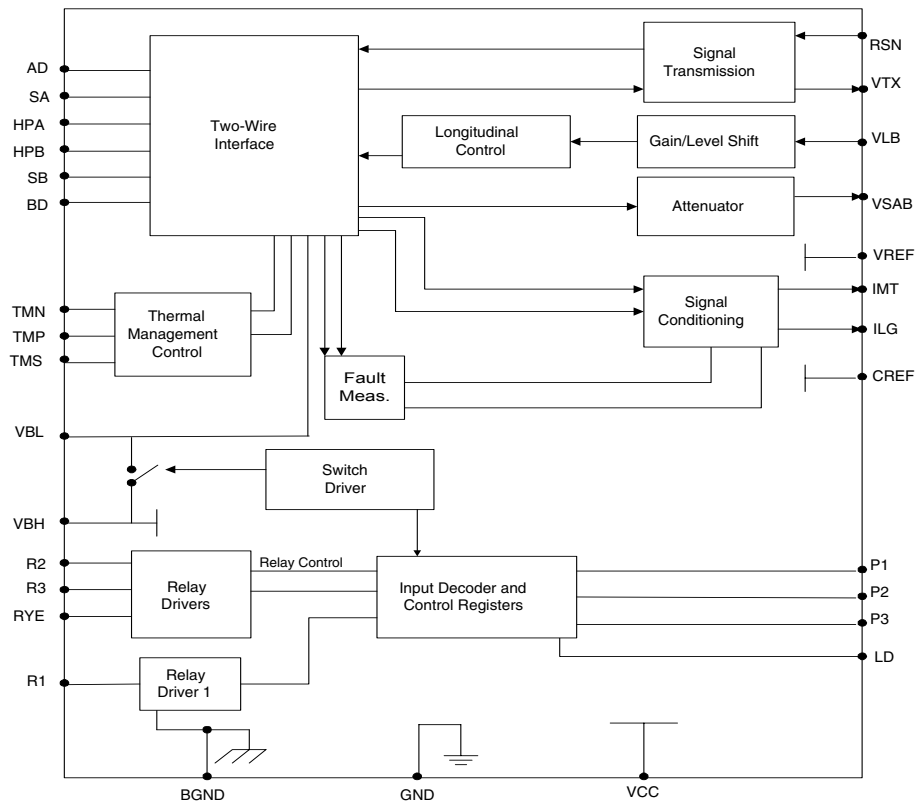


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The Am79231, in combination with an ISLAC™ device, implements the telephone line interface function. This enables the design of a low cost, high performance, fully software programmable line interface for multiple country applications worldwide. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces on the ISLAC device. Additionally, the Am79231 device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

DISTINCTIVE CHARACTERISTICS OF THE INTELLIGENT ACCESS™ VOICE CHIPSET

- **Performs all battery feed, ring-trip, signaling, hybrid and test (BORSCHT) functions**
- **Two chip solution supports high density, multi-channel architecture**
- **Single hardware design meets multiple country requirements through software programming of:**
 - DC loop-feed characteristics and current-limit
 - Loop-supervision detection thresholds
 - Off-hook debounce circuit
 - Ground-key and ring-trip filters
 - Off-hook detect de-bounce interval
 - Two-wire AC impedance
 - Transhybrid balance
 - Transmit and receive gains
 - Equalization
 - Digital I/O pins
 - A-law/ μ -law and linear selection
- **Supports external battery-backed ringing**
 - Unbalanced ringing
 - Ring relay driver
 - Ring relay operation synchronized to zero crossings of ringing voltage and current
 - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- **Supports metering generation with envelope shaping**
- **Smooth or abrupt polarity reversal**
- **Adaptive transhybrid balance**
 - Continuous or adapt and freeze
- **Supports both loop-start and ground-start signaling**
- **Exceeds LSSGR and CCITT central office requirements**
- **Selectable PCM or GCI interface**
 - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- **On-hook transmission**
- **Power/service denial mode**
- **Line-feed characteristics independent of battery voltage**
- **Only 5 V, 3.3 V and battery supplies needed**
- **Low idle-power per line**
- **Linear power-feed with intelligent power-management feature**
- **Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance**
- **Monitors two-wire interface voltages and currents for subscriber line diagnostics**
- **Built-in voice-path test modes**
- **Power-cross, fault, and foreign voltage detection**
- **Integrated line-test features**
 - Leakage
 - Line and ringer capacitance
 - Loop resistance
- **Integrated self-test features**
 - Echo gain, distortion, and noise
- **0 to 70°C commercial operation**
 - -40°C to 85°C extended temperature range available
- **Small physical size**
- **Up to three relay drivers per ISLIC™ device**
 - Configurable as test load switches

BLOCK DIAGRAMS

Figure 1. Example Four-Channel Linecard Block Diagram

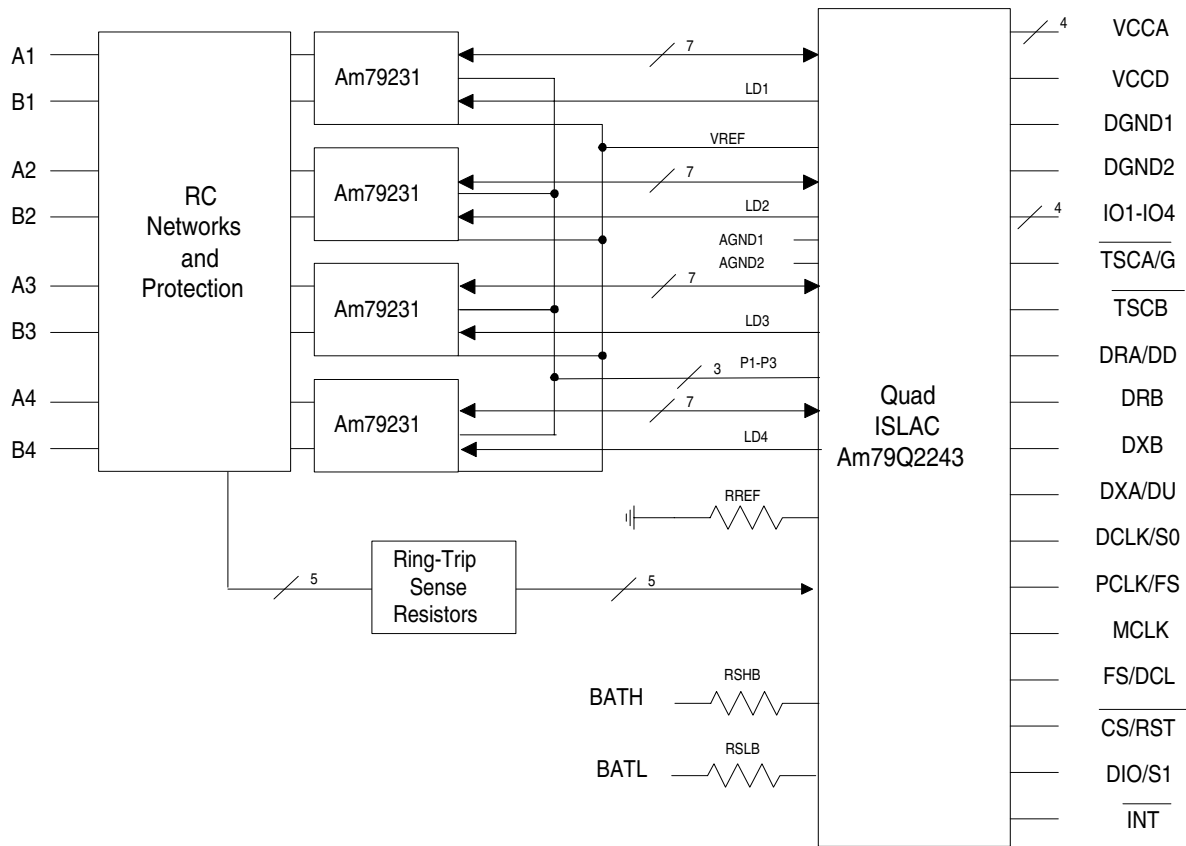
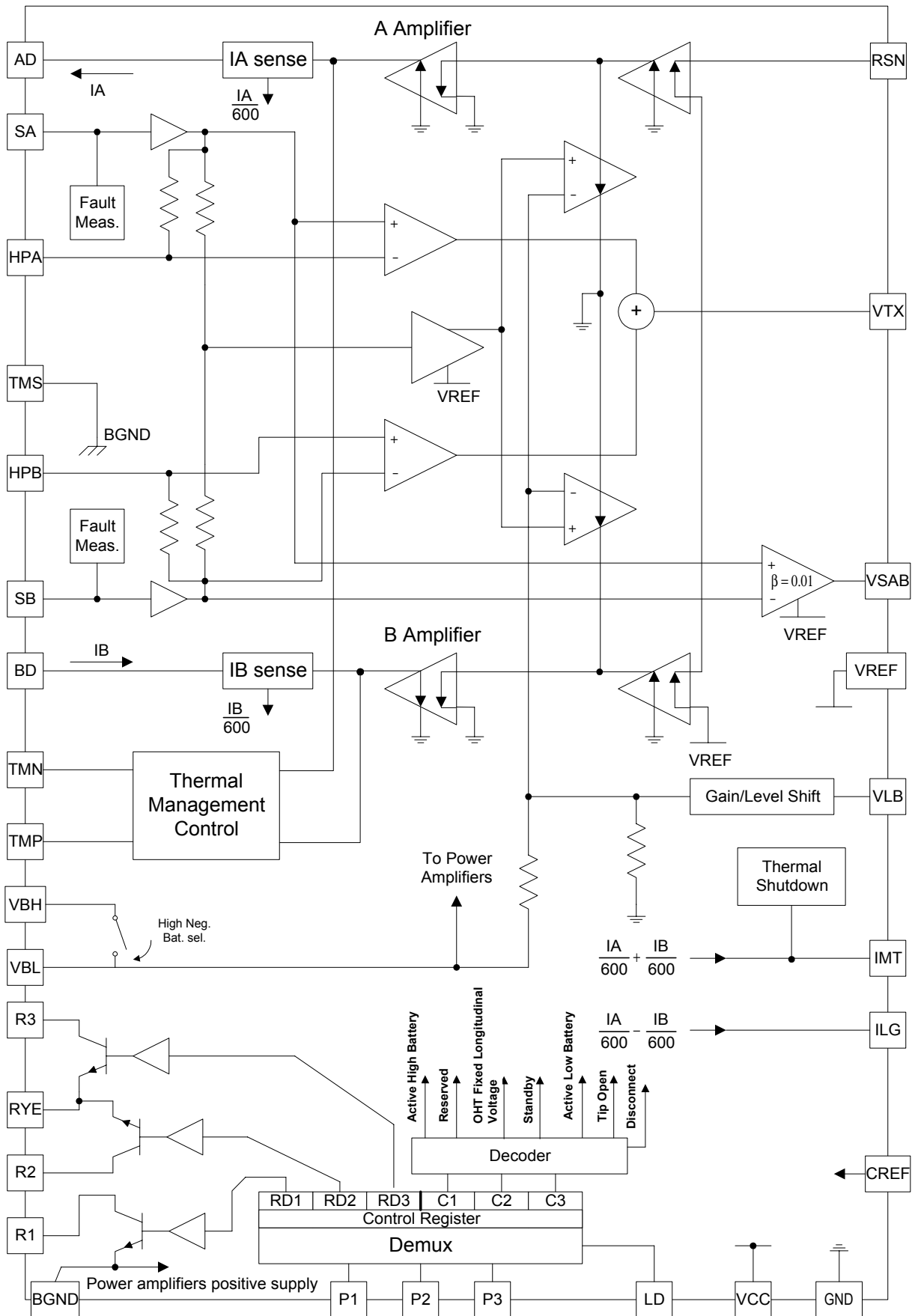
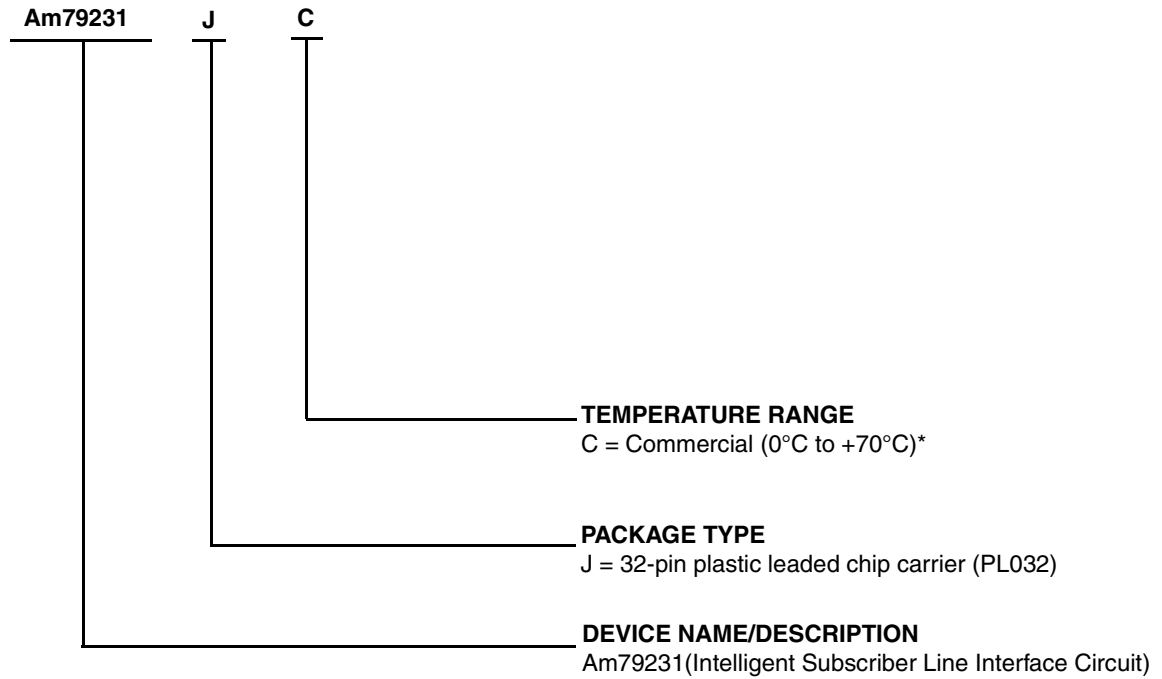


Figure 2. Am79231 Block Diagram



ORDERING INFORMATION

Legerity standard products are available in several packages and operating ranges. The ordering number (valid combination) is formed by a combination of the elements below. An ISLAC device must be used with this part.



Valid Combinations	
Am79231	JC

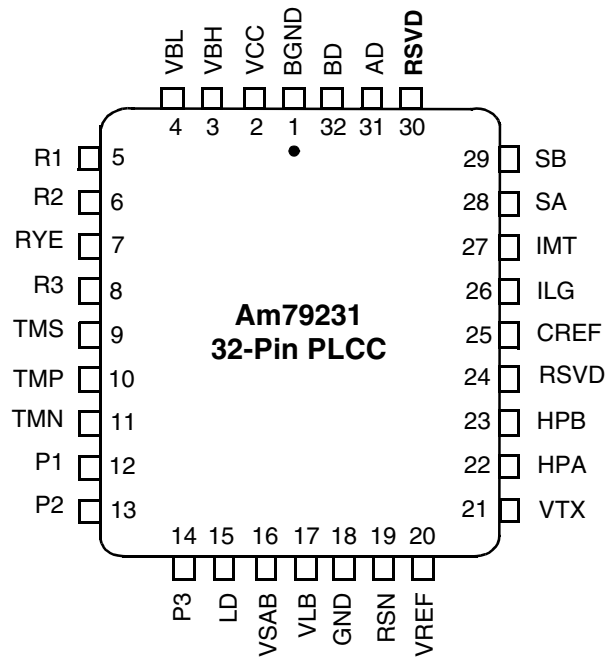
Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

Note:

**Functionality of the device from 0°C to 70°C is guaranteed by production testing. Performance from -40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAM



PIN DESCRIPTIONS

Pin	Pin Name	I/O	Description
AD, BD	A, B Line Drivers	O	Provide the currents to the A and B leads of the subscriber loop.
BGND	Ground		Ground return for high and low battery supplies.
CREF	+3.3 VDC		VCCD reference. It is the digital high logic supply rail, used by the ISLIC to ISLAC interface.
GND	Ground		Analog and digital ground return for VCC.
HPA, HPB	High-Pass Filter Capacitor	O	These pins connect to CHP, the external high-pass filter capacitor that separates the DC loop-voltage from the voice transmission path.
ILG	Longitudinal Current Sense	O	ILG is proportional to the common-mode line current (IAD-IBD), except in disconnect mode, where ILG is proportional to the current into grounded SB.
IMT	Metallic Current Sense	O	IMT is proportional to the differential line current (IAD + IBD), except in disconnect mode, where IMT is proportional to the current into grounded SA. The Am79231 indicates thermal overload by pulling IMT to CREF.
LD	Register Load	I	The LD pin controls the input latch and responds to a 3-level input. When the LD pin is a logic 1 ($>(V_{ref}+0.3V)$), the logic levels on P1-P3 latch into the Am79231 control register bits that operate the mode-decoder. When the LD pin is a logic 0 ($<(V_{ref}-0.3V)$), the logic levels on P1-P3 latch into the Am79231 control register bits that control the relay drivers (RD1-RD3). When the LD pin level is at $\sim V_{REF}$, the control register contents are locked.
P1-P3	Control Bus	I	Inputs to the latch for the operating-mode decoder and the relay-drivers.
R1	Ring Relay Driver	O	Collector connection for ring relay driver. Emitter internally connected to BGND.
R2	Relay 2 Driver	O	Collector connection for relay 2 driver. Emitter internally connected to RYE
R3	Relay 3 Driver	O	Collector connection for relay 3 driver. Emitter internally connected to RYE.
RSN	Receive Summing Node	I	The metallic current between AD and BD is equal to 500 times the current into this pin. Networks that program receive gain and two-wire impedance connect to this node. This input is at a virtual potential of VREF.
RSVD	Reserved		This is used during Legerity testing. In the application, this pin must be left floating.
RYE	Relay 2, 3 Common Emitter	O	Emitter connection for R2 and R3. Normally connected to relay ground.
SA, SB	A, B Lead Voltage Sense	I	Sense the voltages on the line side of the fuse resistors at the A and B leads. External sense resistors, RSA and RSB, protect these pins from lightning or power-cross.
TMP, TMN, TMS	Thermal Management		External resistors connected from TMP to TMS and TMN to VBL to offload excess power from the Am79231.
VBH	Battery (Power)		Connection to high-battery supply used for ringing and long loops. Connects to the substrate. When only a single battery is available, it connects to both VBH and VBL.
VBL	Battery (Power)		Connection to low-battery supply used for short loops. When only a single battery is available, this pin can be connected to VBH.
VCC	+5 V Power Supply		Positive supply for low voltage analog and digital circuits in the Am79231.
VLB	Longitudinal Voltage	I	Sets the DC longitudinal voltage of the Am79231. It is the reference for the longitudinal control loop. When the VLB pin is greater than VREF, the Am79231 sets the longitudinal voltage to a voltage approximately half-way between the positive and negative power supply battery rails. When the VLB pin is driven to levels between 0V and VREF, the longitudinal voltage decreases linearly with the voltage on the VLB pin.
VREF	1.4 V Analog Reference	I	The ISLAC chip provides this voltage which is used by the Am79231 for internal reference purposes. All analog input and output signals interfacing to the ISLAC chip are referenced to this pin.
VSAB	Loop Voltage	O	Scaled-down version of the voltage between the sense points SA and SB on this pin.
VTX	4-Wire Transmit Signal	O	The voltage between this pin and VREF is a scaled down version of the AC component of the voltage sensed between the SA and SB pins. One end of the two-wire input impedance programming network connects to VTX. The voltage at VTX swings positive and negative with respect to VREF.

GENERAL DESCRIPTION

The Intelligent Access™ voice chipsets integrate all functions of the subscriber line. Two chip types are used to implement the linecard; an Am79231 device and an ISLAC device. These provide the following basic functions:

1. The Am79231: A high voltage, bipolar device that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The ISLAC device: A low voltage CMOS IC that provides conversion, control and DSP functions for the Am79231.

Complete schematics of a linecard using the Intelligent Access voice chipsets for external ringing is shown in Figure 3.

The Am79231 uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the ISLAC device to operate in eight different modes that control power consumption and signaling. This enables it to have full control over the subscriber loop. The Am79231 is designed to be used exclusively with the ISLAC devices. The Am79231 requires only +5 V power and the battery supplies for its operation.

The Am79231 implements a linear loop-current feeding method with the enhancement of intelligent Thermal Management. This limits the amount of power dissipated on the Am79231 chip by dissipating power in external resistors in a controlled manner.

Each ISLAC device contains high-performance circuits that provide A/D and D/A conversion for the voice (codec), DC-feed and supervision signals. The ISLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Intelligent Access voice chipset provides a complete software configurable solution to the BOR-SCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chipsets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide linecard requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge. It allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The Am79231 interface unit inside the ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the ISLAC device to place several key Am79231 performance parameters under software control.

The main functions that can be observed and/or controlled through the ISLAC backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth battery reversal
- Subscriber line matching

- Ringing
- Sophisticated line and circuit tests

To accomplish these functions, the ISLIC device collects the following information and feeds it, in analog form, to the ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltage

The outputs supplied by the ISLAC device to the ISLIC device are then:

- A voltage (VHLi) that provides control for the following high-level ISLIC device outputs:
 - DC loop current
 - 12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal (VOUTi)
- A voltage that controls longitudinal offset for test purposes (VLBi)

The ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or μ -law.

Besides the codec functions, the Intelligent Access voice chipset provides all the sensing, feedback, and clocking necessary to completely control ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The ISLAC device supplies complete mode control to the ISLIC device using the control bus (P1-P3) and tri-level load signal (LDi).

The Intelligent Access voice chipset provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built-in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual measurement data directly to a higher level processor by way of the PCM voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

LINECARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the linecard ($i = 1, 2, 3, 4$).

Item	Type	Value	Tol.	Rating	Comments
U1	Am79231				ISLIC device
U2	Am79X22xx				ISLAC device
U5	TISP61089			80 V	Transient Voltage Suppressor, Power Innovations
DHi, DLi, DT1i, DT2i ⁴	Diode	100 mA		100 V	50 ns
RFAi, RFBi	Resistor	50 Ω	2%	2 W	Fusible PTC protection resistors
RSAi, RSBi	Resistor	200 k Ω	2%	1/4 W	Sense resistors
RTi	Resistor	80.6 k Ω	1%	1/10 W	
RRXi	Resistor	100 k Ω	1%	1/10 W	
RREF	Resistor	69.8 k Ω	1%	1/10 W	Current reference
RMGLi, RMGPi	Resistor	1 k Ω	5%	1 W	Thermal management resistors
RSHB, RSLB	Resistor	750 k Ω	1%	1/8 W	Battery Sense Resistors
RHLai	Resistor	40.2 k Ω	1%	1/10 W	
RHLbi	Resistor	4.32 k Ω	1%	1/10 W	
RHLci	Resistor	2.87 k Ω	1%	1/10 W	
RHLdi	Resistor	2.87 k Ω	1%	1/10 W	
CHLbi	Capacitor	3.3 nF	10%	10 V	Not Polarized
CHLdi	Capacitor	0.82 μ F	10%	10 V	Ceramic
RMTi	Resistor	3.01 k Ω	1%	1/8 W	Metallic Current Sense Resistors
RLGi	Resistor	6.04 k Ω	1%	1/8 W	Longitudinal Current Sense Resistors
RTEST	Resistor	2 k Ω	1%	1 W	Test board
CADi, CBDi ¹	Capacitor	22 nF	10%	100 V	Ceramic, not voltage sensitive
CBATHi, CBATLi	Capacitor	100 nF	20%	100 V	Ceramic
CHPi	Capacitor	22 nF	20%	100 V	Ceramic
CSi ¹	Capacitor	100 nF	20%	100 V	Protector speed-up capacitor
CSSi ³	Capacitor	56 pF	5%	100 V	Ceramic
RGFDi	Resistor	510 Ω	2%	2 W	1.2 W typ
RSRBi, RSRc	Resistor	750 k Ω	2%	1/4 W	Matched to within 0.2% for initial tolerance and 0 to 70° C ambient temperature range. ² 17 mW typ
KRi	Relay	5 V Coil			DPDT

Notes:

1. Value can be adjusted to suit application.
2. Can be looser for relaxed ring-trip requirements.
3. Required for metering > 2.2 Vrms, otherwise may be omitted.
4. DT2i is optional - Should be put if there is a chance that this chip may be replaced by Am79R251.

ELECTRICAL CHARACTERISTICS

Power Dissipation

Loop resistance = 0 to ∞ unless otherwise noted (not including fuse resistors), 2 x 50 Ω fuse resistors, BATL = -36 V, BATH = -65 V, VCC = +5 V. For power dissipation measurements, DC-feed conditions are as follows:

- ILA (Active mode current limit) = 25 mA (IRSN = 50 μ A)
- RFD (Feed resistance) = 500 Ω
- VAS (Anti-sat activate voltage) = 10 V
- VAPP (Apparent Battery Voltage) = 48 V
- RTMG1 = RTMG2 (Thermal management resistors) = 1 k Ω

Description	Test Conditions	Min	Typ	Max	Unit
Power Dissipation Normal Polarity	On-Hook Disconnect		50		mW
	On-Hook Standby		65		
	On-Hook Transmission Fixed Longitudinal Voltage	ISLIC	145		
	On-Hook Active High Battery	ISLIC	270		
	Off-Hook Active Low Battery RL = 294 Ω	ISLIC TMG	620 200		
Power Supply Currents	On-Hook Disconnect	VBH	0.5		mA
		VBL VCC	0.1 3.1		
	On-Hook Standby	VBH VBL VCC	0.75 0 3.1		
	On-Hook Transmission Fixed Longitudinal Voltage	VBH VBL VCC	1.85 0 5		
	On-Hook Active High Battery	VBH VBL VCC	3.6 0 7.3		
	Off-Hook Active Low Battery RL = 294 Ω	VBH VBL VCC	.7 26.9 7.5		

Thermal Resistance

The junction to air thermal resistance of the Am79231 in a 32-pin, PLCC package is 45°C/W. The typical junction to case thermal resistance is 14°C/W. Measured under free air convection conditions and without external heatsinking.

Absolute Maximum Ratings

Storage temperature	-55 to +150°C
Ambient temperature, under bias	-40 to +85°C
Humidity	TBD
VCC with respect to GND	-0.4 to +7 V
VBH, VBL with respect to GND ²	+0.4 to -70 V
BGND with respect to GND	-3 to +3 V
Voltage on relay outputs	+7 V
AD or BD to BGND:	
Continuous	VBH - 1 to BGND + 1
10 ms (F = 0.1 Hz)	VBH - 5 to BGND + 5
1 μs (F = 0.1 Hz)	VBH - 10 to BGND + 10
250 ns (F = 0.1 Hz)	VBH - 15 to BGND + 15
Current into SA or SB: 10 μs rise to I _{peak} ; 1000 μs fall to 0.5 I _{peak} ; 2000 μs fall to I = 0	I _{peak} = ±5 mA
Current into SA or SB: 2 μs rise to I _{peak} ; 10 μs fall to 0.5 I _{peak} ; 20 μs fall to I = 0	I _{peak} = ±12.5 mA
SA SB continuous	5 mA
Current through AD or BD	± 150 mA
P1, P2, P3, LD to GND	-0.4 to VCC + 0.4 V
ESD Immunity (Human Body Model)	1500 V min
Maximum power dissipation, ¹ T _A = 70°C T _A = 85°C	1.67 W 1.33 W
Notes:	
1. Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature. Operation above 145°C junction temperature may degrade device reliability.	
2. Rise time of VBH (dv/dt) must be limited to less than 27 v/μs.	

Operating Ranges

Operating ranges define those limits between which device functionality is guaranteed. Functionality of the device from 0°C to 70°C is guaranteed by production testing. Performance from -40°C to 85°C is guaranteed by characterization and periodic sampling of production units.

Environmental Ranges

Ambient Temperature	0 to 70°C Commercial
	-40 to +85 °C extended temperature
Ambient Relative Humidity	15 to 85%

Electrical Maximum Ranges

VCC	5 V ± 5%
VBL	-(V _{loopmax} + 6V + V _{pk}) to VBH V
VBH	-42.5 V to -70 V
BGND with respect to GND	-100 mV to +100 mV
Load resistance on VTX to Vref	20 kΩ minimum
Load resistance on VSAB to Vref	20 kΩ minimum

Note:

V_{loopmax}: Maximum expected loop voltage in application; I_{LOOP} • maximum off-hook loop resistance.

V_{pk}: Peak signal voltage for application.

SPECIFICATIONS

Target Specifications (See note 1)

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Two-wire loop voltage (including offset)	Standby mode, open circuit, VBH < 55 V VBH > 55 V Any Active mode (does not include OHT), RL = 600 Ω, I _{RSN} = 50 μA OHT mode, RL = 600 Ω I _{RSN} = 20 μA	VBH – 8 48 13.88 8.64 19.8	VBH–7 51 15 10.8 22	VBH–6 55.5 16.13 12.96	V	3
2	Feed resistance per leg at pins AD & BD	Standby mode	130	250	375	Ω	
3	Feed current limit	Feed current Standby mode, RL = 600 Ω		34	45	mA	
	IMT current	Standby mode, RL = 2200 Ω	44.6	56			
	ILG current	Standby mode A to VBH B to Ground	36 43			μA	
4	Ternary input voltage boundaries for LD pin. Mid-level input source must be Vref.	Low boundary High boundary Input high current Input low current Mid-level current	CREF – 1	108 47 51	0.6	V V μA μA μA	— — — — 3
5	Logic Inputs P1, P2, P3	Input high voltage Input low voltage Input high current Input low current	2.0	10 50	0.8	V V μA μA	
6	VTX output offset		–50		+50	mV	
7	VREF input current	VREF = 1.4 V		.05		mA	3
8	CREF input current	CREF = 3.3 V		.09		mA	3
9	β, DC Ratio of VSAB to loop voltage: $\beta = \frac{V_{SAB}}{V_{SA} - V_{SB}}$	T _j < 145°C, VSA – VSB = 22 V	0.0088	0.0097	0.0106	V/V	
10	Fault Indicator Threshold	Voltage Output on IMT	TBD	CREF - 0.3 V	CREF	V	3
11	Gain from VLB pin to A or B pin			30		V/V	
12	VLB pin input current	VLB = VREF ±1 V		TBD		mA	
13	ILOOP/IMT	ILOOP = 10 mA	275	300	325	A/A	
14	ILONG/ILG	ILONG = 10 mA	560	600	640	A/A	
15	Input current, SA and SB pins	Active modes		1.0	3.0	μA	3
16	K1	Incremental DC current gain		500			
17	ISA/IMT	Disconnect, ISA = 2 mA		6		A/A	
18	ISB/ILG	Disconnect, ISB = 2 mA		12			
19	VSAB output offset			TBD		mV	
20	IMT output offset		-3	0	3	mV	
21	ILG output offset		-1	1	3	mV	

Relay Driver Specifications

Item	Condition	Min	Typ	Max	Unit	Note
On Voltage	25 mA/relay sink		0.4	0.5	V	3
	40 mA/ relay sink		0.8	1.0		3
R2,R3 Off Leakage	R2,R3 = BGND RYE = VBH	0		100	μ A	
Zener Break Over	I _z = 100 μ A	6.6	7.9		V	
Zener On Voltage	I _z = 30 mA		11		V	

Figure 4. Relay Driver Configuration

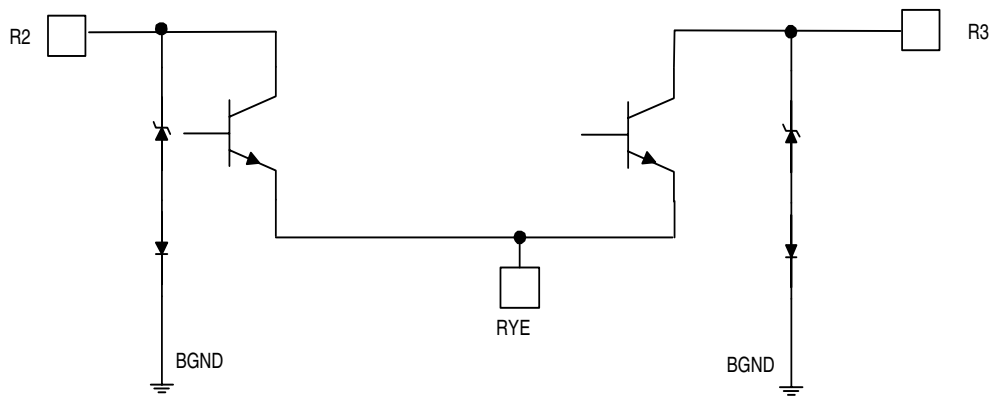
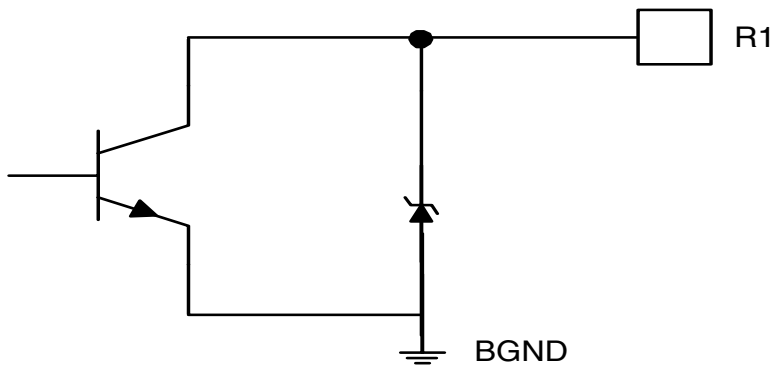


Figure 4A. Ring Relay Driver



Am79231 Transmission Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	RSN input impedance	f = 300 to 3400 Hz		1		Ω	3
2	VTX output impedance			3			
3	Max, AC + DC loop current	Active High Battery or Active Low Battery	70			mA	3
4	Input impedance, A or B to GND	Active mode		70	135	Ω	
5	2-4 wire gain	-10 dBm, 1 kHz, 0 to 70°C T _A = -40°C to 85°C	-14.13 -14.18	-13.98 -13.98	-13.83 -13.78	dB	
6	2-4 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz T _A = -40°C to 85°C	-0.1		+0.1		
7	2-4 wire gain tracking	+3 dBm to -55 dBm Reference: -10 dBm T _A = -40 to 85°C	-0.1	TBD	+0.1		6
8	4-2 wire gain	-10 dBm, 1 kHz T _A = -40°C to 85°C	-0.15	0 TBD	+0.15		
9	4-2 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz	-0.1		+0.1		
10	4-2 wire gain tracking	+3 dBm to -55 dBm Reference: -10 dBm	-0.1		+0.1		6
11	Total harmonic distortion level	300 Hz to 3400 Hz				dB	3
	2-wire	0 dBm			-50		
	4-wire	11.2 dBm			-40		
	4-wire overload level at VTX	-12 dBm -0.8 dBm RLOAD = 600 Ω			-48 -38		
12	Idle channel noise	Active modes				dBmC	3
	C-message	R _L = 600 Ω		+7	+11		
	Weighted	2-wire T _A = -40 to 85°C		TBD	-7	dBmp	3
	Psophometric	4-wire		-83	-79		
13	Longitudinal balance (IEEE method) Normal Polarity	L - T 200 to 1000 Hz	58	63		dB	
		T _A = -40°C to 0°C/70°C to 85°C	53				
		1000 to 3400 Hz	53	58			
		T _A = -40°C to 0°C/70°C to 85°C	48				
	T - L 200 to 3400 Hz	40					
Reverse Polarity	L - T 200 to 1000 Hz	50					
	T _A = -40°C to 0°C/70°C to 85°C	48					
14	PSRR (VBH, VBL)	50 to 3400 Hz	25	45			4, 5 2, 3, 5
		3.4 to 50 kHz		40			
15	PSRR (VCC)	50 to 3400 Hz	25	45			4, 5 2, 3, 5
		3.4 to 50 kHz		35			
16	Longitudinal AC current per wire	F = 15 to 60 Hz Active mode	20	30		mArms	3
17	Metering distortion	Freq = 12 kHz 2.8 Vrms Freq = 16 kHz metering load = 200 Ω	40			dB	3

Am79231 Current-Limit Behavior

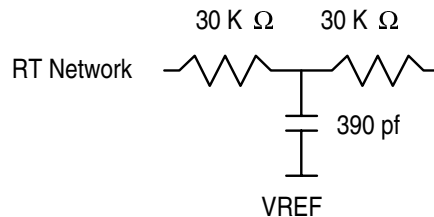
SLIC Mode	Condition	Min	Typ	Max	Unit	Note
Disconnect	Applied fault between ground and T/R VBH applied to Tip or Ring		1 VBH/200 k Ω	100	μ A A	7
Tip Open	Ring Short to GND	32	34	37	mA	
Standby	Short Tip-to-VBH Short Ring-to-GND	24 26	38 35	47 44		

Am79231 Fault Indications

Fault	Indication	Unit	Note
No Fault	IMT operates normally ($V_{ref} \pm 1V$)		
Thermal Shutdown	IMT above 2.8 V; ILG operates normally		

Notes:

- Unless otherwise specified, test conditions are: $V_{CC} = 5 V$, $RMG1 = RMG2 = 1 k\Omega$, $BATH = -65 V$, $BATL = 36 V$, $VBL = 34$, $RRX = 150 k\Omega$, $RL = 600 \Omega$, $RSA = RSB = 200 k\Omega$, $RFA = RFB = 50 \Omega$, $CHP = 22 nF$, $CAD = CBD = 22 nF$, $IRSN = 84 \mu A$. DC-feed conditions are normally set by the ISLAC device. When the Am79231 is tested by itself, its operating conditions must be simulated as if it were connected to an ideal ISLAC device.



- These tests are performed with the following load impedances:
Frequency < 12 kHz – Longitudinal impedance = 500 Ω ; metallic impedance = 300 Ω
Frequency > 12 kHz – Longitudinal impedance = 90 Ω ; metallic impedance = 135 Ω
- Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.
- This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
- When the Am79231 and ISLAC device is in the anti-sat operating region, this parameter is degraded. The exact degradation depends on system design.
- 55 dBm gain tracking level not tested in production. This parameter is guaranteed by characterization and correlation to other tests.
- This spec is valid from 0 V to VBL or -50 V, whichever is lower in magnitude.

Operating Modes

The Am79231 receives multiplexed control data on the P1, P2 and P3 pins. The LD pin then controls the loading of P1, P2, and P3 values into the proper bits in the Am79231 control register. When the LD pin is less than 0.3 V below VREF ($< (VREF - 0.3 V)$), P1–P3 must contain data for relay control bits RD1, RD2 and RD3. These are latched into the first three bits in the Am79231 control register. When the LD pin is more than 0.3 V above VREF ($> (VREF + 0.3 V)$), P1–P3 must contain ISLIC control data C1, C2, and C3, which are latched into the last three bits of the Am79231 control register. Connecting the LD pin to VREF locks the contents of the Am79231 control register.

The operating mode of the Am79231 is determined by the C1, C2, and C3 bits in the control register of the Am79231. Table 1 defines the Am79231 operating modes set by these signals.

Under normal operating conditions, the ISLIC device does not have active relays. The Am79231 to ISLAC device interface is designed to allow continuous real-time control of the relay drivers to avoid incorrect data loads to the relay bit latches of the Am79231 devices.

To perform external ringing, the ISLAC device from the Intelligent Access voice family is set to external ringing mode (RMODE = 1), enables the ring relay, and puts the Am79231 in the Standby mode.

Table 1. Operating Modes

C3	C2	C1	Operating Mode	Battery Voltage Selection	Operating Mode	Connection to RMGPi & RMGLi Resistors
0	0	0	Standby ¹	High Battery (BATH) and BGND	(High ohmic feed): Loop supervision active, A and B amplifiers shut down	Open
0	0	1	Tip Open ¹	High Battery (BATH) and BGND	Tip Open: AD at High-Impedance, Channel A power amplifier shut down	Open
0	1	0	On-Hook Transmission, Fixed Longitudinal Voltage	High Battery (BATH) and BGND	Fixed longitudinal voltage of –30 V	A and B Amplifier Output
0	1	1	Disconnect	Low Battery selection at VBL	AD and BD at High-Impedance, Channel A and B power amplifiers shut down	
1	0	0	RSVD		Active feed, normal or reverse polarity	
1	0	1	Active High Battery	High Battery (BATH) and BGND		
1	1	0	Active Low Battery	Low Battery (BATL) and BGND		
1	1	1	RSVD			

Note:

1. In these modes, the ring lead (B-lead) output has a –50 V internal clamp to battery ground (BGND).

Table 2. Mode Descriptions

Operating Mode	Description
Disconnect	This mode disconnects both A and B output amplifiers from the AD and BD outputs. The A and B amplifiers are shut down and the Am79231 selects the low battery voltage at the VBL pin. In the Disconnect state, the currents on IMT and ILG represent the voltages on the SA and SB pins, respectively. These currents are scaled to produce voltages across RMTi and RLGi of $\frac{V_{SA}}{400}$ and $\frac{V_{SB}}{400}$, respectively.
Standby	The power amplifiers are turned off. The AD output is driven by an internal 250 Ω (typical) resistor, which connects to ground. The BD output is driven by an internal 250 Ω (typical) resistor, which connects to the high battery (BATH) at the VBH pin, through a clamp circuit, which clamps at -50 V with respect to BGND. For VBH values above -55 V, the open-circuit voltage, which appears at this output is $\sim VBH + 5$ V. If VBH is below -55 V, the voltage at this output is -50 V. The battery selection for the balance of the circuitry on the chip is VBL. Line supervision remains active. Current limiting is provided on each line to limit power dissipation under short-loop conditions as specified in the "Am79231 Current-Limit Behavior" section. In external ringing, the standby ISLIC state is selected.
Tip Open	In this mode, the AD (Tip) lead is opened and the BD (Ring) lead is connected to a clamp, which operates from the high battery on VBH pin and clamps to approximately -50 V with respect to BGND through a resistor of approximately 250 Ω (typical). The battery selection for the balance of the circuitry on the chip is VBL. To prevent excessive power dissipation, the current in the Ring lead is limited by an internal current source to 30 mA.
Active High Battery	In the Active High Battery mode, battery connections are as shown in Table 1. Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. Active High Battery mode is enabled during a call in applications when a long loop can be encountered.
Active Low Battery	Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. VBL, the low negative battery, is selected in the Active Low Battery mode. This is typically used during the voice part of a call.
On-Hook Transmission (OHT), Fixed Longitudinal Voltage	In the On-Hook Transmission, Fixed Longitudinal Voltage mode, battery connections are as shown in Table 1. The longitudinal voltage is fixed at -30 V to allow compliance with safety specifications for some classes of products.

Control bits RD1, RD2, and RD3 do not affect the operating mode of the Am79231. These signals usually perform the following functions.

Table 3. Driver Descriptions

Driver	Description
R1	A logic 1 on RD1 turns the R1 driver on and operates a relay connected between the R1 pin and VCCD. R1 drives the ring relay.
R2	A logic 1 on the RD2 signal turns the R2 driver on and routes current from the R2 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R2 pin can sink current from a relay connected to VCCD. Another option is to connect the RYE pin to the BD (Ring) lead through a diode and connect a test load between R2 and the AD (Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the linecard. The test load must be connected to the Am79231 side of the protection resistor to avoid damage to the R2 driver.

Driver	Description
R3	<p>A logic 1 on the RD3 signal turns the R3 driver on and routes current from the R3 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R3 pin can sink current from a relay connected to VCCD.</p> <p>Another option is to connect the RYE pin to the B (Ring) lead through a diode and connect a test load between R3 and the A (Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the linecard. The test load must be connected to the Am79231 side of the protection resistor to avoid damage to the R3 driver.</p>

Thermal-Management Equations (All Modes except Standby)

$I_L < 5 \text{ mA}$ $P_{SLIC} = (S_{BAT} - I_{LRL}) \cdot I_L + 0.3 \text{ W}$ $P_{TMG} = 0$	TMG resistor-current is limited to be $5 \text{ mA} < I_L$. If $I_L < 5 \text{ mA}$, no current flows in the TMG resistor and it all flows in the Am79231.
$I_L > 5 \text{ mA}$ $P_{SLIC} = (S_{BAT} - I_L(R_L + 2 \cdot R_{FUSE})) \cdot I_L + 0.3 \text{ W} - P_{TMG}$ $P_{TMG} = (I_L - 5 \text{ mA})^2 \cdot (R_{TMG1} + R_{TMG2})$	These equations are valid when $R_{TMGX} \cdot (I_L - 5 \text{ mA}) < (S_{BAT} - R_L I_L) / 2 - 2$ because the longitudinal voltage is one-half the battery voltage and the TMG switches require approximately 2 V.

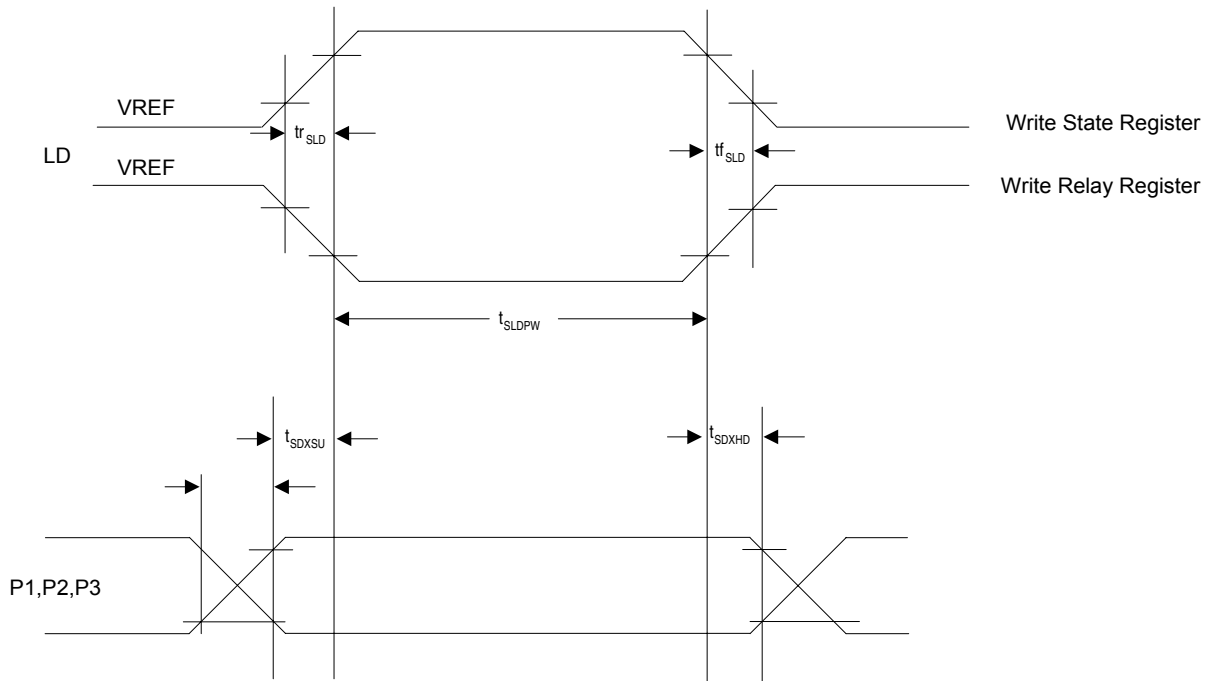
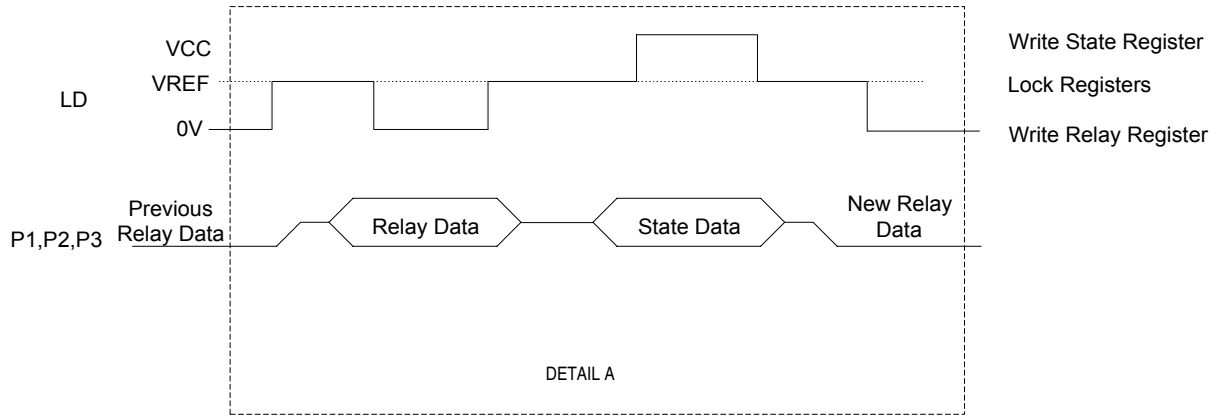
TIMING SPECIFICATIONS

Symbol	Signal	Parameter	Min	Typ	Max	Unit
trSLD	LD	Rise time Am79231 LD pin			2	μs
tfSLD	LD	Fall time Am79231 LD pin			2	
tSLDPW	LD	LD minimum pulse width	3			
tSDXSU	P1,P2,P3	P1–3 data Setup time	4.5			
tSDXHD	P1,P2,P3	P1–3 data hold time	4.5			
tSDXD	P1,P2,P3	Max P1–3 data delay			5	

Notes:

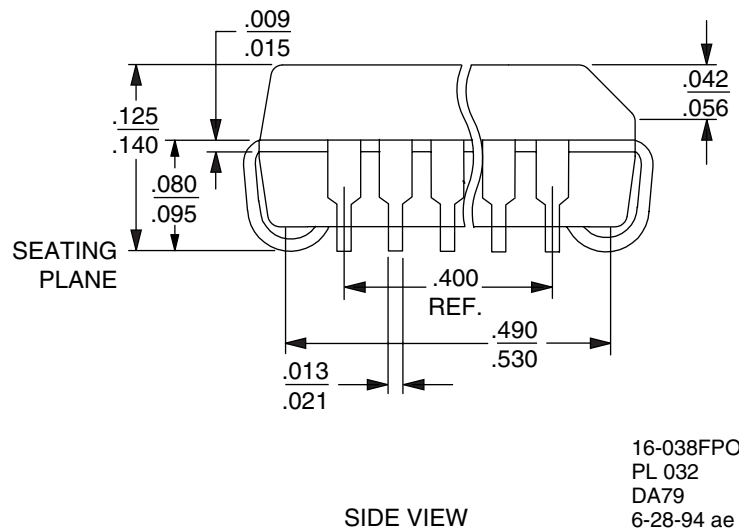
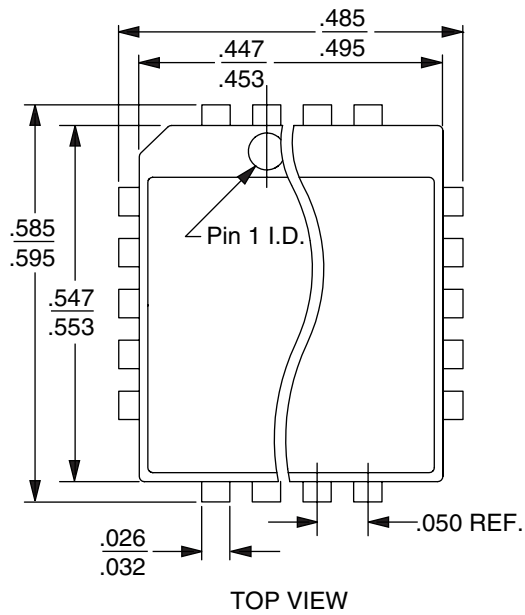
- The P1–3 pins are updated continuously during operation by the LD signal.
- After a power-on reset or hardware reset, the relay outputs from the Am79231 turn all relays off. An unassuming state is to place the relay control pins, which are level triggered, to a reset state for all relays. Any noise encountered only raises the levels toward the register lock state.
- When writing to the ISLIC registers, the sequence is:
 - Set LD pin to mid-state
 - Place appropriate data on the P1–3 pins
 - Assert the LD pin to High or Low to write the proper data
 - Return LD pin to mid-state
- Am79231 registers are refreshed at 5.33 kHz when used with an ISLAC device.
- If the clock or MPI becomes disabled, the LD pins and P1–3 returns to 0 V state, thus protecting the Am79231 and the line connection.
- Not tested in production. Guaranteed by characterization.

WAVEFORMS



PHYSICAL DIMENSIONS

PL032



REVISION SUMMARY

Revision A to Revision B

- Revision A was a condensed version of the datasheet while Revision B contained the full version.

Revision B to Revision C

- Page 12, Linecard Parts List, Rows CHLbi and CHLdi: switched the numbers in the "Values" column.

Notes:

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Notes:

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