# Am79C873

**AMD**

**NetPHY™ -1**
**10/100 Mbps Ethernet Physical Layer Single-Chip Transceiver with 100BASE-FX Support**

## DISTINCTIVE CHARACTERISTICS

- 100BASE-FX direct interface to industry standard electrical/optical transceivers
- 10/100BASE-TX physical-layer, single-chip transceiver
- Compliant with the IEEE 802.3u 100BASE-TX standard
- Compliant with the ANSI X3T12 TP-PMD 1995 standard
- Compliant with the IEEE 802.3u Auto-Negotiation protocol for automatic link type selection
- Supports the MII with serial management interface
- Supports Full Duplex operation for 10 Mbps and 100 Mbps

- High performance 100 Mbps clock generator and data recovery circuitry
- Adaptive equalization circuitry for 100 Mbps receiver
- Controlled output edge rates in 100 Mbps
- Supports a 10BASE-T interface without the need for an external filter
- Provides Loopback mode for system diagnostics
- Includes flexible LED configuration capability
- Digital clock recovery circuit using advanced digital algorithm to reduce jitter
- Low-power, high-performance CMOS process
- Available in a 100-pin PQFP package

## GENERAL DESCRIPTION

The NetPHY-1 device is a physical-layer, single-chip, low-power transceiver for 100BASE-TX, 100BASE-FX, and 10BASE-T operations. On the media side, it provides a direct interface to Fiber Media for 100BASE-FX Fast Ethernet, Unshielded Twisted Pair Category 5 Cable (UTP5) for 100BASE-TX Fast Ethernet, or UTP5/UTP3 Cable for 10BASE-T Ethernet. Through the IEEE 802.3u Media Independent Interface (MII), the NetPHY-1 device connects to the Medium Access Control (MAC) layer, ensuring a high interoperability among products from different vendors.

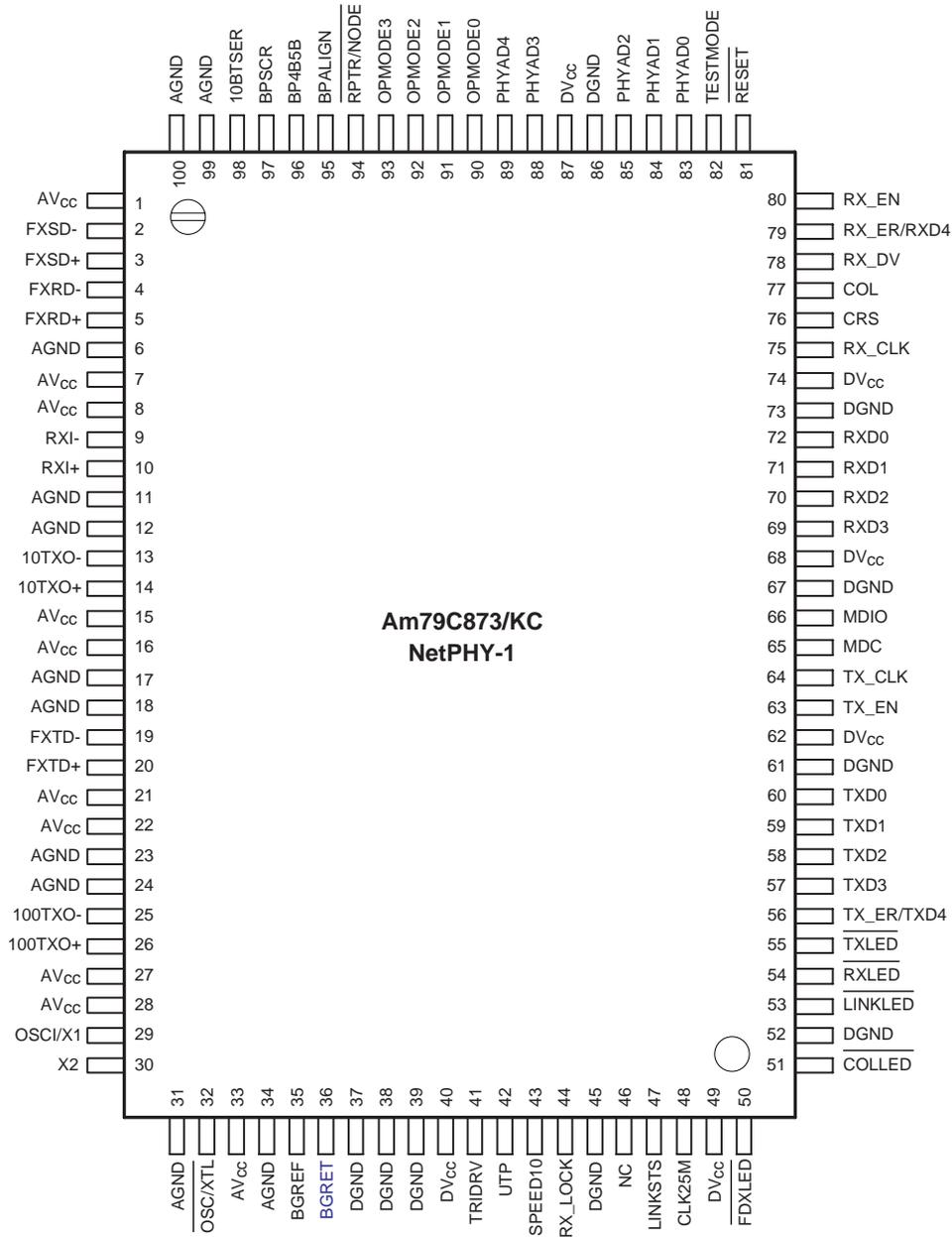The NetPHY-1 device uses a low-power, high-performance CMOS process. It contains the entire physical layer functions of 100BASE-FX and 100BASE-TX as defined by the IEEE 802.3u standard, including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), 100BASE-TX Twisted Pair Physical Medium Dependent (TP-PMD) sublayer, and a 10BASE-T Encoder/Decoder (ENDEC). The NetPHY-1 device provides strong support for the Auto-Negotiation function utilizing automatic media speed and protocol selection. The NetPHY-1 device incorporates an internal wave-shaping filter to control rise/fall time, eliminating the need for external filtering on the 10/100 Mbps signals.

## BLOCK DIAGRAM
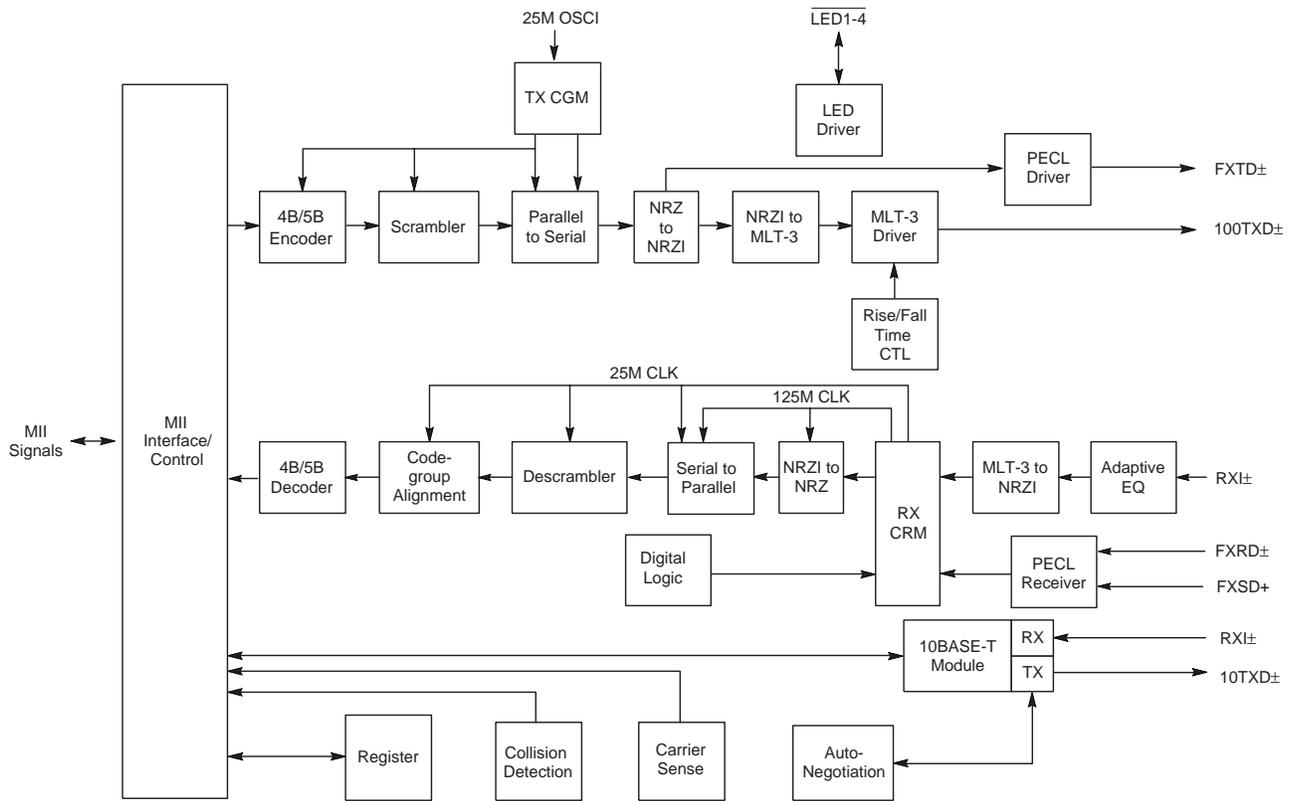


22164A-1

## CONNECTION DIAGRAM
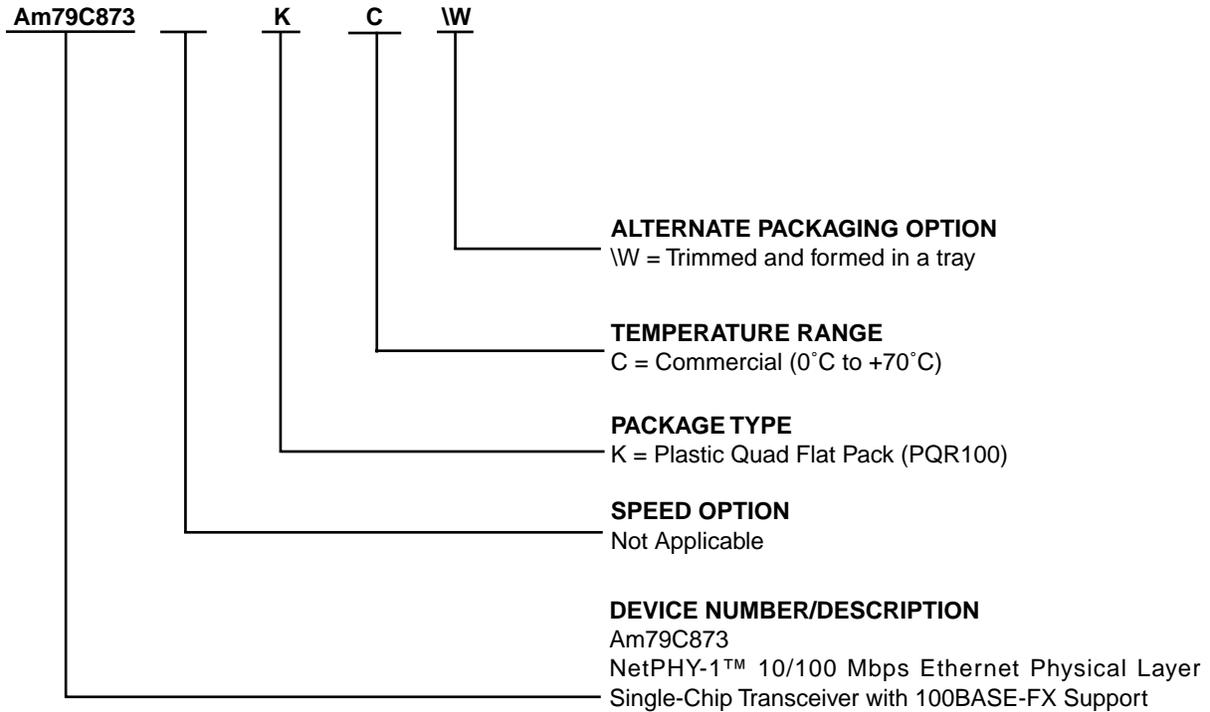
```
                                                                    RPTR/NODE
                                                                    OPMODE3
                                                                    OPMODE2
                                                                    OPMODE1
                                                                    OPMODE0
                                  10BTSER                           PHYAD4
                                  BPSCR                             PHYAD3
                         AGND     BP4B5B                            DVcc
                         AGND     BPALIGN                  DGND     PHYAD2
                                                                    PHYAD1
                                                                    PHYAD0
                                                                    TESTMODE
                                                                    RESET

            AVcc      1                                        80   RX_EN
            FXSD-     2                                        79   RX_ER/RXD4
            FXSD+     3                                        78   RX_DV
            FXRD-     4                                        77   COL
            FXRD+     5                                        76   CRS
            AGND      6                                        75   RX_CLK
            AVcc      7                                        74   DVcc
            AVcc      8                                        73   DGND
            RXI-      9                                        72   RXD0
            RXI+     10                                        71   RXD1
            AGND     11                                        70   RXD2
            AGND     12                                        69   RXD3
            10TXO-   13                                        68   DVcc
            10TXO+   14                Am79C873/KC             67   DGND
            AVcc     15                  NetPHY-1              66   MDIO
            AVcc     16                                        65   MDC
            AGND     17                                        64   TX_CLK
            AGND     18                                        63   TX_EN
            FXTD-    19                                        62   DVcc
            FXTD+    20                                        61   DGND
            AVcc     21                                        60   TXD0
            AVcc     22                                        59   TXD1
            AGND     23                                        58   TXD2
            AGND     24                                        57   TXD3
            100TXO-  25                                        56   TX_ER/TXD4
            100TXO+  26                                        55   TXLED
            AVcc     27                                        54   RXLED
            AVcc     28                                        53   LINKLED
            OSCI/X1  29                                        52   DGND
            X2       30                                        51   COLLED
```

Pin labels (bottom, 31–50): AGND, OSC/XTL, AVcc, AGND, BGREF, BGRET, DGND, DGND, DGND, DVcc, TRIDRV, UTP, SPEED10, RX_LOCK, DGND, NC, LINKSTS, CLK25M, DVcc, FDXLED

22164A-2

## ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am79C873      K    C    \W

**ALTERNATE PACKAGING OPTION**
\W = Trimmed and formed in a tray

**TEMPERATURE RANGE**
C = Commercial (0˚C to +70˚C)

**PACKAGE TYPE**
K = Plastic Quad Flat Pack (PQR100)

**SPEED OPTION**
Not Applicable

**DEVICE NUMBER/DESCRIPTION**
Am79C873
NetPHY-1™ 10/100 Mbps Ethernet Physical Layer
Single-Chip Transceiver with 100BASE-FX Support

| Valid Combinations | |
|---|---|
| Am79C873 | KC\W |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

# RELATED AMD PRODUCTS

| Part No. | Description |
|---|---|
| **Controllers** | |
| Am79C90 | CMOS Local Area Network Controller for Ethernet (C-LANCE™) |
| **Integrated Controllers** | |
| Am79C930 | PCnet™-Mobile Single Chip Wireless LAN Media Access Controller |
| Am79C940 | Media Access Controller for Ethernet (MACE™) |
| Am79C961A | PCnet-ISA II Full Duplex Single-Chip Ethernet Controller for ISA Bus |
| Am79C965A | PCnet-32 Single-Chip 32-Bit Ethernet Controller for 486 and VL Buses |
| Am79C970A | PCnet-PCI II Full Duplex Single-Chip Ethernet Controller for PCI Local Bus |
| Am79C971 | PCnet-FAST Single-Chip Full Duplex 10/100 Mbps Ethernet Controller for PCI Local Bus |
| Am79C972 | PCnet-FAST+ Enhanced 10/100 Mbps PCI Ethernet Controller with OnNow Support |
| Am79C973/ Am79C975 | PCnet-Fast III Single-chip 10/100 Mbps PCI Ethernet Controller With Integrated PHY |
| Am79C978 | PCnet-Home Single-chip 1/10 Mbps PCI Home networking Controller |
| **Physical Layer Devices (Single-Port)** | |
| Am7996 | IEEE 802.3/Ethernet/Cheapernet Transceiver |
| Am79761 | Physical Layer 10-Bit Transceiver for Gigabit Ethernet (GigaPHY™-SD) |
| Am79C98 | Twisted Pair Ethernet Transceiver (TPEX) |
| Am79C100 | Twisted Pair Ethernet Transceiver Plus (TPEX+) |
| **Physical Layer Devices (Multi-Port)** | |
| Am79C871 | Quad Fast Ethernet Transceiver for 100BASE-X Repeaters (QFEXr™) |
| Am79C988A | Quad Integrated Ethernet Transceiver (QuIET™) |
| Am79C989 | Quad Ethernet Switching Transceiver (QuEST™) |
| **Integrated Repeater/Hub Devices** | |
| Am79C981 | Integrated Multiport Repeater Plus (IMR+) |
| Am79C982 | Basic Integrated Multiport Repeater (bIMR) |
| Am79C983 | Integrated Multiport Repeater 2 (IMR2™) |
| Am79C984A | Enhanced Integrated Multiport Repeater (eIMR™) |
| Am79C985 | Enhanced Integrated Multiport Repeater Plus (eIMR+™) |
| Am79C987 | Hardware Implemented Management Information Base (HIMIB™) |

## CONTENTS

# PIN DESCRIPTIONS

## MII Interface

### TX_ER/TXD4

**Transmit Error**                     **Input**

In 100 Mbps mode, if this signal is asserted high and TX_EN is active, the HALT symbol is substituted for the actual data nibble. In 10 Mbps mode, this input is ignored.

In bypass modes (BP4B5B or BPALIGN), TX_ER becomes the TXD4 pin, the fifth TXD data bit.

### TXD[3:0]

**Transmit Data**                     **Input**

These are the transmit data input pins for nibble data from the MII in 100 Mbps or 10 Mbps nibble mode (25 MHz for 100 Mbps mode, 2.5 MHz for 10 Mbps nibble mode).

In 10 Mbps serial mode, the TXD0 pin is used as the serial data input pin. TXD[3:1] are ignored.

### TX_EN

**Transmit Enable**                     **Input**

Active high input indicates the presence of valid nibble data on TXD[3:0] for both 100 Mbps or 10 Mbps nibble mode.

In 10 Mbps serial mode, active high indicates the presence of valid 10 Mbps data on TXD0.

### TX_CLK

**Transmit Clock**                     **Output/Z[1]**

This pin provides the transmit clock output from the NetPHY-1 deviceas follows:

- 25 MHz nibble transmit clock derived from transmit Phase Locked Loop (TX PLL) in 100BASE-TX mode

- 2.5 MHz transmit clock in 10BASE-T nibble mode

- 10 MHz transmit clock in 10BASE-T serial mode

### MDC

**Management Data Clock**                     **Input**

This pin is the synchronous clock to the MDIO management data input/output serial interface which is asynchronous to transmit and receive clocks. The maximum clock rate is 2.5 MHz.

### MDIO

**Management Data I/O**                     **Input/Output**

This pin is the bidirectional management instruction/data signal that may be driven by the station management entity or the PHY. This pin requires a 1.5 KΩ pull-up resistor.

### RXD[3:0]

**Receive Data**                     **Output/Z[1]**

Nibble wide receive data (synchronous to RX_CLK - 25 MHz for 100BASE-TX mode, 2.5 MHz for 10BASE-T nibble mode). Data is driven on the falling edge of RX_CLK.

In 10 Mbps serial mode, the RXD0 pin is used as the data output pin. RXD[3:1] are ignored.

### RX_CLK

**Receive Clock**                     **Output/Z[1]**

Provides the recovered receive clock for different modes of operation:

- 25 MHz nibble clock in 100 Mbps mode

- 2.5 MHz nibble clock in 10 Mbps nibble mode

- 10 MHz receive clock in 10 Mbps serial mode

### CRS

**Carrier Sense**                     **Output/Z[1]**

This pin is asserted high to indicate the presence of carrier due to receive or transmit activities in 10BASE-T or 100BASE-TX Half Duplex modes.

In Repeater, when Full Duplex or Loopback mode is a logic 1, it indicates the presence of carrier due only to receive activity.

### COL

**Collision Detect**                     **Output/Z[1]**

This pin is asserted high to indicate detection of collision conditions in 10 Mbps and 100 Mbps Half Duplex modes. In 10BASE-T Half Duplex mode with Heartbeat set active (bit 13, register 18h), it is also asserted for a duration of approximately 1ms at the end of transmission to indicate heartbeat. In Full Duplex mode, this signal is always logic 0. There is no heartbeat function in Full Duplex mode.

### RX_DV

**Receive Data Valid**                     **Output/Z[1]**

This pin is asserted high to indicate that valid data is present on RXD[3:0].

### RX_ER/RXD4

**Receive Error**                     **Output/Z[1]**

This pin is asserted high to indicate that an invalid symbol has been detected inside a received packet in 100 Mbps mode.

In a bypass mode (BP4B5B or BPALIGN modes), RX_ER becomes RXD4, the fifth RXD data bit of the 5B symbols.

---

1. Goes to high impedance.

---

## RX_EN

**Receive Enable**                    **Input**

This pin is active high enabled for receive signals RXD[3:0], RX_CLK, RX_DV and RX_ER. A low on this input tri-states these output pins. For normal operation in a NODE application, this pin should be pulled high.

## Media Interface

### RXI±

**100/10 Mbps-TX/T Twisted Pair Differential Input Pair**                    **Input**

These pins are the differential receive input for 10BASE-T and 100BASE-TX. They are capable of receiving 100BASE-TX MLT-3 or 10BASE-T Manchester encoded data.

### FXRD±

**100BASE-FX PECL Differential Input Pair**    **Input**

These pins are the differential receive input for 100BASE-FX. They are capable of receiving 100BASE-FX.

### FXSD±

**100BASE-FX PECL Signal Detect**        **Input**

These input signals from the FX-PMD transceiver indicate detection of a receive signal from the Fiber Media.

### 10TXO±

**10BASE-T Differential Output Pair**        **Output**

This output pair provides controlled rise and fall times designed to filter the transmitters output.

### 100TXO±

**100BASE-TX Twisted Pair Differential Output Pair**
                    **Output**

This output pair drives MLT-3 encoded data to the 100 M twisted pair cable and provides controlled rise and fall times designed to filter the transmitters output, reducing any associated EMI.

### FXTD±

**100BASE-FX PECL Differential Output Pair Output**

These pins are the differential transmit output for 100BASE-FX. They are capable of transmitting 100BASE-FX

## LED Interface

These outputs can directly drive LEDs or provide status information to a network management device.

### $\overline{\text{FDXLED}}$ (POLLED)

**Polarity/Full Duplex LED**            **Output**

This pin indicates Full Duplex mode status for 100 Mbps and 10 Mbps operation (Active low). If bit 4 of Register 16 (FDXLED_MODE) is set, the $\overline{\text{FDXLED}}$ pin

function will change to indicate the Polarity status for 10 Mbps operation. If polarity is inverted, the POLLED will go ON.

### $\overline{\text{COLLED}}$

**Collision LED**                    **Output**

This pin indicates the presence of collision activity for 10 Mbps and 100 Mbps operation. This LED has no meaning for 10 Mbps or 100 Mbps Full Duplex operation (Active low).

### $\overline{\text{LINKLED}}$ (TRAFFIC LED)

**Link LED**                        **Output**

This pin indicates Good Link status for 10 Mbps and 100 Mbps operation (Active low). It functions as the TRAFFIC LED when bit 5 of register 16 is set to 1. In TRAFFIC LED mode, it is always ON when the link is OK. The TRAFFIC LED flashes when transmitting or receiving.

### $\overline{\text{RXLED}}$

**Receive LED**                    **Output Drain**

This pin indicates the presence of receive activity for 10 Mbps and 100 Mbps operation (Active low). The Net-PHY-1 device incorporates a "monostable" function on the RXLED output. This ensures that even minimal receive activity will generate an adequate LED ON time.

### $\overline{\text{TXLED}}$

**Transmit LED**                    **Output Drain**

This pin indicates the presence of transmit activity for 10 Mbps and 100 Mbps operation (Active low). The Net-PHY-1 device incorporates a "monostable" function on the TXLED output. This ensures that even minimal transmit activity will generate an adequate LED ON time.

## Device Configuration/Control/Status Interface

### UTP

**UTP Cable Indication**                **Output**

This pin is the UTP Cable Indication. When UTP=1, it indicates that the UTP cable is being used.

### SPEED10

**Speed 10 Mbps**                    **Output**

When set high, this bit indicates a 10 Mbps operation, when set low 100 Mbps operation. This pin can drive a low current LED to indicate that 100 Mbps operation is selected.

### RX_LOCK

**Lock for Clock/Data Recovery PLL**        **Output**

When this pin is high, it indicates that the receiver recovery PLL logic has locked to the input data stream.

## LNKSTS

**Link Status Register Bit**                    **Output**

This pin reflects the status of bit 2 register 1.

## OPMODE0-OPMODE3

**OPMODE0-OPMODE3**                    **Input**

These pins are used to control the forced or advertised operating mode of the NetPHY-1 device (see table below). The value is latched into the NetPHY-1 device registers at power-up/rese..

| OP-MODE3 | OP-MODE2 | OP-MODE1 | OP-MODE0 | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Auto-Negotiation enable with all capabilities with Flow Control |
| 0 | 0 | 0 | 1 | Auto-Negotiation enable without all capabilities without Flow Control |
| 0 | 0 | 1 | 0 | Auto-Negotiation 100TX FDX with Flow Control only |
| 0 | 0 | 1 | 1 | Auto-Negotiation 100TX FDX/HDX without Flow Control |
| 0 | 1 | 0 | 0 | Auto-Negotiation 10TP FDX with Flow Control only |
| 0 | 1 | 0 | 1 | Auto-Negotiation 10TX FDX/HDX without Flow Control |
| 0 | 1 | 1 | 0 | Manual select 100TX FDX |
| 0 | 1 | 1 | 1 | Manual select 100TX HDX |
| 1 | 0 | 0 | 0 | Manual select 10TX FDX |
| 1 | 0 | 0 | 1 | Manual select 10TX HDX |
| 1 | 0 | 1 | 0 | Manual select 100FX FDX |
| 1 | 0 | 1 | 1 | Manual select 100FX HDX |
| 1 | 1 | 1 | 1 | Auto-Negotiation 10/100TX. HDX only |

## RTPR/NODE

**Repeater/Node Mode**                    **Input**

When set high, this bit selects REPEATER mode; when set low, it selects NODE. In REPEATER mode or NODE mode with Full Duplex configured, the Carrier Sense (CRS) output from the NetPHY-1 device will be asserted only during receive activity. In NODE mode or a mode not configured for Full Duplex operation, CRS will be asserted during receive or transmit activity. At power-up/reset, the value on this pin is latched into Register 16, bit 11.

## BPALIGN

**Bypass Alignment**                    **Input**

This pin allows 100 Mbps transmit and receive data streams to bypass all of the transmit and receive operations when set high. At power-up/reset, the value on this pin is latched into bit Register 16, bit 13.

## BP4B5B

**Bypass 4B5B Encoder/Decoder**                    **Input**

This pin allows 100 Mbps transmit and receive data streams to bypass the 4B to 5B encoder and 5B to 4B decoder circuits when set high. At power-up/reset, the value on this pin is latched into Register 16, bit 15.

## BPSCR

**Bypass Scrambler/Descrambler**                    **Input**

This pin allows 100 Mbps transmit and receive data streams to bypass the scrambler and descrambler circuits when set high. At power-up/reset, the value on this pin is latched into Register 16, bit 14.

## 10BTSER

**Serial/Nibble Select**                    **Input**

10 Mbps Serial Operation:

When set high, this input selects a serial data transfer mode. Manchester encoded transmit and receive data is exchanged serially with a 10 MHz clock rate on the least significant bits of the nibble-wide MII data buses, pin TXD[0] and RXD[0] respectively. This mode is intended for use with the NetPHY-1 device connected to a device (MAC or Repeater) that has a 10 Mbps serial interface. Serial operation is not supported in 100 Mbps mode. For 100 Mbps, this input is ignored.

10 and 100 Mbps Nibble Operation:

When set low, this input selects the MII compliant nibble data transfer mode. Transmit and receive data is exchanged in nibbles on the TXD[3:0] and RXD[3:0] pins respectively.

At power-up/reset, the value on this pin is latched into Register 18, bit 10.

## Clock Interface

### OSCI/X1

**Crystal or Oscillator Input**                  **Input**

This pin should be connected to a 25 MHz (±50 ppm) crystal if $\overline{OSC/XTL}$=0 or a 25 MHz (±50 ppm) external TTL oscillator input, if $\overline{OSC/XTLB}$=1.

### X2

**Crystal Oscillator Output**                  **Output**

An external 25 MHz (±50 ppm) crystal should be connected to this pin if $\overline{OSC/XTL}$=0, or left unconnected if $\overline{OSC/XTL}$=1.

### $\overline{OSC/XTL}$

**Crystal or Oscillator Selector Pin**          **Output**

$\overline{OSC/XTL}$=0: An external 25 MHz (±50ppm) crystal should be connected to X1 and X2 pins.

■ $\overline{OSC/XTL}$=1: An external 25 MHz (±50ppm) oscillator should be connected to X1 and X2 should be left unconnected.

### CLK25M

**25 MHz Clock Output**                       **Output/Z**

This clock is derived directly from the crystal circuit.

## PHY Address Interface

The PHYAD[4:0] pins provide up to 32 unique PHY addresses. An address selection of all zeros (00000) will result in a PHY isolation condition. See the isolate bit description in the BMCR, address 00.

### PHYAD0

**PHY Address 0**                             **Input**

This pin provides PHY address bit 0 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 8 during power up/reset.

### PHYAD1

**PHY Address 1**                             **Input**

This pin provides PHY address bit 1 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 7 during power up/reset.

### PHYAD2

**PHY Address 2**                             **Input**

This pin provides PHY address bit 2 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 6 during power up/reset.

### PHYAD3

**PHY Address 3**                             **Input**

This pin provides PHY address bit 3 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 5 during power up/reset.

### PHYAD4

**PHY Address 4**                             **Input**

This pin provides PHY address bit 4 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 4 during power up/reset.

## Miscellaneous

### NC

**No Connect**

These pins are to be left unconnected (floating).

### BGREF

**Bandgap Voltage Reference**                 **Input**

Connect a 6.01K $\Omega$, 1% resistor between this pin and the BGRET pin to provide an accurate current reference for the NetPHY-1 device.

### BGRET

**Bandgap Voltage Reference Return**          **Input**

This is the return pin for 6.01K $\Omega$ resistor connection.

### TRIDRV

**Tri-State Digital Output**                   **Input**

When set high, all digital output pins are set to a high impedance state, and I/O pins, go to input mode.

### $\overline{RESET}$

**Reset**                                     **Input**

This pin is the active low input that initializes the NetPHY-1 device. It should remain low for 30 ms after VCC has stabilized at 5 Vdc (nominal) before it transitions high.

### TESTMODE

**Test Mode Control Pin**                      **Input**

TESTMODE=0: Normal operating mode.

TESTMODE=1: Enable test mode.

## Power and Ground Pins

The power (VCC) and ground (GND) pins of the NetPHY-1 device are grouped in pairs of two categories - Digital Circuitry Power/Ground Pairs and Analog Circuitry Power/Ground Pair.

### DGND

**Digital Logic Ground**                       **Power**

These pins are the digital supply pairs.

### DVCC

**Digital Logic Power Supply**                 **Power**

These pins are the digital supply pairs.

### AGND

**Analog Circuit Ground**                      **Power**

These pins are the analog circuit supply pairs.

### AVCC

**Analog Circuit Power Supply**                **Power**

These pins are the analog circuit supply pairs.

# FUNCTIONAL DESCRIPTION

The NetPHY-1 Fast Ethernet single-chip transceiver, provides the functionality as specified in the IEEE 802.3u standard, integrates complete 100BASE-FX, 100BASE-TX modules and a complete 10BASE-T module. The NetPHY-1 device provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

The NetPHY-1 device performs all Physical Coding Sublayer (PCS), Physical Media Access (PMA), Twisted Pair Physical Medium Dependent (TP-PMD) sublayer, 10BASE-T Encoder/Decoder, and Twisted Pair Media Access Unit (TPMAU) functions. Figure 1 shows the major functional blocks implemented in the NetPHY-1 device.
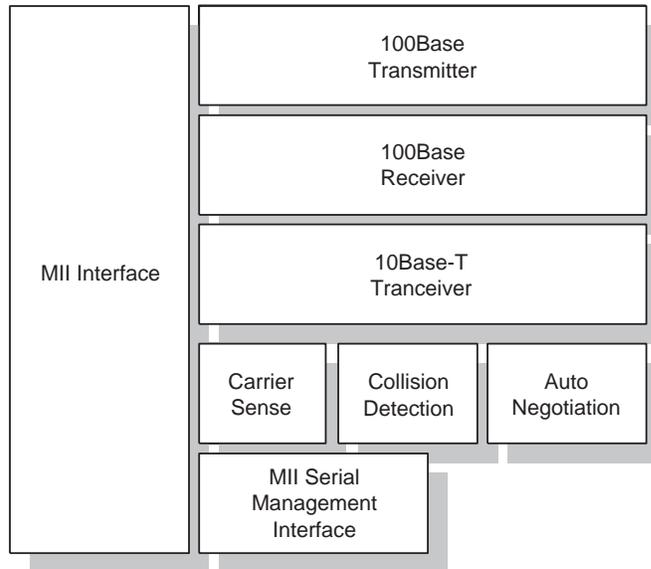


22164A-3

**Figure 1.   Functional Block Diagram**

## MII Interface

The purpose of the MII interface is to provide a simple, easy to implement connection between the MAC Reconciliation layer and the PHY. The MII is designed to make the differences between various media transparent to the MAC sublayer.

The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the PHY and the Reconciliation layer.

■ TXD (transmit data) is a nibble (4 bits) of data that are driven by the reconciliation sublayer synchronously with respect to TX_CLK. For each TX_CLK period which TX_EN is asserted, TXD (3:0) are accepted for transmission by the PHY.

■ TX_CLK (transmit clock) output to the MAC reconciliation sublayer is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals.

■ TX_EN (transmit enable) input from the MAC reconciliation sublayer to indicate nibbles are being presented on the MII for transmission on the physical medium. TX_ER (transmit coding error) transitions synchronously with respect to TX_CLK. If TX_ER is asserted for one or more clock periods, and TX_EN is asserted, the PHY will emit one or more symbols that are not part of the valid data delimiter set somewhere in the frame being transmitted.

■ RXD (receive data) is a nibble (4 bits) of data that are sampled by the reconciliation sublayer synchronously with respect to RX_CLK. For each RX_CLK period which RX_DV is asserted, RXD (3:0) are transferred from the PHY to the MAC reconciliation sublayer.

■ RX_CLK (receive clock) output to the MAC reconciliation sublayer is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals.

- RX_DV (receive data valid) input from the PHY to indicate the PHY is presenting recovered and decoded nibbles to the MAC reconciliation sublayer. To interpret a receive frame correctly by the reconciliation sublayer, RX_DV must encompass the frame starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.

- RX_ER (receive error) transitions synchronously with respect to RX_CLK. RX_ER will be asserted

for 1 or more clock periods to indicate to the reconciliation sublayer that an error was detected somewhere in the frame being transmitted from the PHY to the reconciliation sublayer.

- CRS (carrier sense) is asserted by the PHY when either the transmit or receive medium is non-idle and deasserted by the PHY when the transmit and receive medium are idle. Figure 2 depicts the behavior of CRS during 10BASE-T and 100BASE-TX transmission.
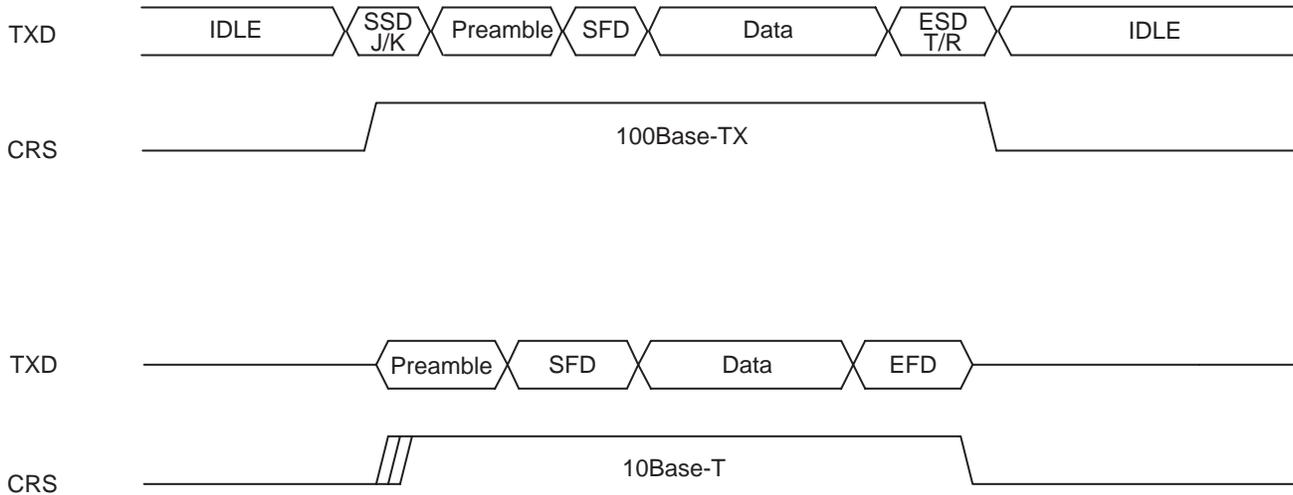


22164A-4

**Figure 2.   Carrier Sense during 10BASE-T and 100BASE-TX Transmission**

## 100BASE Operation

The 100BASE transmitter receives 4-bit nibble data clocked in at 25 MHz at the MII and outputs a scrambled 5-bit encoded MLT-3 signal to the media at 100 Mbps. The on-chip clock circuit converts the 25 MHz clock into a 125 MHz clock for internal use.

The IEEE 802.3u specification defines the Media Independent Interface. The interface specification defines a dedicated receive data bus and a dedicated transmit data bus.

These two busses include various controls and signal indications that facilitate data transfers between the NetPHY-1 device and the Reconciliation layer.

### 100BASE Transmit

The 100BASE transmitter consists of the functional blocks shown in Figure 3. The 100BASE transmit section converts 4-bit synchronous data provided by the MII to a scrambled MLT-3 125 million symbols per second serial data stream.
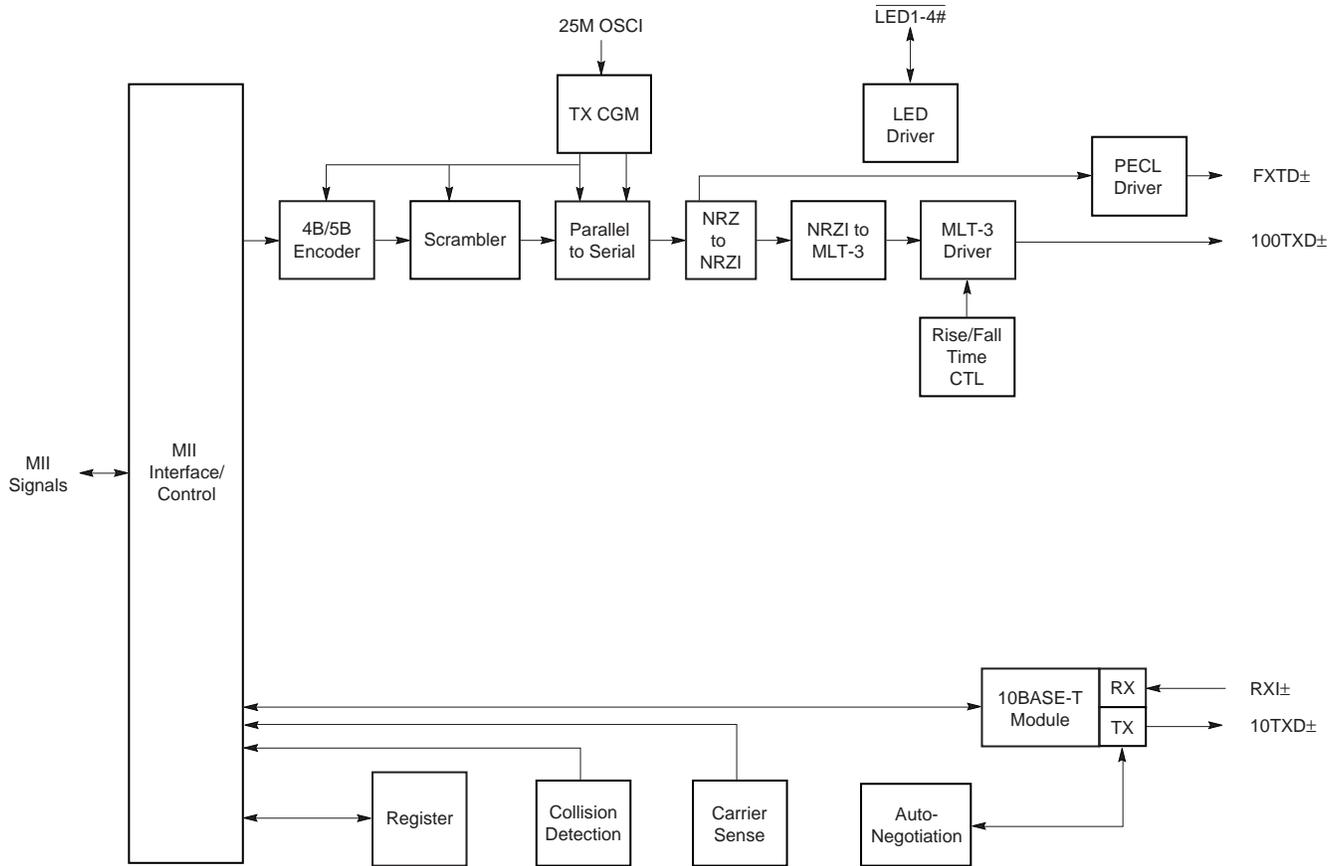
22164A-5

**Figure 3. 100BASE Transmitter Functional Block Diagram**

The block diagram in Figure 3 provides an overview of the functional blocks contained in the transmit section. The transmitter section contains the following functional blocks:

■ 4B5B Encoder

■ Scrambler

■ Parallel-to-Serial Converter

■ NRZ-to-NRZI Converter

■ PECL Driver (For FX Operation)

■ NRZI to MLT-3 (For TX Operation)

■ MLT-3 Driver (For TX Operation)

## 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission (see Table 1). This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit.

The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

The NetPHY-1 device includes a Bypass 4B5B conversion option within the 100BASE-TX transmitter for support of applications like 100 Mbps repeaters which do not require 4B5B conversion.

**AMD**

**Table 1.   4B5B Code Group**

| Symbol | Meaning | 4B code 3210 | 5B Code 43210 |
|---|---|---|---|
| 0 | Data 0 | 0000 | 11110 |
| 1 | Data 1 | 0001 | 01001 |
| 2 | Data 2 | 0010 | 10100 |
| 3 | Data 3 | 0011 | 10101 |
| 4 | Data 4 | 0100 | 01010 |
| 5 | Data 5 | 0101 | 01011 |
| 6 | Data 6 | 0110 | 01110 |
| 7 | Data 7 | 0111 | 01111 |
| 8 | Data 8 | 1000 | 10010 |
| 9 | Data 9 | 1001 | 10011 |
| A | Data A | 1010 | 10110 |
| B | Data B | 1011 | 10111 |
| C | Data C | 1100 | 11010 |
| D | Data D | 1101 | 11011 |
| E | Data E | 1110 | 11100 |
| F | Data F | 1111 | 11101 |
| I | Idle | undefined | 11111 |
| J | SFD (1) | 0101 | 11000 |
| K | SFD (2) | 0101 | 10001 |
| T | ESD (1) | undefined | 01101 |
| R | ESD (2) | undefined | 00111 |
| H | Error | undefined | 00100 |
| V | Invalid | undefined | 00000 |
| V | Invalid | undefined | 00001 |
| V | Invalid | undefined | 00010 |
| V | Invalid | undefined | 00011 |
| V | Invalid | undefined | 00101 |
| V | Invalid | undefined | 00110 |
| V | Invalid | undefined | 01000 |
| V | Invalid | undefined | 01100 |
| V | Invalid | undefined | 10000 |
| V | Invalid | undefined | 11001 |

## Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100BASE-TX operation. By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to repeated 5B sequences like continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies. Since EMI is not a concern in a fiber application, the scrambler is bypassed in 100BASE-FX.

## Parallel-to-Serial Converter

The Parallel-to-Serial Converter receives parallel 5B scrambled data from the scrambler and serializes it (i.e., converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ-to-NRZI Encoder block

## NRZ-to-NRZI Converter

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard for 100BASE-TX transmission over Category-5 unshielded twisted pair cable.

## PECL Driver For 100BASE-FX

The PECL driver accepts NRZI coded data and converts it to PECL signal levels for transmission over fiber media.

The output pair is a differential pseudo ECL (PECL) interface designed to connect directly to a standard fiber optic PMD. The differential driver for the FXTD± is current mode and is designed to drive resistive termination in a complementary mode. The FXTD± pins are incapable of sourcing current, this implies that VOH must be set by the ratios of the Thevenin termination resistors for each of the lines. RIOH is a pull-up resistor connected from the FXTD± output to VCC. RIOL is a pull-down resistor connected from the FXTD± output to ground. RIOH and RIOL are electrically in parallel from an AC standpoint. A target impedance of 50 $\Omega$ is needed for the transmission line impedance. A value of 62 $\Omega$ for RIOH and a value of 300 $\Omega$ for RIOL will yield a Thevenin equivalent characteristic impedance of 49.7 $\Omega$ and a VOH value of VCC-.88 volts, compatible with PECL circuits. VOL is required to be VDD-1.81 or greater. A sink current of 19 milli-amps (mA) would achieve this through the output termination resistors.

## MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events.

## MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver which converts these streams to current sources and alternately drives either side of the transmit transformer primary winding resulting in a minimal current MLT-3 signal. Refer to Figure 4 for the block diagram of the MLT-3 converter.

## 100BASE Receiver

The 100BASE receiver contains several function blocks that convert the scrambled 125 Mbps serial data to synchronous 4-bit nibble data that is then provided to the MII.

The receive section contains the following functional blocks:

■ Signal Detect

■ Adaptive Equalization

■ MLT-3-to-Binary Decoder

■ Clock Recovery Module

■ NRZI -o-NRZ Decoder

■ Serial-to-Parallel Converter

■ Descrambler

■ Code Group Alignment

■ 4B5B Decoder

### 100BASE-TX Signal Detect

The signal detect function meets the specifications mandated by the ANSI XT12 TP-PMD 100BASE-TX standards for both voltage thresholds and timing parameters.
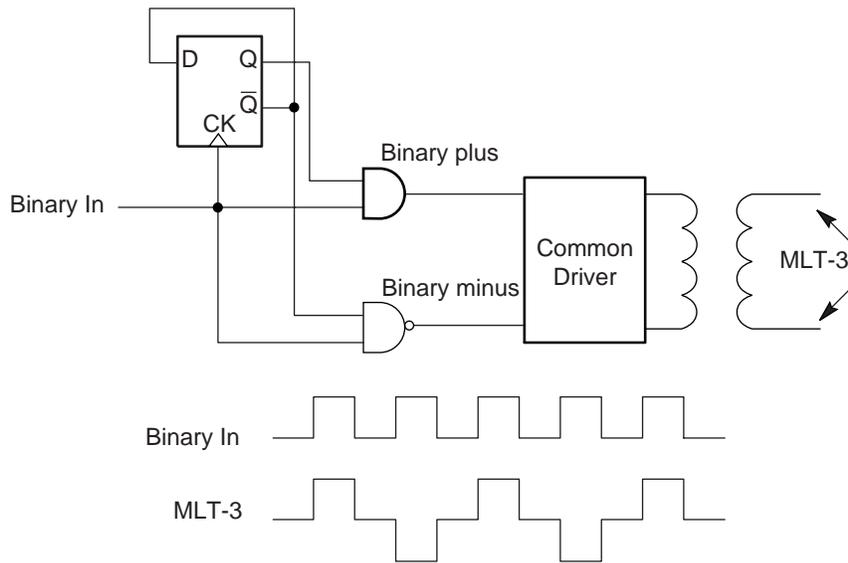


22164A-6

**Figure 4.   MLT-3 Converter Block Diagram**

### 100BASE-FX Signal Detect

The NetPHY-1 device accepts signal detect information on the FXSD pin at PECL signal levels from the FX Optical Module.

### Adaptive Equalization

When transmitting data at high speeds over copper twisted pair cable, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation

in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the received data.

In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will be over-kill in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will

cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

### PECL Receiver

The PECL receiver accepts PECL signal-level data from the FX Optical Module and presents it to the Clock Recovery Module.

### MLT-3-to-NRZI Decoder

The NetPHY-1 device decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data. The relationship between NRZI and MLT-3 data is shown in Figure 4.

### Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3-to-NRZI decoder or the PECL Receiver. The Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI-to-NRZ Decoder.

### NRZI-to-NRZ Decoder

The transmit data stream is required to be NRZI encoded in for compatibility with 100BASE transmission over. This conversion process must be reversed on the receive end. The NRZI-to-NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

### Serial-to-Parallel Converter

The Serial-to-Parallel Converter receives a serial data stream from the NRZI-to-NRZ converter, and converts the data stream to parallel data to be presented to the descrambler.

### Descrambler

Because of the scrambling process required to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, descrambles the data streams, and presents the data streams to the Code Group alignment block.

*Note: The scrambler is bypassed for 100BASE-FX operation.*

### Code Group Alignment

The Code Group Alignment block receives unaligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

### 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first two 5-bit code groups received are the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R symbols). The T/R symbol pair is also stripped from the nibble presented to the Reconciliation layer.

## 10BASE-T Operation

The 10BASE-T transceiver is IEEE 802.3u compliant. When the NetPHY-1 device is operating in 10BASE-T mode, the coding scheme is Manchester. Data processed for transmit is presented to the MII interface in nibble format, converted to a serial bit stream, then Manchester encoded. When receiving, the Manchester encoded bit stream is decoded and converted into nibble format for presentation to the MII interface.

### Collision Detection

For Half Duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. When a collision has been detected, it will be reported by the COL signal on the MII interface. Collision detection is disabled in Full Duplex operation.

### Carrier Sense

Carrier Sense (CRS) is asserted in Half Duplex operation during transmission or reception of data. During Full Duplex mode, CRS is asserted only during receive operations.

### Auto-Negotiation

The objective of Auto-Negotiation is to provide a means to exchange information between segment linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-Negotiation does not test the link segment characteristics. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-Negotiation also provides a parallel detection function for devices that do not support the Auto-Negotiation feature. During Parallel detection there is no exchange of configuration information, instead, the receive signal is examined. If it is discovered that the signal matches a technology that the receiving device

supports, a connection will be automatically established using that technology. This allows devices that do not support Auto-Negotiation but support a common mode of operation to establish a link.

## MII Serial Management

The MII serial management interface consists of a data interface, basic register set, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, get status and error information, and determine the type and capabilities of the attached PHY device(s).

The NetPHY-1 devices management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16,17, and 18.

In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits

(preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP):<10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written onto management registers.
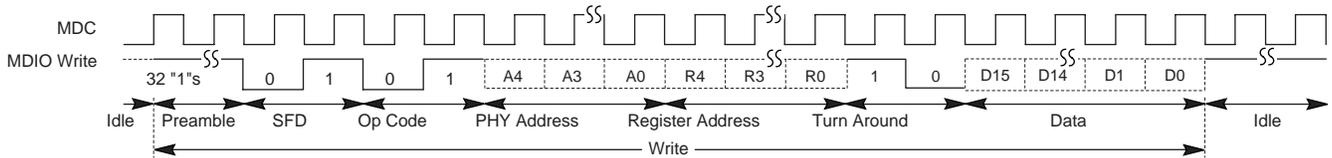
## Serial Management Interface

The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of Management Data Clock (MDC), and Management Data Input/Output (MDI/O) signals.

The MDIO pin is bidirectional and may be shared by up to 32 devices.
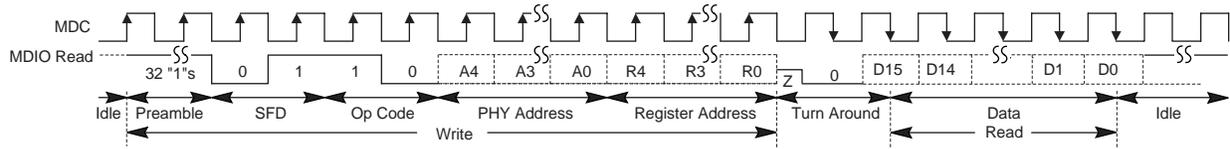


22164A-7

**Figure 5.   Management Interface - Read Frame Structure**



22164A-8

**Figure 6.   Management Interface - Write Frame Structure**

## Register Description

| Register Address | Register Name | Description |
|:---:|:---:|:---|
| 0 | BMCR | Basic Mode Control Register |
| 1 | BMSR | Basic Mode Status Register |
| 2 | PHYIDR1 | PHY Identifier Register 1 |
| 3 | PHYIDR2 | PHY Identifier Register 2 |
| 4 | ANAR | Auto-Negotiation Advertisement Register |
| 5 | ANLPAR | Auto-Negotiation Link Partner Ability Register |
| 6 | ANER | Auto-Negotiation Expansion Register |
| 16 | DSCR | AMD Specified Configuration Register |
| 17 | DSCSR | AMD Specified Configuration/Status Register |
| 18 | 10BTCSR | 10BASE-T Configuration/Status Register |
| Others | Reserved | Reserved For Future Use-Do Not Read/Write To These Registers |

**Key to Default**

In the register description that follows, the default column takes the form:

<Reset Value>, <Access Type> / <Attribute(s)>

Where

<Reset Value>:

| 1 | Bit set to logic one |
|:---:|:---|
| 0 | Bit set to logic zero |
| X | No default value |
| (Pin No.) | Value latched in from pin number at reset |

<Access Type>:

RO = Read only

RW = Read/Write

<Attribute (s)>:

SC = Self clearing

P = Value permanently set

LL = Latching low

LH = Latching high

## Basic Mode Control Register (BMCR) - Register 0

| Bit | Bit Name | Default | Description |
|-----|----------|---------|-------------|
| 0.15 | Reset | 0, RW/SC | **Reset**: <br> 1=Software reset <br> 0=Normal operation <br> When set this bit configures the PHY status and control registers to their default states. This bit will return a value of one until the reset process is complete. |
| 0.14 | Loopback | 0, RW | **Loopback**: <br> Loopback control register <br> 1=Loopback enabled <br> 0=Normal operation <br> When in 100M operation is selected, setting this bit will cause the descrambler to lose synchronization. A 720ms "dead time" will occur before any valid data appears at the MII receive outputs. |
| 0.13 | Speed Selection | 1, RW | **Speed Select**: <br> 1=100 Mbps <br> 0=10 Mbps <br> Link speed may be selected either by this bit or by Auto-Negotiation if bit 12 of this register is set. When Auto-Negotiation is enabled, this bit will return Auto-Negotiation link speed. |
| 0.12 | Auto-Negotiation Enable | 1, RW | **Auto-Negotiation Enable**: <br> 1= Auto-Negotiation enabled: <br> 0= Auto-Negotiation disabled: <br> When auto-Negotiation is enabled bits 8 and 13 will contain the Auto-Negotiation results. When Auto-Negotiation is disabled bits 8 and 13 will determine the duplex mode and link speed. |
| 0.11 | Power Down | 0, RW | **Power Down**: <br> 1=Power Down <br> 0=Normal Operation <br> Setting this bit will power down the NetPHY-1 device with the exception of the crystal oscillator circuit. |
| 0.10 | Isolate | (PHYAD= 00000), RW | **Isolate**: <br> 1= Isolate <br> 0= Normal Operation <br> When this bit is set the data path will be isolated from the MII interface. TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL and CRS will be placed in a high impedance state. The management interface is not effected by this bit. When the PHY Address is set to 00000 the isolate bit will be set upon power-up/reset. |

## Basic Mode Control Register (BMCR) - Register 0 (Continued)

| Bit | Bit Name | Default | Description |
|-----|----------|---------|-------------|
| 0.9 | Restart Auto-Negotiation | 0, RW/SC | **Restart Auto-Negotiation**:<br>1= Restart Auto-Negotiation.<br>0= Normal Operation<br>When this bit is set the Auto-Negotiation process is re-initiated. When Auto-Negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated. The operation of the Auto-Negotiation process will not be affected by the management entity that clears this bit. |
| 0.8 | Duplex Mode | 1, RW | **Duplex Mode**:<br>1= Full Duplex operation.<br>0= Normal operation<br>If Auto-Negotiation is disabled, setting this bit will cause the NetPHY-1 device to operate in Full Duplex mode. When Auto-Negotiation is enabled, this bit reflects the duplex selected by Auto-Negotiation. |
| 0.7 | Collision Test | 0, RW | **Collision Test**:<br>1= Collision Test enabled.<br>0= Normal Operation<br>When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN. |
| 0.6 | Reserved | 0, RO | **Reserved**:<br>Write as 0, ignore on read. |

## Basic Mode Status Register (BMSR) -
## Register 1

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 1.15 | 100BASE-T4 | 0,RO/P | **100BASE-T4 Capable**:<br>1=NetPHY-1 device is able to perform in 100BASE-T4 mode.<br>0=NetPHY-1 device is not able to perform in 100BASE-T4 mode. |
| 1.14 | 100BASE-TX<br>Full Duplex | 1,RO/P | **100BASE-TX Full Duplex Capable**:<br>1=NetPHY-1 device is able to perform 100BASE-TX in Full Duplex mode.<br>0=NetPHY-1 device is not able to perform 100BASE-TX in Full Duplex mode. |
| 1.13 | 100BASE-TX<br>Half Duplex | 1,RO/P | **100BASE-TX Half Duplex Capable**:<br>1=NetPHY-1 device is able to perform 100BASE-TX in Half Duplex mode.<br>0=NetPHY-1 device is not able to perform 100BASE-TX in Half Duplex mode. |
| 1.12 | 10BASE-T<br>Full Duplex | 1,RO/P | **10BASE-T Full Duplex Capable**:<br>1=NetPHY-1 device is able to perform 10BASE-T in Full Duplex mode.<br>0=NetPHY-1 device is not able to perform 10BASE-T in Full Duplex mode. |
| 1.11 | 10BASE-T<br>Half Duplex | 1,RO/P | **10BASE-T Half Duplex Capable**:<br>1=NetPHY-1 device is able to perform 10BASE-T in Half Duplex mode.<br>0=NetPHY-1 device is not able to perform 10BASE-T in Half Duplex mode. |
| 1.10-1.7 | Reserved | 0,RO | **Reserved**:<br>Write as 0, ignore on read. |
| 1.6 | MF Preamble<br>Suppression | 0,RO | **MII Frame Preamble Suppression**:<br>1=PHY will accept management frames with preamble suppressed.<br>0=PHY will not accept management frames with preamble suppressed. |
| 1.5 | Auto-Negotiation<br>Complete | 0,RO | **Auto-Negotiation Complete**:<br>1=Auto-Negotiation process completed.<br>0=Auto-Negotiation process not completed. |
| 1.4 | Remote Fault | 0,<br>RO/LH | **Remote Fault**:<br>1= Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is NetPHY-1 device implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set.<br>0= No remote fault condition detected. |
| 1.3 | Auto-Negotiation<br>Ability | 1,RO/P | **Auto Configuration Ability**:<br>1=NetPHY-1 device able to perform Auto-Negotiation.<br>0=NetPHY-1 device not able to perform Auto-Negotiation. |
| 1.2 | Link Status | 0,RO/LL | **Link Status**:<br>1=Valid link established (for either 10 Mbps or 100 Mbps operation).<br>0=Link not established.<br>The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the Link Status bit to be cleared and remain cleared until it is read via the management interface. |

## Basic Mode Status Register (BMSR) - Register 1

| Bit | Bit Name | Default | Description |
|-----|----------|---------|-------------|
| 1.1 | Jabber Detect | 0, RO/LH | **Jabber Detect**:<br>1=Jabber condition detected.<br>0=No jabber condition detected.<br>This bit is implemented with a latching function. Once Jabber conditions are detected this bit will remain set until a read operation is completed through a management interface or a NetPHY-1 device reset. This bit works only in 10 Mbps mode. |
| 1.0 | Extended Capability | 1,RO/P | **Extended Capability**:<br>1=Extended register capable.<br>0=Basic register capable only. |

## PHY ID Identifier Register 1 (PHYIDR1) - Register 2

The PHY Identifier Registers 1 and 2 work together in a single identifier of the NetPHY-1 device. The Identifier consists of a concatenation of the **Organizationally Unique Identifier** (OUI), a vendor's model number, and a model revision number. The IEEE assigned OUI is 00606E.

| Bit | Bit Name | Default | Description |
|-----|----------|---------|-------------|
| 2.15-2.0 | OUI_MSB | <0181H> | **OUI Most Significant Bits**:<br>This register stores bits 3 - 18 of the OUI (00606E) to bits 15 - 0 of this register, respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2). |

## PHY Identifier Register 2 (PHYIDR2) - Register 3

| Bit | Bit Name | Default | Description |
|-----|----------|---------|-------------|
| 3.15-3.10 | OUI_LSB | <101110>,RO/P | **OUI Least Significant Bits**:<br>Bits 19 - 24 of the OUI (00606E) are mapped to bits 15 - 10 of this register, respectively. |
| 3.9-3.4 | VNDR_MDL | <000000>,RO/P | **Vendor Model Number**:<br>Six bits of the vendor model number mapped to bits 9 - 4 (most significant bit to bit 9). |
| 3.3-3.0 | MDL_REV | <0001>,RO/P | **Model Revision Number**:<br>Four bits of the vendor model revision number mapped to bits 3 - 0 (most significant bit to bit 3). |

## Auto-Negotiation Advertisement Register(ANAR) - Register 4

This register contains the advertised abilities of the NetPHY-1 device as they will be transmitted to link partners during Auto-Negotiation.

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 4.15 | NP | 0,RO/P | **Next Page Indication**:<br>0=No next page available<br>1=Next page available<br>The NetPHY-1 device does not support the next page function. This bit is permanently set to 0 |
| 4.14 | ACK | 0,RO | **Acknowledge**:<br>1=Link partner ability data reception acknowledged.<br>0=Not acknowledged.<br>The NetPHY-1 device's Auto-Negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-Negotiation process. Software should not attempt to write to this bit. |
| 4.13 | RF | 0, RW | **Remote Fault**:<br>1=Local Device senses a fault condition.<br>0=No fault detected. |
| 4.12-4.11 | Reserved | 0, RW | **Reserved**:<br>Write as 0, ignore on read. |
| 4.10 | FCS | 0, RW | **Flow Control Support**:<br>1=Controller chip supports flow control ability.<br>0=Controller chip does not support flow control ability. |
| 4.9 | T4 | 0, RO/P | **100BASE-T4 Support**:<br>1=100BASE-T4 supported by the local device.<br>0=100BASE-T4 not supported.<br>The NetPHY-1 device does not support 100BASE-T4 so this bit is permanently set to 0. |
| 4.8 | TX_FDX | 1, RW | **100BASE-TX Full Duplex Support**:<br>1=100BASE-TX Full Duplex supported by the local device.<br>0=100BASE-TX Full Duplex not supported. |
| 4.7 | TX_HDX | 1, RW | **100BASE-TX Support**:<br>1=100BASE-TX supported by the local device.<br>0=100BASE-TX not supported. |
| 4.6 | 10_FDX | 1, RW | **10BASE-T Full Duplex Support**:<br>1=10BASE-T Full Duplex supported by the local device.<br>0=10BASE-T Full Duplex not supported. |
| 4.5 | 10_HDX | 1, RW | **10BASE-T Support**:<br>1=10BASE-T supported by the local device.<br>0=10BASE-T not supported. |
| 4.4-4.0 | Selector | <00001>, RW | **Protocol Selection Bits**:<br>These bits contain the binary encoded protocol selector supported by this node.<br><00001> indicates that this device supports IEEE 802.3 CSMA/CD. |

**AMD ☐**

## Auto-Negotiation Link Partner Ability Register (ANLPAR) - Register 5

This register contains the advertised abilities of the link partner as they are received during Auto-Negotiation.

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 5.15 | NP | 0, RO | **Next Page Indication**:<br>0= Link partner, no next page available.<br>1= Link partner, next page available. |
| 5.14 | ACK | 0, RO | **Acknowledge**:<br>1=Link partner ability data reception acknowledged.<br>0=Not acknowledged.<br>The NetPHY-1 device's Auto-Negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit. |
| 5.13 | RF | 0, RO | **Remote Fault**:<br>1=Remote fault indicated by link partner.<br>0=No remote fault indicated by link partner. |
| 5.12-5.10 | Reserved | 0, RO | **Reserved**:<br>Write as 0, ignore on read. |
| 5.9 | T4 | 0, RO | **100BASE-T4 Support**:<br>1=100BASE-T4 supported by the link partner.<br>0=100BASE-T4 not supported by the link partner. |
| 5.8 | TX_FDX | 0, RO | **100BASE-TX Full Duplex Support**:<br>1=100BASE-TX Full Duplex supported by the link partner.<br>0=b 100BASE-TX Full Duplex not supported by the link partner. |
| 5.7 | TX_HDX | 0, RO | **100BASE-TX Support**:<br>1=100BASE-TX Half Duplex supported by the link partner.<br>0=100BASE-TX Half Duplex not supported by the link partne.r |
| 5.6 | 10_FDX | 0, RO | **10BASE-T Full Duplex Support**:<br>1=10BASE-T Full Duplex supported by the link partner.<br>0=10BASE-T Full Duplex not supported by the link partner. |
| 5.5 | 10_HDX | 0, RO | **10BASE-T Support**:<br>1=10BASE-T Half Duplex supported by the link partner.<br>0=10BASE-T Half Duplex not supported by the link partner. |
| 5.4-5.0 | Selector | <00000>, RO | **Protocol Selection Bits**:<br>Link partners binary encoded protocol selector. |

## Auto-Negotiation Expansion Register
## (ANER) - Register 6

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 6.15-6.5 | Reserved | 0, RO | **Reserved**:<br>Write as 0, ignore on read. |
| 6.4 | PDF | 0, RO/LH | **Local Device Parallel Detection Fault**:<br>PDF=1: A fault detected via parallel detection function.<br>PDF=0: No fault detected via parallel detection function. |
| 6.3 | LP_NP_ABLE | 0, RO | **Link Partner Next Page Able**:<br>LP_NP_ABLE=1: Link partner, next page available.<br>LP_NP_ABLE=0: Link partner, no next page. |
| 6.2 | NP_ABLE | 0,RO/P | **Local Device Next Page Able**:<br>NP_ABLE=1: NetPHY-1 device, next page available.<br>NP_ABLE=0: NetPHY-1 device, no next page.<br>NetPHY-1 device does not support this function, so this bit is always 0. |
| 6.1 | PAGE_RX | 0, RO/LH | **New Page Received**:<br>A new link code word page received. This bit will be automatically cleared when the register (Register 6) is read by management. |
| 6.0 | LP_AN_ABLE | 0, RO | **Link Partner Auto-Negotiation Able**:<br>LP_AN_ABLE=1 indicates that the link partner supports Auto-Negotiation. |

## AMD Specified Configuration Register (DSCR) - Register 16

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 16.15 | BP_4B5B | , RW | **Bypass 4B5B Encoding and 5B4B Decoding**:<br>1=4B5B encoder and 5B4B decoder function bypassed.<br>0=Normal 4B5B and 5B4B operation The value of the pin is latched into this bit at power-up/reset. |
| 16.14 | BP_SCR | Pin 97, RW | **Bypass Scrambler/Descrambler Function**:<br>1=Scrambler and descrambler function bypassed.<br>0=Normal scrambler and descrambler operation.<br>The value of the input pin is latched into this bit at power-up/reset. |
| 16.13 | BP_ALIGN | Pin 98, RW | **Bypass Symbol Alignment Function**:<br>1= Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed.<br>0= Normal operation.<br>The value of the BPALIGN input pin is latched into this bit at power-up/reset. |
| 16.12 | Reserved | 0, RW | **Reserved**:<br>This bit must be set as 0. |
| 16.11 | REPEATER | Pin 94, RW | **Repeater/Node Mode**:<br>1=Repeater mode.<br>0=Node mode.<br>In Repeater mode, the Carrier Sense (CRS) output from the NetPHY-1 device will be asserted only by receive activity. In NODE mode, or a mode not configured for Full Duplex operation, CRS will be asserted by either receive or transmit activity.<br>The value of the RPTR/NODE input pin is latched into this bit at power-up reset. |
| 16.10 | TX | 1, RW | **100BASE-TX or FX Mode Control**:<br>1=100BASE-TX operation.<br>0=100BASE-FX operation. |
| 16.9 | UTP | 1, RW | **UTP Cable Control**:<br>1=The media is a UTP cable, 0=STP. |
| 16.8 | CLK25MDIS | 0, RW | **CLK25M Disable**:<br>1=CLK25M output clock signal tri-stated.<br>0=CLK25M enabled.<br>This bit should be set to 1 to disable the 25 MHz output and reduce ground bounce and power consumption. For applications requiring the CLK25M output, set this bit to 0. |
| 16.7 | F_LINK_100 | 1, RW | **Force Good Link in 100 Mbps**:<br>1=Normal 100 Mbps operation.<br>0=Force 100 Mbps good link status.<br>This bit is useful for diagnostic purposes. |
| 16.6 | Reserved | 0, RW | **Reserved**:<br>This bit must be written as 0. |

## AMD Specified Configuration Register (DSCR) -
## Register 16

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 16.5 | LINKLED_CTL | 0, RW | **LINKLED Mode Select**:<br>0= Link LED output configured to indicate link status only.<br>1= Link LED output configured to indicate traffic status: When the link status is OK, the LED will be on. When the chip is in transmitting or receiving, it flashes. |
| 16.4 | FDXLED_MODE | 0, RW | **FDXLED Mode Select**:<br>1= FDXLED output configured to indicate polarity in 10BASE-T mode.<br>0= FDXLED output configured to indicate Full DuplexFull Duplex mode status for 10 Mbps and 100 Mbps operation. |
| 16.3 | SMRST | 0, RW | **Reset State Machine**:<br>When this bit is set to 1, all state internal machines will be reset. This bit will clear after reset is completed. |
| 16.2 | MFPSC | 0, RW | **MF Preamble Suppression Control**:<br>1= MF preamble suppression on.<br>0= MF preamble suppression off.<br>MII frame preamble suppression control bi.t |
| 16.1 | SLEEP | 0, RW | **Sleep Mode**:<br>Writing a 1 to this bit will cause NetPHY-1 device to enter Sleep mode and power down all circuits except the oscillator and clock generator circuit. To exit Sleep mode, write 0 to this bit position. The prior configuration will be retained when the sleep state is terminated, but the state machine will be reset. |
| 16.0 | RLOUT | 0, RW | **Remote Loopout Control**:<br>When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing. |

**AMD** ⬛

## AMD Specified Configuration and Status Register (DSCSR) - Register 17

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 17.15 | 100FDX | 1, RO | **100 M Full Duplex Operation**:<br>After Auto-Negotiation is completed, the results will be written to this bit. A 1 in this bit position indicates 10 0M Full Duplex operation. The software can read bits [15:12] to determine which mode is selected after Auto-Negotiation. This bit is invalid when Auto-Negotiation is disabled. |
| 17.14 | 100HDX | 1, RO | **100 M Half Duplex Operation**:<br>After Auto-Negotiation is completed, the results will be written to this bit. A 1 in this bit position indicates 100 M Half Duplex operation. The software can read bits [15:12] to determine which mode is selected after Auto-Negotiation. This bit is invalid when Auto-Negotiation is disabled. |
| 17.13 | 10FDX | 1, RO | **10 M Full Duplex Operation**:<br>After Auto-Negotiation is completed, the results will be written to this bit. A 1 in this bit position indicates 10 M Full Duplex operation. The software can read bits [15:12] to determine which mode is selected after Auto-Negotiation. This bit is invalid when Auto-Negotiation is disabled. |
| 17.12 | 10HDX | 1, RO | **10 M Half Duplex Operation**:<br>After Auto-Negotiation is completed, the results will be written to this bit. A 1 in this bit position indicates 10M Half Duplex operation. The software can read bits [15:12] to determine which mode is selected after Auto-Negotiation. This bit is invalid when Auto-Negotiation is disabled. |
| 17.11-17.10 | Reserved | 0, RW | **Reserved**:<br>Write as 0, ignore on read. |
| 17.8-17.4 | PHYAD[4:0] | (PHYAD), RW | **PHY Address Bit 4:0**:<br>The values of the PHYAD[4:0] pins are latched to this register at power-up/reset. The first PHY address bit transmitted or received is the MSB (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY. A PHY address of <00000> will cause the isolate bit of the BMCR (bit 10, Register Address 00) to be set. |

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 17.3-17.0 | ANMB[3:0] | 0, RO | **Auto-Negotiation Monitor Bits**:<br>These bits are for debug only. The Auto-Negotiation status will be written to these bits.

| b3 | b2 | b1 | b0 | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | In IDLE state |
| 0 | 0 | 0 | 1 | Ability match |
| 0 | 0 | 1 | 0 | Acknowledge match |
| 0 | 0 | 1 | 1 | Acknowledge match fail |
| 0 | 1 | 0 | 0 | Consistency match |
| 0 | 1 | 0 | 1 | Consistency match fail |
| 0 | 1 | 1 | 0 | Parallel detect signal_link_ready |
| 0 | 1 | 1 | 1 | Parallel detect signal_link_ready fail |
| 1 | 0 | 0 | 0 | Auto-Negotiation completed successfully |

## 10BASE-T Configuration/Status (10BTCSRSCR) - Register 18

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 18.15 | Reserved | 0, RO | **Reserved**:<br>Write as 0, ignore on read. |
| 18.14 | LP_EN | 1, RW | **Link Pulse Enable**:<br>1=Transmission of link pulses enabled.<br>0=Link pulses disabled, good link condition forced.<br>This bit is valid only in 10 Mbps operation. |
| 18.13 | HBE | Inverse Pin 94, RW | **Heartbeat Enable**:<br>1=Heartbeat function enabled.<br>0=Heartbeat function disabled.<br>When the NetPHY-1 device is configured for Full Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full Duplex mode). The initial state of this bit is the inverse value of RPTR/NODE input pin at power on reset. |
| 18.12 | Reserved | 0, RO | **Reserved**:<br>Write as 0, ignore on read. |
| 18.11 | JABEN | 1, RW | **Jabber Enable**:<br>1= Jabber function enabled.<br>0= Jabber function disabled.<br>Enables or disables the Jabber function when the NetPHY-1 device is in 10BASE-T Full Duplex or 10BASE-T Transceiver Loop-back mode. |
| 18.10 | 10BT_SER | Pin 98, RW | **10BASE-T Serial Mode**:<br>1=10BASE-T serial mode selected.<br>0=10BASE-T nibble mode selected.<br>The value on the 10BTSER input pin is latched into this bit at power-up/rese.t<br>Serial mode not supported for 100 Mbps operation. |
| 18.9-18.1 | Reserved | 0, RO | **Reserved**:<br>Write as 0, ignore on read. |
| 18.0 | POLR | 0, RO | **Polarity Reversed**:<br>When this bit is set to 1, it indicates that the 10M cable polarity is reversed. This bit is set and cleared by 10BASE-T module automatically. |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . . . . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . . . . . . . . . . . –0°C to +70°C

Supply Voltage
with Respect to Ground . . . . . . . . . -4.75 V to +5.25 V

DC Input Voltage ($V_{IN}$) . . . . . . . . –0.5 V to $V_{CC}$ +0.5 V

DC Output or I/O Pin Voltage ($V_{OUT}$) . . . . .–0.5 V to
$V_{CC}$ +0.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

**Commercial (C) Devices**

Ambient Temperature ($T_A$)
Operating in Free Air. . . . . . . . . . . . . . .0°C to +70°C

Supply Voltage ($V_{CC}$)
with Respect to Ground . . . . . . . . +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**Power Consumption**

100BASE-TX Full Duplex . . . . . . . . . . . . . . . 185 mA

*(Measured using Unscrambled IDLE transmission looped back to RXIN, includes external termination circuitry)*

10BASE-T Full Duplex . . . . . . . . . . . . . . . . . 222 mA

*(Measured using Maximum packet size, minimum I.P.G. transmission looped back to RXIN, includes external termination circuitry)*

Auto-Negotiation . . . . . . . . . . . . . . . . . . . . . 165 mA

*(Measured during Parallel Detect until link established)*

Idle . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 120 mA

*(Measured with no link established)*

Power Down Mode . . . . . . . . . . . . . . . . . . . . . 40 mA

*(Measured while MII Register 0 Bit 11 set true)*

## DC ELECTRICAL CHARACTERISTICS
## ($V_{CC}$ = 5 $V_{DC}$, ±5%, $T_A$ = 0 to 70, unless specified otherwise)

| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{100TX}$ | Supply Current 100BASE 100BASE-TX active | $V_{cc}$ = 5.0 V | | 180 | 185 | mA |
| $I_{10TTP}$ | Supply Current 10BASE-TX active (Random data, Random IPG and Random size) | $V_{cc}$ = 5.0 V | | 120 | | mA |
| $I_{10TWC}$ | Supply Current 10BASE-TX active (Max. Packet size, Min. IPG and Worst case data pattern) | $V_{cc}$ = 5.0 V | | | 220 | mA |
| $I_{PDM}$ | Supply Current Power Down Mode | $V_{cc}$ = 5.0 V | | | 40 | mA |
| $I_{AN}$ | Supply Current during Auto-Negotiation | $V_{cc}$ = 5.0 V | | | 165 | mA |
| $I_{RST}$ | Supply Current during Reset. | $V_{cc}$ = 5.0 V | | | 115 | mA |
| **TTL Inputs** <br> **(TXD0-TXD3, TX_CLK, MDIO, TX_EN, TX_DV, TX_ER, TESTMODE, PHYAD0-4, OPMODE0-4, RPTR, BPALIGN, BP4B5B, BPSCR, 10BTSER, $\overline{RESET}$)** | | | | | | |
| $V_{IL}$ | Input Low Voltage | IIL = -400 uA | | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | IIH = 100 uA | 2.0 | | | V |
| $I_{IL}$ | Input Low Current | VIN = 0.4 V | -200 | | | uA |
| $I_{IH}$ | Input High Current | VIN = 2.7 V | | | 100 | uA |

## DC ELECTRICAL CHARACTERISTICS
## ($V_{CC}$ = 5 $V_{DC}$, ±5%, $T_A$ = 0 to 70, unless specified otherwise) (Continued)

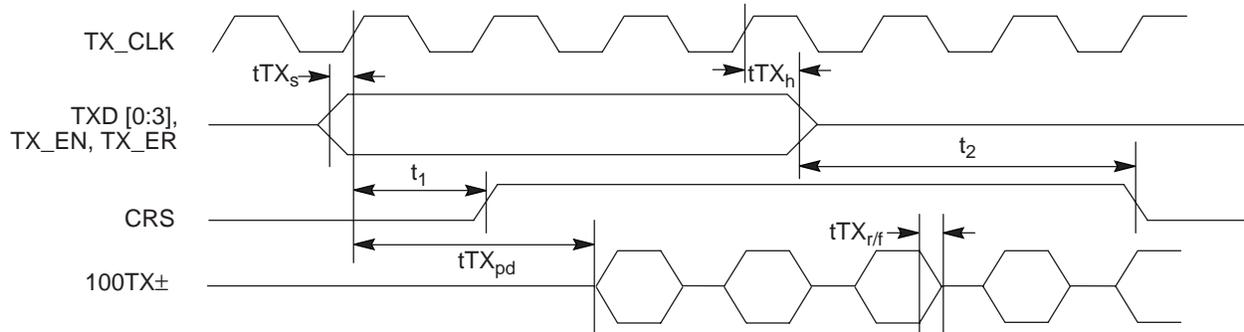| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| **MII TTL Outputs** **(RXD0-3, RX_EN, RX_DV, RX_ER, CRS, COL, MDIO)** | | | | | | |
| $V_{OL}$ | Output Low Voltage | IOL = 4 mA | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | IOH = -4 mA | 2.4 | | | V |
| **Non-MII TTL Outputs** **(TXLED, RXLED, LINKLED, COLLED, FDXLED, RX_LOCK)** | | | | | | |
| $V_{OL}$ | Output Low Voltage | IOL = 1 mA | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | IOH = -0.1 mA | 2.4 | | | V |
| $V_{ICM}$ | RXI+/RXI- Input Common-Mode Voltage | 100 Ω Termination Across | 1.5 | 2.0 | 2.5 | V |
| **Twisted Pair Transmitter** | | | | | | |
| $I_{TD100}$ | 100TX+± 100BASE-TX Mode Differential Output Current | | 19 | | 21 | mA |
| ITD10 | 10TX± 10BASE-T Differential Output Current | | 44 | 50 | 56 | mA |
| **PECL Receiver** | | | | | | |
| VIH - VCC | PECL Receiver Voltage - High | | -1.16 | | -0.90 | |
| VIL - VCC | PECL Receiver Voltage - Low | | -1.81 | | -1.48 | |
| **PECL Signal Detect** | | | | | | |
| VIH - VCC | PECL Signal Detect Voltage - High | | -1.16 | | -0.90 | |
| VIL - VCC | PECL Signal Detect Voltage - Low | | -1.81 | | -1.48 | |
| **PECL Transmitter** | | | | | | |
| VOH - VCC | PECL Output Voltage - High | | -1.05 | | -0.88 | |
| VOL - VCC | PECL Output Voltage - Low | | -1.85 | | -1.60 | |

## AC ELECTRICAL CHARACTERISTICS
## (Over full range of operating conditions unless specified otherwise)

| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| $t_{TR/F}$ | 100TXO+/- Differential Rise/Fall Time | | 3.0 | | 5.0 | ns |
| $t_{TM}$ | 100TXO+/- Differential Rise/Fall Time Mismatch | | -0.5 | | 0.5 | ns |
| $t_{TDC}$ | 100TXO+/- Differential Output Duty Cycle Distortion | | -0.5 | | 0.5 | ns |
| $t_{T/T}$ | 100TXO+/- Differential Output Peak-to-Peak Jitter | | | 300 | | ps |
| XOST | 100TXO+/- Differential Voltage Overshoot | | | | 5 | % |

## AC ELECTRICAL CHARACTERISTICS
## (Over full range of operating conditions unless specified otherwise) (Continued)

| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|--------|-----------|------------|-----|---------|-----|------|
| **PECL Transmitter (FX Transmit Interface)** | | | | | | |
| $pt_{TR/F}$ | 100FXTD+/- Differential Rise/Fall Time | | 1.0 | | 2.0 | ns |
| $pt_{TM}$ | 100FXTD+/- Differential Rise/Fall Time Mismatch | | -0.5 | | 0.5 | ns |
| $pt_{TDC}$ | 100FXTD+/- Differential Output Duty Cycle Distortion | | -0.5 | | 0.5 | ns |
| $pt_{PPJ}$ | 100FXTD+/- Differential Output Peak-to-Peak Jitter | | | | 300 | ps |
| $pt_{DDJ}$ | 100FXTD+/- Differential Output Data Dependent Jitter | | | | 500 | ps |
| **Clock Specifications** | | | | | | |
| XNTOL | TX Input Clock Frequency Tolerance | 25 MHz Frequency | | | | ppm |
| XBTOL | TX Output Clock Frequency Tolerance | 25 MHz Frequency | -100 | | +100 | ppm |
| $t_{PWH}$ | OSC Pulse Width High | | 14 | | | ns |
| $t_{PWL}$ | OSC Pulse Width Low | | 14 | | | ns |
| $t_{RPWH}$ | RX_CLK Pulse Width High | | 14 | | | ns |
| $t_{RPWL}$ | RX_CLK Pulse Width Low | | 14 | | | ns |

## MII 100BASE-TX Transmit Timing



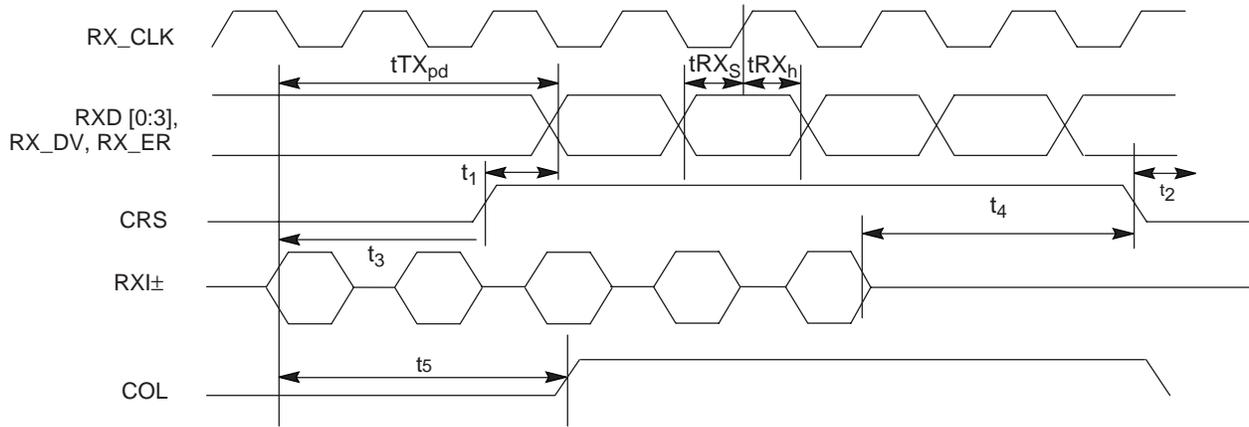22164A-9

**Figure 7.    MII 100BASE-TX Transmit Timing Diagram**

---

**MII 100BASE-TX Transmit Timing Parameters** (Half Duplex)

| Symbol | Parameter | Conditions | Min | Typical (Note 1) | Max | Unit |
|---|---|---|---|---|---|---|
| $tTX_s$ | TXD[0:3], TX_EN, TX_ER Setup To TX_CLK High | | 11 | - | - | ns |
| $tTX_h$ | TXD[0:3], TX_EN, TX_ER Hold From TX_CLK High | | 0 | - | - | ns |
| t1 | TX_EN Sampled To CRS Asserted | | - | 4 | - | BT |
| t2 | TX_EN Sampled To CRS De-asserted | | - | 4 | - | BT |
| $tTX_{pd}$ | TX_EN Sampled To TPO Out (Tx Latency) | | - | 8 | - | BT |
| $tTX_{r/f}$ | 100TX Driver Rise/Fall Time | 90% To 10%, Into 100 $\Omega$ Differential | 3 | 4 | 5 | ns |

**Note:**
1. Typical values are at 25 and are for design aid only; not guaranteed and not subject to production testing.

## MII 100BASE-TX Receive Timing



22164A-10

**Figure 8.   MII 100BASE-TX Receive Timing Diagram**

**MII-100BASE-TX Receive Timing Parameter** (Half Duplex)

| Symbol | Parameter | Conditions | Min | Typical (Note 1[)] | Max | Unit |
|--------|-----------|------------|-----|--------------------|-----|------|
| $tRX_s$ | RXD[0:3], RX_DV, RX_ER Setup To RX_CLK High | | 10 | - | - | ns |
| $tRX_h$ | RXD[0:3], RX_DV, RX_ER Hold From RX_CLK High | | 10 | - | - | ns |
| $tRX_{pd}$ | RXI In To RXD[0:3] Out (RX Latency) | | - | 15 | - | BT |
| t1 | CRS Asserted To RXD[0:3], RX_DV, RX_ER | | - | 4 | - | BT |
| t2 | CRS De-asserted To RXD[0:3], RX_DV, RX_ER | | - | 0 | - | BT |
| t3 | RXI In To CRS Asserted | | 10 | - | 14 | BT |
| t4 | RXI Quiet To CRS De-asserted | | 14 | - | 18 | BT |
| t5 | RXI In To COL De-asserted | | 14 | - | 18 | BT |

**Note:**

1. Typical values are at 25 and are for design aid only; not guaranteed and not subject to production testing.

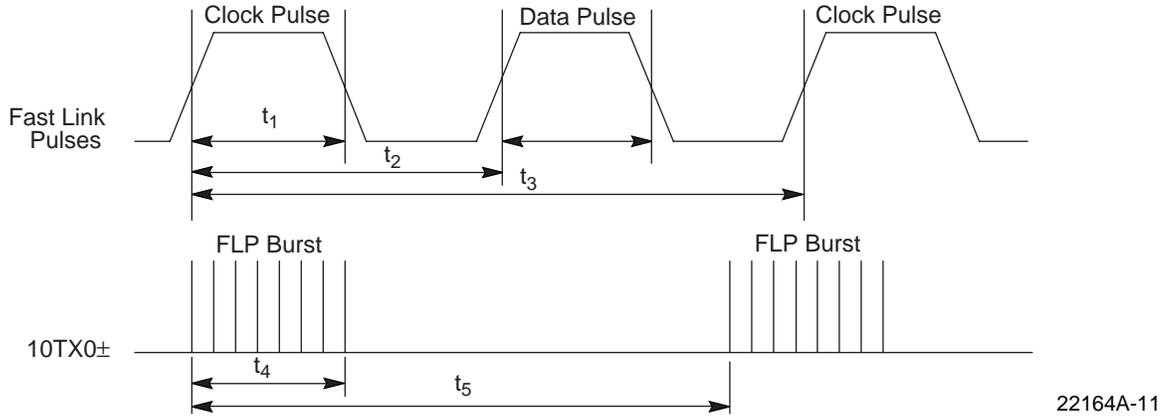## Auto-Negotiation and Fast Link Pulse Timing



**Figure 9.    Auto-Negotiation and Fast Link Pulse Timing Diagram**

### Auto-Negotiation and Fast Link Pulse Timing Parameters

| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|--------|-----------|-----------|-----|---------|-----|------|
| t1 | Clock/Data Pulse Width | | - | 100 | - | ns |
| t2 | Clock Pulse To Data Pulse Period | DATA = 1 | - | 62.5 | - | us |
| t3 | Clock Pulse To Clock Pulse Period | | - | 125 | - | us |
| t4 | FLP Burst Width | | - | 2 | - | ms |
| t5 | FLP Burst To FLP Burst Period | | - | 13.93 | - | ms |
| - | Clock/Data Pulses Per Burst | | 33 | 33 | 33 | ea |

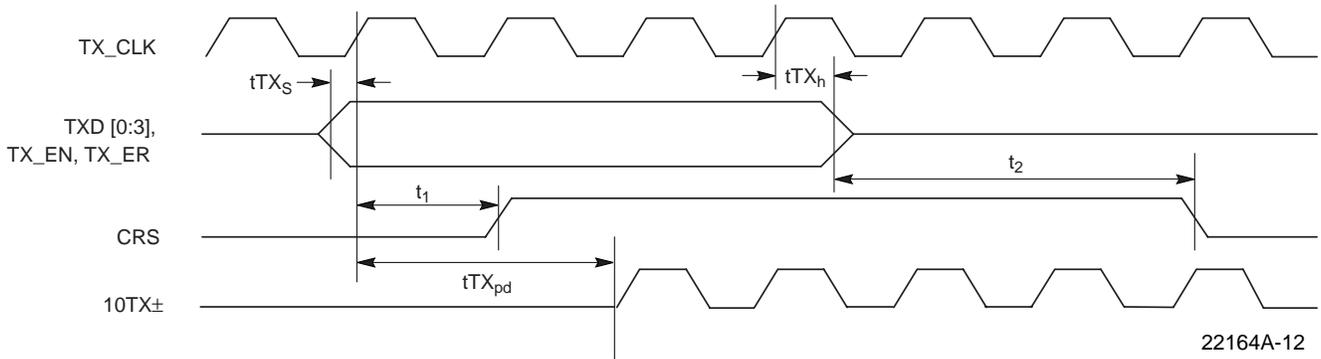## MII 10BASE-T Nibble Transmit Timing



**Figure 10.    MII 10BASE-T Nibble Transmit Timing Diagram**

### MII-10BASE-T Nibble Transmit Timing Parameters

| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|--------|-----------|-----------|-----|---------|-----|------|
| $tTX_s$ | TXD[0:3), TX_EN, TX_ER Setup To TX_CLK High | | 11 | - | - | ns |
| $tTX_h$ | TXD[0:3], TX_EN, TX_ER Hold From TX_CLK High | | 0 | - | - | ns |
| t1 | TX_EN Sampled To CRS Asserted | | - | 2 | 4 | BT |
| t2 | TX_EN Sampled To CRS De-asserted | | - | 15 | 20 | BT |
| $tTX_{pd}$ | TX_EN Sampled To 10TXO Out (Tx Latency) | | - | 2 | 4 | BT |

## MII 10BASE-T Receive Nibble Timing Diagram
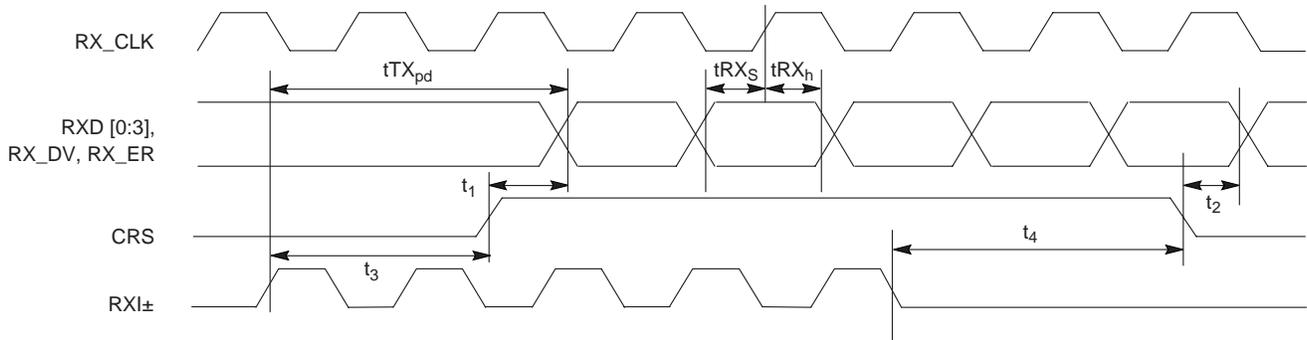


22164A-13

**Figure 11.   MII 10BASE-T Receive Nibble Timing Diagram**

### MII-10BASE-T Receive Nibble Timing Parameters

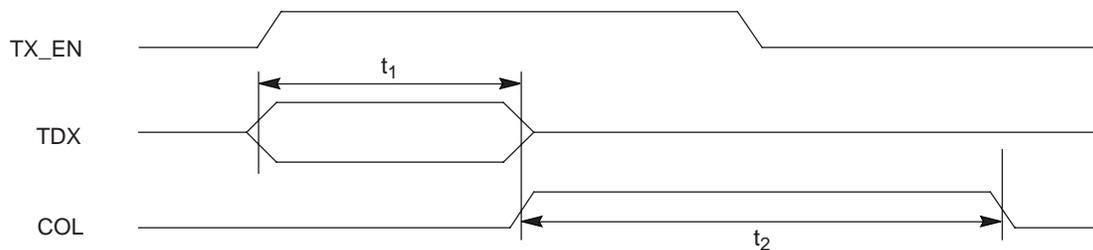| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| $tRX_s$ | RXD[0:3), RX_DV, RX_ER Setup To RX_CLK High | | 10 | - | - | ns |
| $tRX_h$ | RXD[0:3], RX_DV, RX_ER Hold From RX_CLK High | | 10 | - | - | ns |
| $tRX_{pd}$ | RXI In To RXD[0:3] Out (RX Latency) | | - | 7 | - | BT |
| t1 | CRS Asserted To RXD[0:3], RX_DV, RX_ER | | 1 | 14 | 20 | BT |
| t2 | CRS De-asserted To RXD[0:3], RX_DV, RX_ER | | - | - | 3 | BT |
| t3 | RXI In To CRS Asserted | | 1 | 2 | 4 | BT |
| t4 | RXI Quiet To CRS De-asserted | | 1 | 10 | 15 | BT |

## 10BASE-T SQE (Heartbeat) Timing
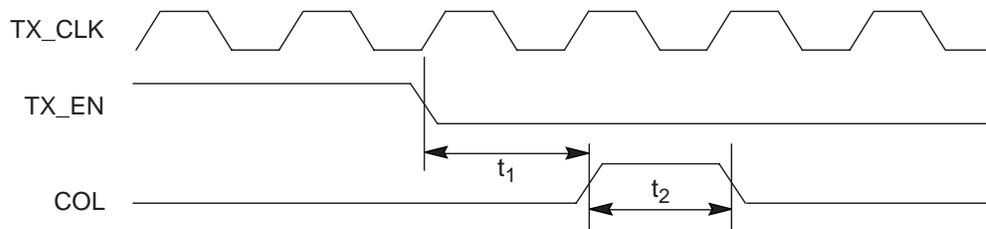


22164A-14

**Figure 12.    10BASE-T SQE (Heartbeat) Timing Diagram**

**10BASE-T SQE (Heartbeat) Timing Parameters**

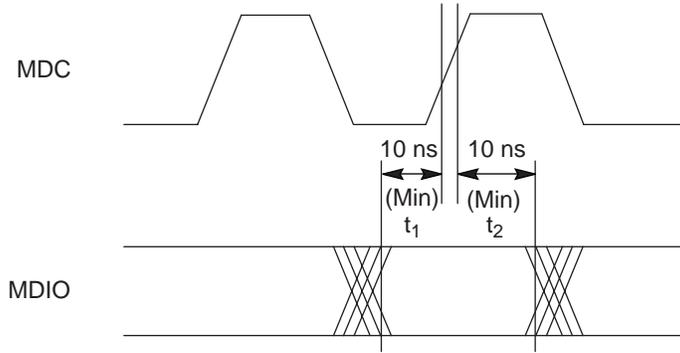| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|--------|-----------|------------|-----|---------|-----|------|
| t1 | COL (SQE) Delay After TX_EN Off | | 0.65 | 1.3 | 1.6 | ms |
| t2 | COL (SQE) Pulse Duration | | 0.5 | 1.1 | 1.5 | ms |

## 10BASE-T Jab and Unjab Timing



22164A-15

**Figure 13.    10BASE-T Jab and Unjab Timing Diagram**

**10BASE-T Jab and Unjab Timing Parameters**

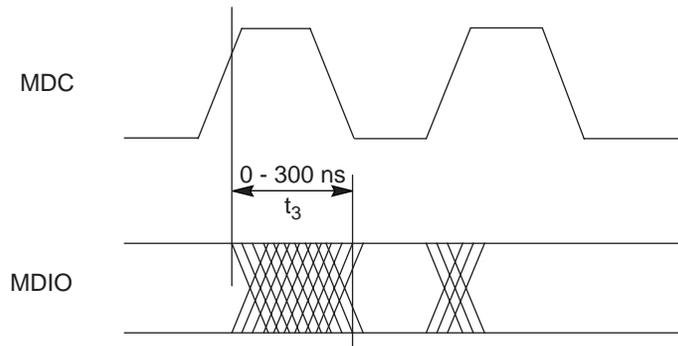| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|--------|-----------|------------|-----|---------|-----|------|
| t1 | Maximum Transmit Time | | 20 | 48 | 150 | ms |
| t2 | Unjab Time | | 250 | 505 | 1500 | ms |

## MDIO Timing when OUTPUT by STA



22164A-16

**Figure 14.    MDIO Timing when OUTPUT by STA Timing Diagram**

## MDIO Timing when OUTPUT by NetPHY-1 Device



22164A-17

**Figure 15.    MDIO Timing when OUTPUT by NetPHY-1 Timing Diagram**

### MII Timing Parameters

| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|--------|-----------|------------|-----|---------|-----|------|
| t1 | MDIO Setup Before MDC | When OUTPUT By STA | 10 | - | - | ns |
| t2 | MDIO Hold After MDC | When OUTPUT By STA | 10 | - | - | ns |
| t3 | MDC To MDIO Output Delay | When OUTPTU By NetPHY-1 device | 0 | - | 100 | ns |

## MAGNETICS SELECTION GUIDE

The NetPHY-1 device requires a 1:1 ratio for both the receive and the transmit transformers. Refer to Table 2 for transformer requirements. Transformers meeting these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetics before using them in an application. The transformers listed in Table 2 are electrical equivalent, but may not be pin-to-pin equivalent.

**Table 2.   Transformer Requirements**

| Manufacturer | Part Number |
|---|---|
| **Bel Fuse** | S558-5999-01 |
| **Delta** | LF8200, LF8221 |
| **HALO Electronics, Inc.** | Single Port<br>TG22-3506ND, TD22-3506G1, TG22-S010ND, TG22-S012ND, TG110-S050N2<br>Quad Port<br>TG110-6506NX, TG110-S450NX, TG110-S452NX |
| **Nano Pulse Inc.** | NPI 6181-37, NPI 6120-30, NPI 6120-37<br>NPI 6170-30 |
| **Pulse Engineering** | PE-68517, PE-68515, H1019, H1012 ----Single Port<br>H1027, H1028 ---- Dual Port<br>PE-69037, H1001, H1036, H1044 ---- Quad Port |
| **Valor** | ST6114, ST6118 |
| **YCL** | 20PMT04, 20PMT05 |

## CRYSTAL SELECTION GUIDE

A crystal can be used to generate the 25 MHz reference clock instead of a crystal oscillator. An M-TRON crystal, part number is 00301-00169, MP-1 Fund, @ 25.000000 MHz, ±50 ppm or equivalent may be used. The crystal must be a fundamental type, parallel resonant. Connect to X1 and X2, shunt each crystal lead to ground with an 18pf capacitor (see Figure 16).
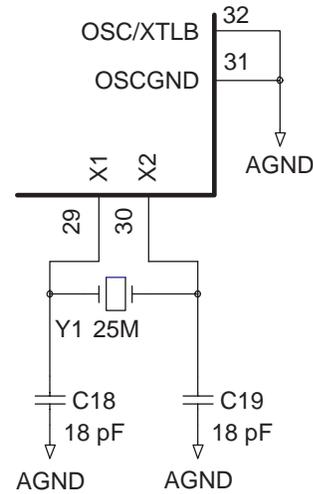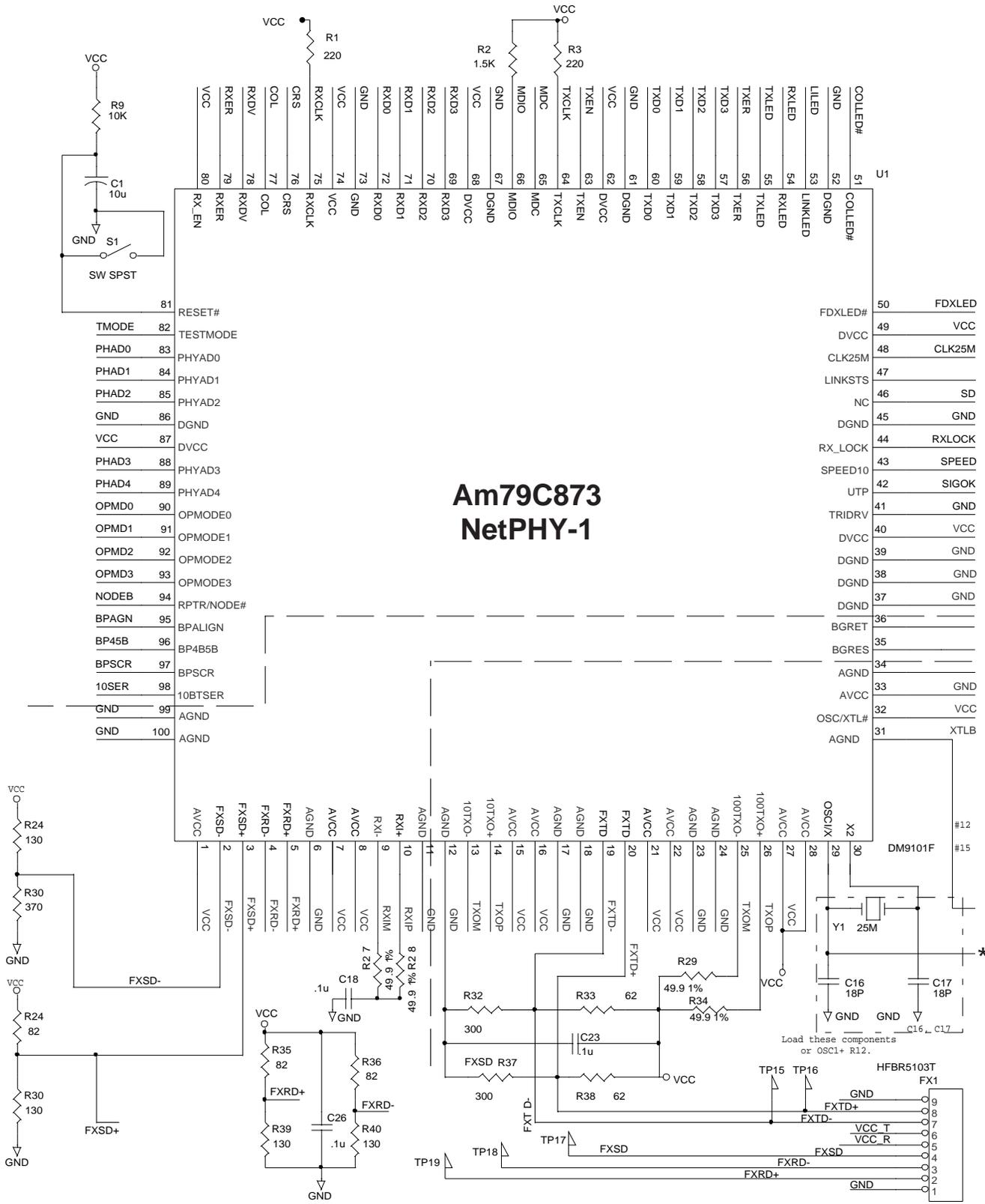


22164A-18

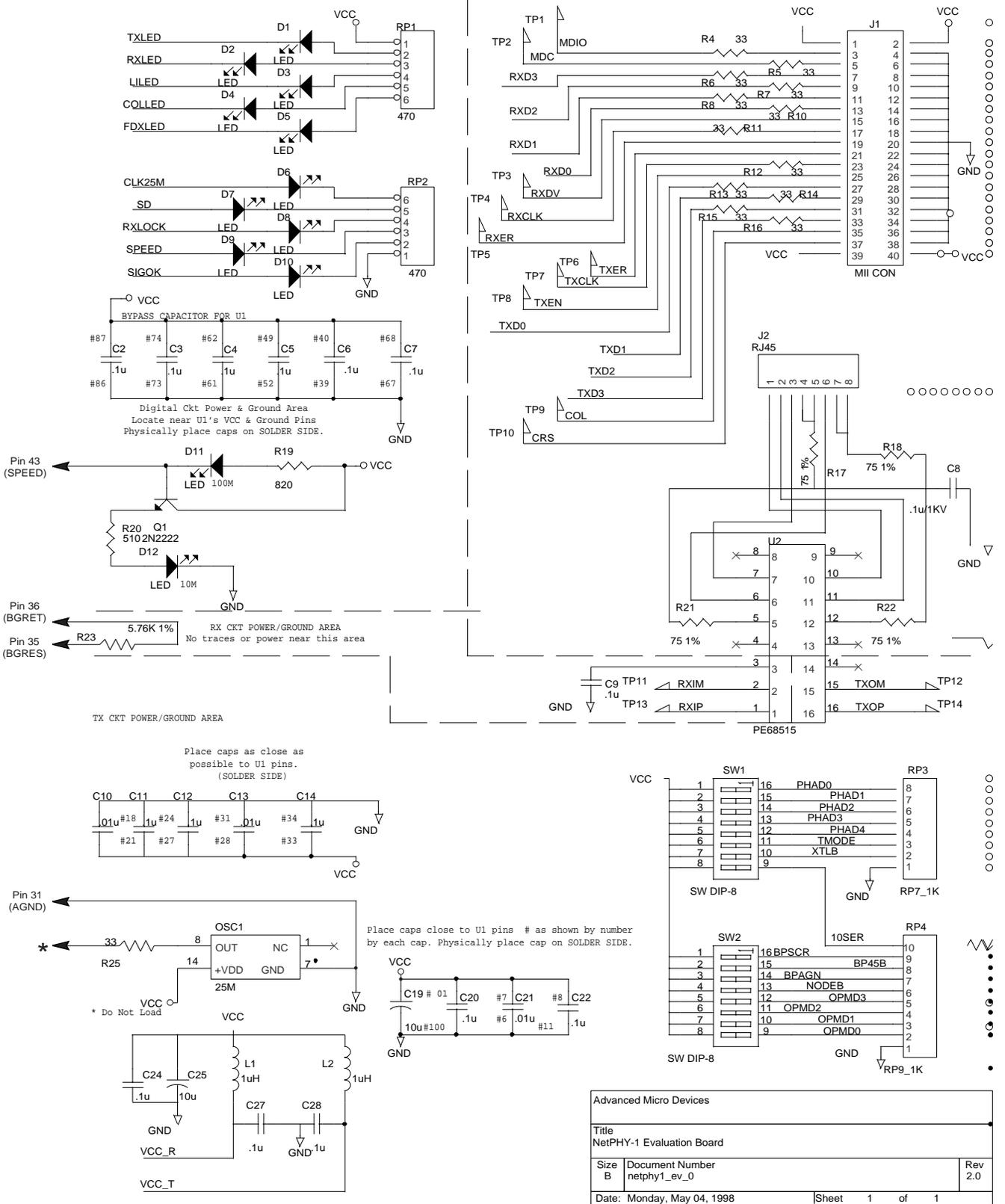**Figure 16.   Crystal Circuit Diagram**

Table 3.   Part List for Example Design

| Item No | Qty | Reference Number | Part Description |
|---|---|---|---|
| 1 | 11 | C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C13 | Capacitor, Decoupling, 0.1 µf, 50 V |
| 2 | 1 | C12 | Capacitor, .01 µf, 2KV |
| 3 | 4 | D1,D2,D3,D4 | LED, General Purpose |
| 4 | 1 | J1 | Connector, RJ45 |
| 5 | 2 | L1,L2 | Ferrite, Panasonic EXCCL4532U |
| 6 | 1 | OSC1 | Oscillator, Crystal, 25 MHz, ±50 ppm |
| 7 | 2 | Q2,Q1 | Transistor, NNP, General Purpose, 2N2222 |
| 8 | 2 | R1,R2 | Resistor, 470$\Omega$, 5% |
| 9 | 1 | R3 | Resistor, 820$\Omega$, 5% |
| 10 | 1 | R4 | Resistor, 33$\Omega$, 5% |
| 11 | 1 | R5 | Resistor, 510$\Omega$, 5% |
| 12 | 1 | R6 | Resistor, 6.01K$\Omega$, 1% |
| 13 | 4 | R7,R8,R14,R15 | Resistor, 49.9$\Omega$, 1% |
| 14 | 1 | R9 | Resistor, 1.5K$\Omega$, 5% |
| 15 | 4 | R10,R11,R12,R13 | Resistor, 75$\Omega$, 1% |
| 16 | 2 | R17,R16 | Resistor, 10K$\Omega$, 5% |
| 17 | 1 | U1 | NetPHY-1 device, PHY/Transceiver, 100 pin QFP |
| 18 | 1 | U2 | Magnetics, Pulse Engineering, PE68515 |
| 19 | 3 | R17,R18,R21 | Resistor 82$\Omega$, 5% |
| 20 | 2 | R19,R21 | Resistor 62$\Omega$, 5% |
| 21 | 3 | R22,R23,R26 | Resistor 130$\Omega$, 5% |
| 22 | 2 | R24,R25 | Resistor 300$\Omega$, 5% |

## NetPHY-1 MII Example Schematic

## NetPHY-1 MII Example Schematic (Continued)

## PHYSICAL DIMENSIONS*

### PQR100



Detail F

*For Reference Only

**Notes:**

1. Dimension D & E do not include resin fins.

2. Dimension GD & GE are for PC Board surface mount pad pitch design reference only.

3. All dimensions are based on metric system.

| Symbol | Dimensions In Inches | | Dimensions In mm | |
|--------|------------|---------|------------|---------|
| A | 0.130 Max. | | 3.30 Max. | |
| A1 | 0.004 Min. | | 0.10 Min. | |
| A2 | 0.1120.005 | | 2.85 ±0.13 | |
| b | 0.012 | +0.004 -0.002 | 0.31 | +0.10 -0.05 |
| c | 0.006 | +0.004 -0.002 | 0.15 | +0.10 -0.05 |
| D | 0.551 ±0.005 | | 14.00 ±0.13 | |
| E | 0.787 ±0.005 | | 20.00 ±0.13 | |
| e | 0.026 ±0.006 | | 0.65 ±0.15 | |
| F | 0.742 NOM. | | 18.85 NOM. | |
| GD | 0.693 NOM. | | 17.60 NOM. | |
| GE | 0.929 NOM. | | 23.60 NOM. | |
| HD | 0.740 ±0.012 | | 18.80 ±0.31 | |
| HE | 0.976 ±0.012 | | 24.79 ±0.31 | |
| L | 0.047 ±0.008 | | 1.19 ±0.20 | |
| L1 | 0.095 ±0.008 | | 2.41 ±0.20 | |
| y | 0.004 Max. | | 0.15 Max. | |
| q | 0∞ ~ 12∞ | | 0∞ ~ 12∞ | |

**Trademarks**