

MAAPSS0003

Preliminary



PCS TDMA/CDMA Power Amplifier 1750 - 1910 MHz

Features

- High Gain 2-stage HBT Amplifier
- Single Supply, 3V Operation
- 29dBm Linear Output Power
- High Efficiency
- Low Quiescent Current
- Operates in US and Korean PCS Bands
- Miniature FQFP-N 4mm Plastic Package

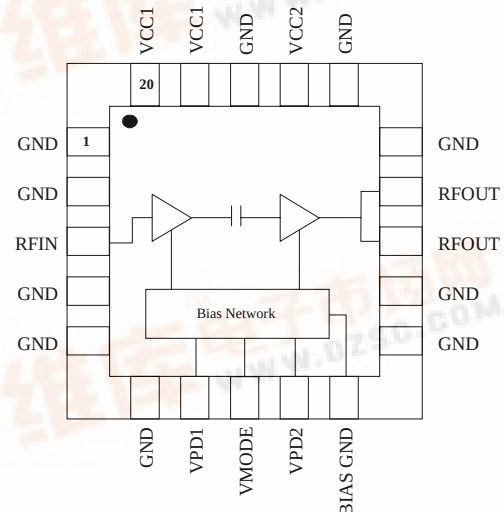
Description

M/A-COM's MAAPSS0003 is a high power, high efficiency linear power amplifier in a miniature FQFP-N 4mm plastic package. The MAAPSS0003 includes a 2-stage amplifier and bias control network. Analog signals control output power and power-off for active and standby modes.

The MAAPSS0003 is ideally suited for TDMA and CDMA handset applications where high linearity and low power consumption are important transmitter requirements. The MAAPSS0003 is design to operate with the MD59-0062 Upconverter/Driver IC.

The MAAPSS0003 is fabricated using M/A-COM's *iHBT* HBT process. The process utilizes the InGaP/GaAs materials system for reduced performance variation over temperature, high reliability and improved manufacturability.

Functional Block Diagram



Ordering Information

Part Number	Package
MAAPSS0003	FQFP-N 4.0mm Plastic Package
MAAPSS0003TR	Forward Tape and Reel ¹
MAAPSS0003RTR	Reverse Tape and Reel ¹

1. If specific reel size is required, consult factory for part number assignment.

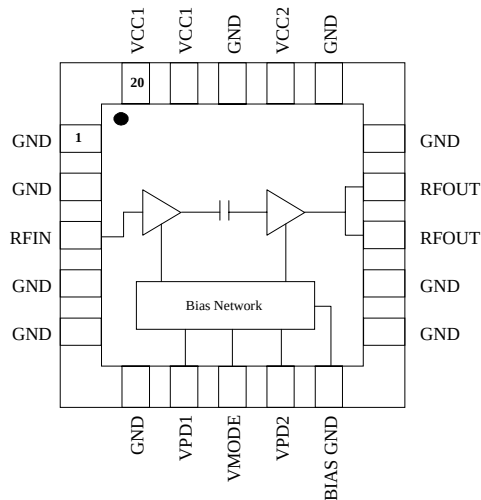
Electrical Specifications: $V_{CC} = 3.4V$, $V_{ref} = 3.0V$, $T_A = +25^{\circ}C$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Frequency Range		MHz	1850		1910
Small Signal Gain	$P_{OUT} \leq 0$ dBm	dB		27	
Linear Gain	$P_{OUT} = 29$ dBm	dB		26	
Linear Output Power	At maximum ACPR Level	dBm	29		
ACPR ¹		dBc			-44
Efficiency	$P_{OUT} = 29$ dBm	%	32		
Quiescent Current		mA		100	
Noise Power in Rx Band	$P_{OUT} \leq 29$ dBm	dBm/Hz			-139
2 nd Harmonic Suppression	$P_{OUT} \leq 29$ dBm	dBc			-40
3 rd Harmonic Suppression	$P_{OUT} \leq 29$ dBm	dBc			-40
Input V_{SWR}				2:1	
Stability	No oscillations, any phase			5:a	
Output Load Ruggedness V_{SWR}	No damage, any phase			10:1	

1. Per IS95: ACPR is defined as the ratio of the total power in a 1.228MHz bandwidth to the power within a 30KHz bandwidth measured at ± 1.25 MHz offset from the carrier frequency.

Specifications subject to change without notice.

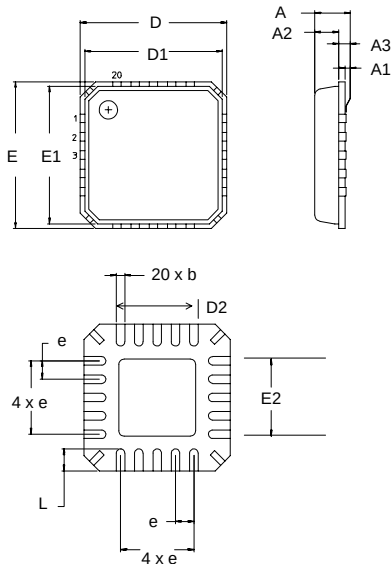
Block Diagram



PIN Configuration

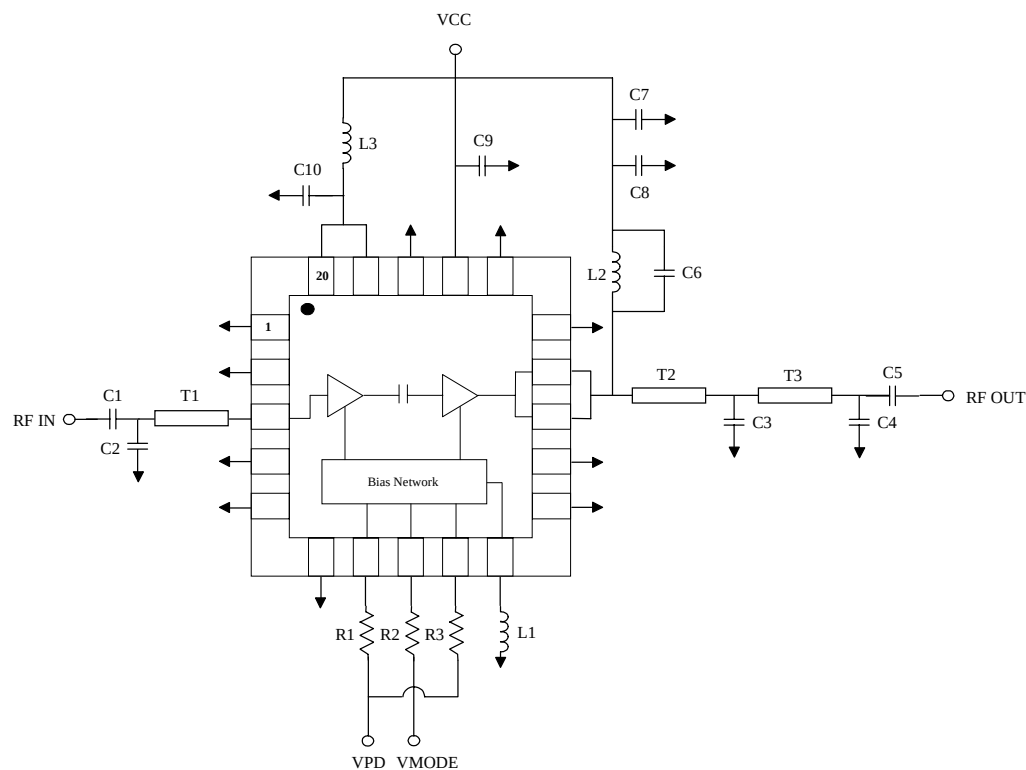
PIN #	PIN Name	Description
1	GND	DC and RF Ground
2	GND	DC and RF Ground
3	RFIN	RF input to the amplifier, requires matching network
4	GND	DC and RF Ground
5	GND	DC and RF Ground
6	GND	DC and RF Ground
7	VPD1	1 st stage bias control
8	VMODE	High / Low gain selector
9	VPD2	2 nd stage bias control
10	BIAS GND	Bias Control Ground, requires RF choke
11	GND	DC and RF Ground
12	GND	DC and RF Ground
13	RF OUT	RF Output of the amplifier, requires matching network
14	RF OUT	RF Output of the amplifier, requires matching network
15	GND	DC and RF Ground
16	GND	DC and RF Ground
17	V _{CC2}	Voltage supply for the bias network
18	GND	DC and RF Ground
19	V _{CC1}	Voltage supply for 1 st stage, requires matching network
20	V _{CC1}	Voltage supply for 1 st stage, requires matching network

FQFP-N 4 mm



Dim.	Measurement (mm)		
	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3		0.25 ref.	
b	0.18	0.23	0.30
D		4.00 basic	
D1		3.75 basic	
D2	0.75	1.70	2.25
e		0.50 basic	
E		4.00 basic	
E1		3.75 basic	
E2	0.75	1.70	2.25
L	0.35	0.55	0.75

Sample Board Schematic



External Circuitry Parts List ¹

Ref. Designation	Value	Purpose
C1	3.0 pF	RF Matching / DC Block
C2	2.7 pF	RF Matching
C3, C7	4.7 pF	RF Matching
C4	2.2 pF	RF Matching
C5	15 pF	DC Block
C8, C9	15 pF	RF Matching
C6	0.8 pF	RF Matching
C10	9.0 pF	RF Matching
L1, L2	15.0 nH	RF Choke
L3	8.2 nH	RF Choke
R1	TBD	Bias Adjust
R2	TBD	Bias Adjust
R3	TBD	Bias Adjust
T1	350 Mils	RF Matching
T2	40 Mils	RF Matching
T3	250 Mils	RF Matching

1. Values of external elements not final.