MAS9138/40

ASYNCHRONOUS TO SYNCHRONOUS CONVERTER

- **Pin compatible with MAS7838**
- **Interfaces a duplex asynchronous to synchronous channel**
- **Modem speeds of 600, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, 12k, 14.4k, 19.2k and 38.4k bps with a single 4.9152 MHz crystal**

DESCRIPTION

MAS9138 is a single chip duplex asynchronous to synchronous converter. It converts asynchronous start stop characters to synchronous format, with stop bit deletion when required as defined in the CCITT recommendation V.14. On the receiver channel MAS9138 converts the incoming synchronous data to asynchronous start stop character format with stop bit insertion when required as defined in the CCITT recommendation V.14. MAS9138 implements the data modes for the synchronous interface as specified in the V.14. MAS9138 can be configured to operate at any frequency up to 38.4 kbits/s within these modes. The device contains a bit generator and frequency selection logic to allow easy operation at other data rates. With just one crystal the device can adapt to ten (10) different bit rates so it is ideally suited to be used with the most common modem systems ranging from V.22 to V.34.

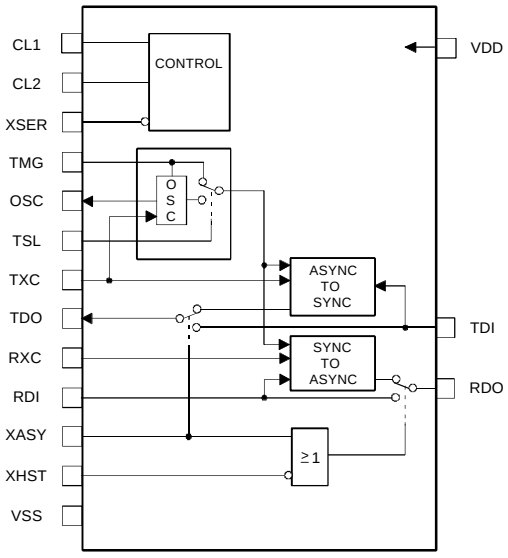
FEATURES

- Implements CCITT recommendation V.14
- Bypass operation
- Character length from 8 to 11 bits including start stop and parity bits
- CMOS and LS-TTL compatible interface
- Low power consumption (typically 10 mW)
- No additional circuitry needed to perform conversion
- Single +3.3...+5V supply
- Operating temperature -40°C to 85°C
- 16-pin PDIP and SO package

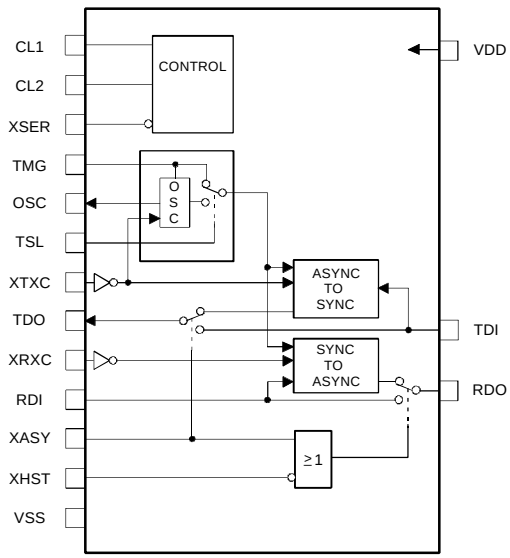
APPLICATION

- Data communication systems
- Adapts asynchronous terminals to synchronous modems
- Full or half card PC modems using UART as a data source
- Simplifying data multiplexing systems

BLOCK DIAGRAM



MAS9138

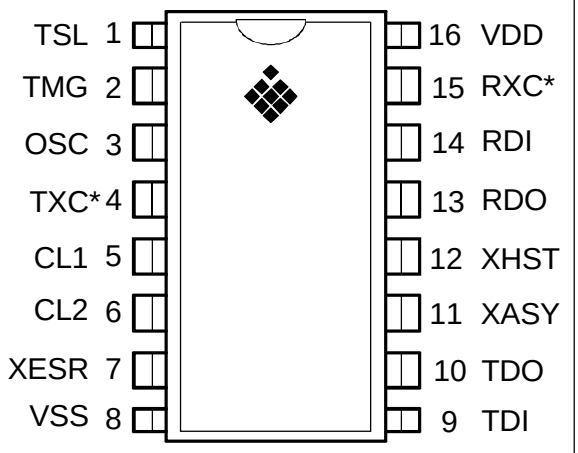


MAS9140

PIN CONFIGURATION

PDIP 16

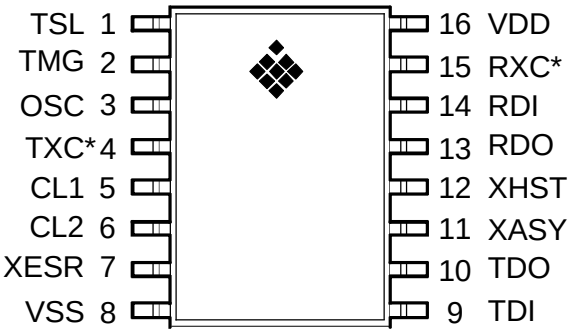
MAS9138/40N



* XTXC, XRXC for MAS9140N

SO16

MAS9138/40S



* XTXC, XRXC for MAS9140S

PIN DESCRIPTION

Pin name	Pin no.		I/O	Function
	PDIP	SO		
TSL	1	1	I	Timing select. 0 selects external sampling timing 16 x TXC from pin 2, TMG. 1 selects internal sampling timing.
TMG	2	2	I	Timing. Square wave timing signal 16 x TXC (TSL = 0) or 128 x TXCmax (TSL = 1). Max f = 10 Mhz when VDD = 5v and 5MHz when VDD = 3.3v.
OSC	3	3	O	Oscillator. Output for crystal. If used, the crystal is connected between pins 2 and 3.
TXC	4	4	I	Transmitter timing (MAS9138 only). Synchronous square wave timing for transmitter. The transmitted data output, TDO is synchronized to the rising edge of TXC. The duty cycle of TXC has to be 50% +/- 5%.
XTXC			I	Inverted transmitter timing (MAS9140 only). Synchronous square wave timing for transmitter. The transmitted data output, TDO is synchronized to the falling edge of XTXC. The duty cycle of XTXC has to be 50% +/- 5%.
CL1	5	5	I	Character length. The total character length including one start bit, one stop bit and possible parity bit is selected with the CL1 and CL2 signals.
CL2	6	6	I	
XESR	7	7	I	Extended signalling rate. The tolerance of the synchronous bit rate can be: XESR = 1 (basic signalling rate) TXC -2.5%...+1.0% XESR = 0 (extended signalling rate) TXC -2.5%...2.3%
VSS	8	8	G	Ground

PIN DESCRIPTION

Pin name	Pin no.		I/O	Function
	PDIP	SO		
TDI	9	9	I	Transmitter data input. 1 = mark or stop bit. 0 = space, start or break signal.
TDO	10	10	O	Transmitter data output. Output data is synchronized to the synchronous timing signal TXC (pin 4). 1 = mark. 0 = space.
XASY	11	11	I	Asynchronous mode. XASY = 0 Asynchronous transmission, XASY = 1 Synchronous transmission. In synchronous transmission the converter is totally bypassed in both directions: TDI = TDO, RDI = RDO
XHST	12	12	I	Higher speed signalling timing. XHST = 1 normal synchronous to asynchronous conversion (CCITT V.14). XHST = 0 asynchronous to synchronous conversion with higher speed synchronous timing (TXC, RXC). TXC and RXC timing must be 1-2% higher than the normal bit rate in order to allow some overspeed in the asynchronous data. On the receiver side the RX buffer is deleted and the synchronous data RDI is directly connected to the asynchronous output RDO.
RDO	13	13	O	Receiver data output. RDO is the received data converted back to asynchrnous mode. 1 = mark or stop bit, 0 = space, start or break signal
RDI	14	14	I	Receiver data input. 1 = mark, 0 = space. The received data must be synchronized to the receiver timing RXC from the synchronous channel (pin 15).
RXC	15	15	I	Receiver timing (MAS9138 only). Receiver square wave timing from the synchronous channel. The received data RDI must be synchronized to the rising edge of RXC.
XRXC			I	Receiver timing (MAS9140 only). Receiver square wave timing from the synchronous channel. The received data RDI must be synchronized to the rising edge of XRXC. Timings between synchronous clocks and data are shown on page five. Note that absolute delays depend on the speed of data transmission.
VDD	16	16	P	Power supply

ABSOLUTE MAXIMUM RATINGS

(GND = 0V)

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	VDD		-0.5	5.5	V
Storage Temperature	Ts		-55	+150	°C

RECOMMEDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD		3	3.3 to 5.0	5.25	V
Supply current	IDD	VDD = 5V	2		5	mA
Operating Temperature	Ta		-40		+85	°C

ELECTRICAL CHARACTERISTICS

◆ Inputs

(test conditions: -40°C to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage	V_{IL}	VDD=5V, VSS=0V			0.8	V
		VDD=3.3V, VSS=0V			0.4	V
Input high voltage	V_{IH}	VDD=5V, VSS=0V	2			V
		VDD=3.3V, VSS=0V	1.4			V
Input leakage current	I_{IL}	VDD=5V, VSS=0V		-100		µA
		VDD=3.3V, VSS=0V		-100		µA
Input capacitance load	C_I	VDD=5V, VSS=0V		1		pF
		VDD=3.3V, VSS=0V		1		pF
Internal pull-up resistor for digital inputs	$R_{pull-up}$	VDD=5V, VSS=0V, VIN=0.4V		150		kΩ
		VDD=5V, VSS=0V, VIN=2.5V		300		kΩ
		VDD=3.3V, VSS=0V, VIN=0.4V	200	275	350	kΩ
		VDD=3.3V, VSS=0V, VIN=1.5V	600	1000	1500	kΩ

ELECTRICAL CHARACTERISTICS

◆ Outputs (TDO, RDO)

(test conditions: -40°C to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output low voltage	V_{OL}	VDD=5V, VSS=0V, I_{OL}=+1.8mA			0.4	V
		VDD=3.3V, VSS=0V, I_{OL}=+0.6mA			0.2	V
Output high voltage	V_{OH}	VDD=5V, VSS=0V, I_{OL}=-4.3mA	3.0			V
		VDD=3.3V, VSS=0V, I_{OL}=-2.1mA	1.8			V

◆ Outputs (OSC)

(test conditions: -40°C to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output low voltage	V_{OL}	VDD=5V, VSS=0V, I_{OL}=+0.5mA			0.4	V
		VDD=3.3V, VSS=0V, I_{OL}=+0.19mA			0.2	V
Output high voltage	V_{OH}	VDD=5V, VSS=0V, I_{OL}=-1.4mA	3.0			V
		VDD=3.3V, VSS=0V, I_{OL}=-0.7mA	1.8			

◆ Data timing

(test conditions:VDD=3.3V - 5V, VSS=0V, -40°C to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low to high logic transition time	t_R	CL = 10pF		20		ns
High to low logic transition time	t_R	CL = 10 pF		20		ns

(test conditions:VDD=3.3V - 5V, VSS=0V, -40°C to 85°C, TSL = 1)

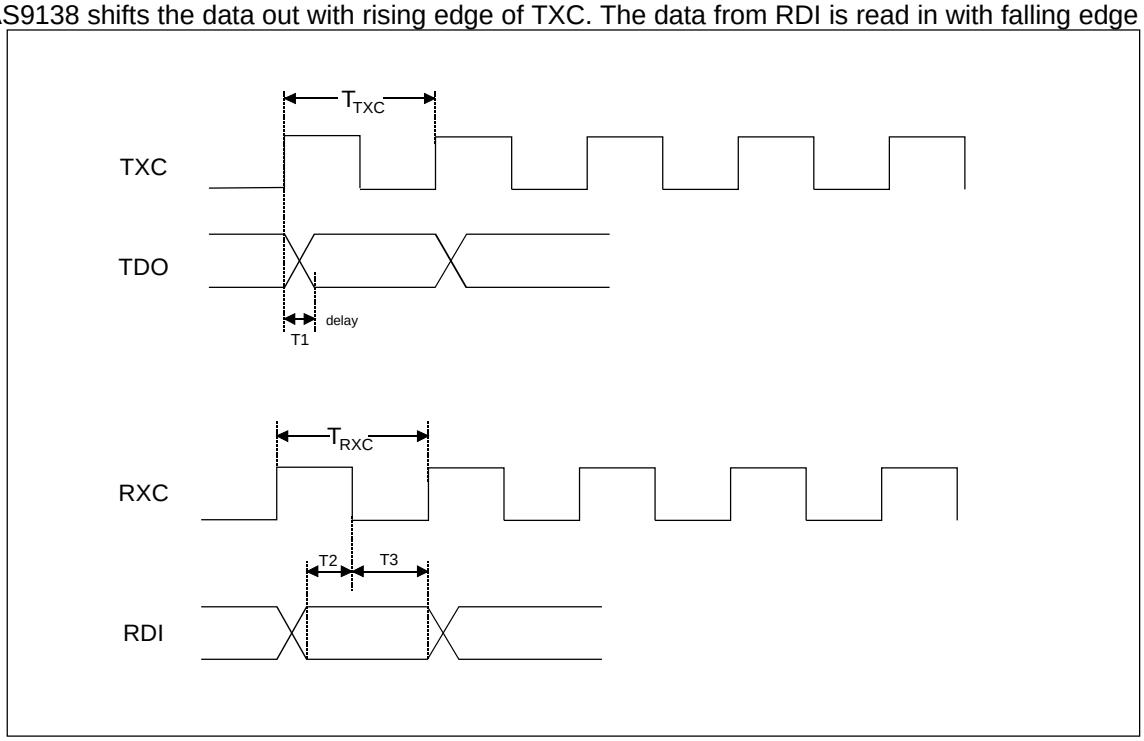
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TDO delay time after TXC	T1		50		T_{TXC}/16 + 350	ns
RDI setup time before RXC	T2		1/4 T_{RXC}			ns
RDI hold time after RXC	T3		1/4 T_{RXC}			ns

(test conditions:VDD=3.3V - 5V, VSS=0V, -40°C to 85°C, TSL = 0, TMG = 16xTXC)

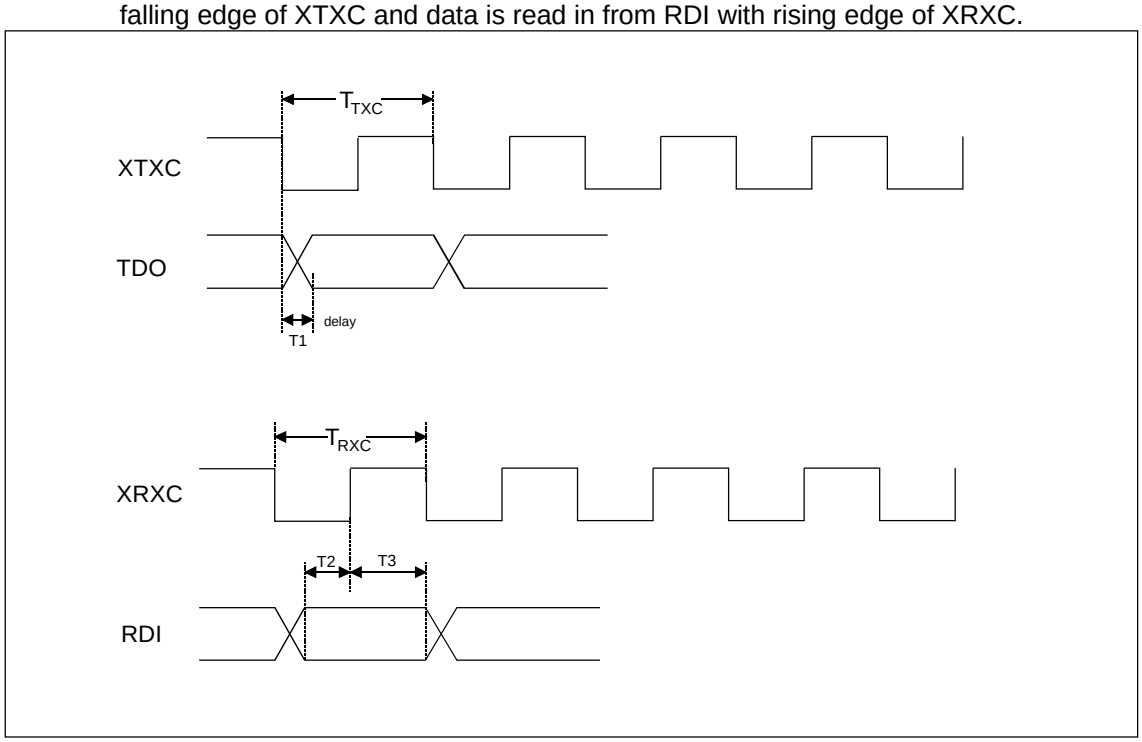
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TDO delay time after TXC	T1		50		1/TMG + 350	ns
RDI setup time before RXC	T2		1/4 T_{RXC}			ns
RDI hold time after RXC	T3		1/4 T_{RXC}			ns

TIMING DIAGRAMS

The MAS9138 shifts the data out with rising edge of TXC. The data from RDI is read in with falling edge of RXC.



The MAS9140 has inverted RXC and TXC clock inputs. The data is shifted out to TDO with falling edge of XTXC and data is read in from RDI with rising edge of XRXC.



FUNCTIONS

◆ **Asynchronous to synchronous converter**

The synchronous start-stop character, TDI (transmitter data input), is read into the Tx buffer. When the character is available the data bits are transferred as TDO (transmitter data output) with the synchronous timing signal TXC (transmitter clock). The bit rate of TDI must be the same as the TDO rate within -2.5%...+1% or -2.5%...+2.3% tolerance depending on XESR (extended signalling rate) signal. The transmitter adds extra stop bits to the synchronous data stream, if TDI is slower than TDO. The over speed is handled by deleting one stop bit in every 8th character at maximum in the synchronous output data TDO. When extended signal rate (XESR = 0) is used 4th stop bit may be deleted. When the transmitter detects a break signal(at least M bits of start polarity, where M is length of character), it sends 2M + 3 bits of start - polarity to TDO. If the break is longer than 2M + 3 bits, then all bits are transferred to TDO. After a break signal, at least 2M bits of stop polarity must be transmitted before sending further data.

◆ **Synchronous to asynchronous converter**

The synchronous RDI (receiver data input) is buffered to recognize the stop and start bits. If a missing stop bit is detected, it is added to the RDO (receiver data output). In this case the stop bits are shortened 12.5% (25% if XESR = 0) during each character. When the receiver gets at least 2M + 3 bits of start polarity, it does not add stop bits to RDO. This enables the break signal to go through the buffer.

◆ **Converting with higher speed timing**

An alternative method to handle the over speed in asynchronous data is to boost synchronous timing TXC and RXC by 1-2%. In this mode XHST (higer speed timing) = 0. In this case there is no need to delete any stop bits in the transmitter buffer. The break signal goes through unchanged. On the receiver side the synchronous data, RDI, is transferred directly to the asynchronous output RDO with RXC.

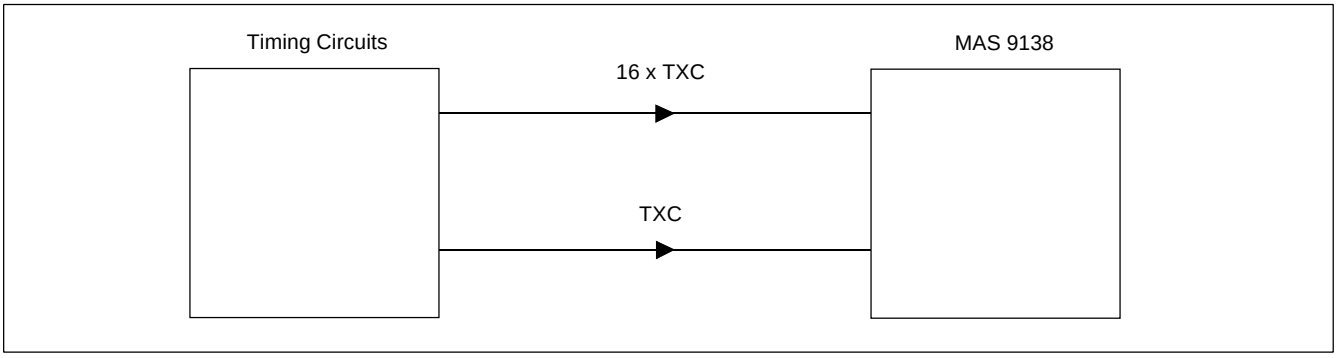
◆ **Timing selection**

The MAS9138 requires clock signals in order to function properly. The synchronous data transfer always requires the TXC clock. The clock is used internally for:

-shifting data out from the TX buffer (to pin TDO)

-detection of the bit rate in order to adjust the internal baud rate generator (only if TSL = 1)

The asynchronous data transfer (pins TDI, TDO) is accomplished by generating an internal timing signal for the asychronous circuits. This internal timing signal (16T) is 16 times the TXC bit rate in order to sample the asynchronous data stream (TDI) at the proper speed. The internal clock 16T is either generated from a crystal frequency by dividing it by 8, 16, 21 1/3, 25 3/5, 32, 42 2/3,64,128,256 or 512. Or it can also be generated externally and fed to pin TMG (TSL = 0). This is especially useful if the system already generates a clock which is 16 times the bit clock TXC as shown or if the bit rate is higher than 38.4 kHz. The divider is automatically selected by internal logic by measuring the TXC clock speed (TSL = 1). A crystal oscillator or a resonator can also be connected between pins 2 and 3. The crystal frequency should be 128 x TXCmax.



EXTERNALLY GENERATED 16T CLOCK

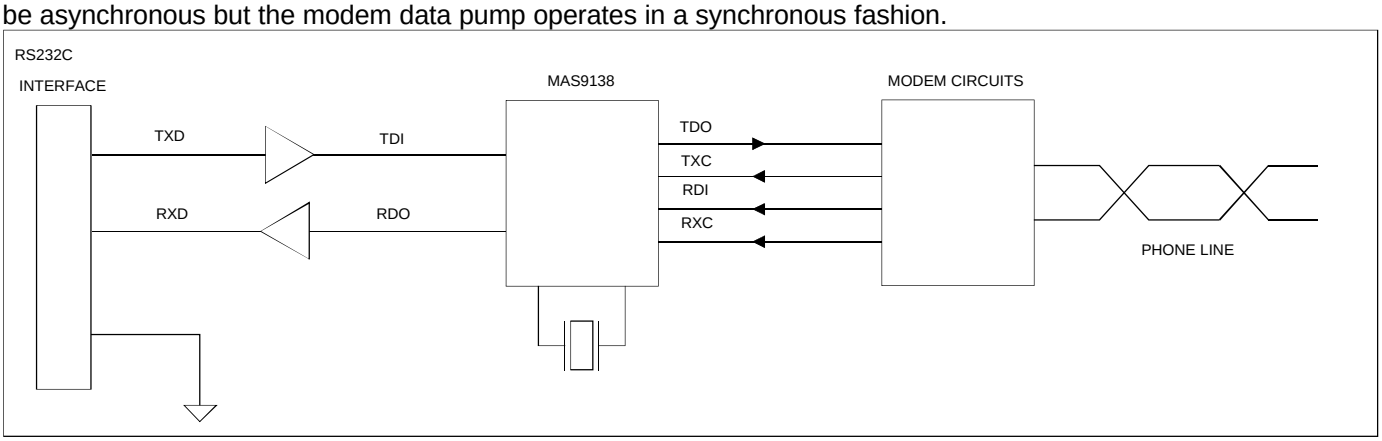
◆ **Character Length CL1,CL2**

CL1	CL2	Conditions
0	1	8 bits
0	0	9 bits
1	1	10 bits
1	0	11 bits

APPLICATION INFORMATION

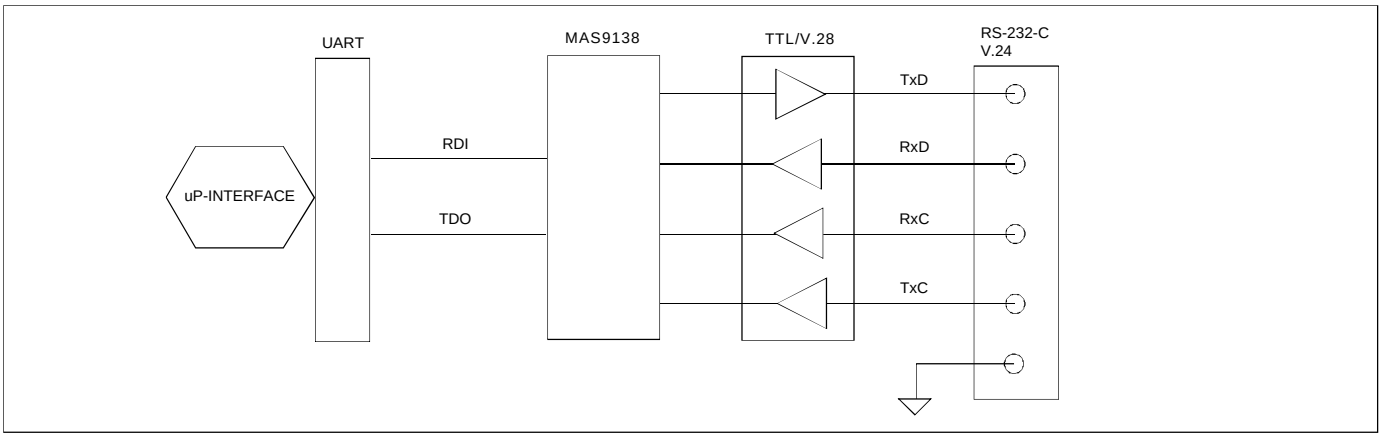
◆ Synchronous modem with asynchronous interface

The mAS9138 is intended for applications where an asynchronous and synchronous data source must be linked together. A typical case appears in a data modem where the terminal interface of the modem has been specified to be asynchronous but the modem data pump operates in a synchronous fashion.



◆ Synchronous serial interface with uP interface

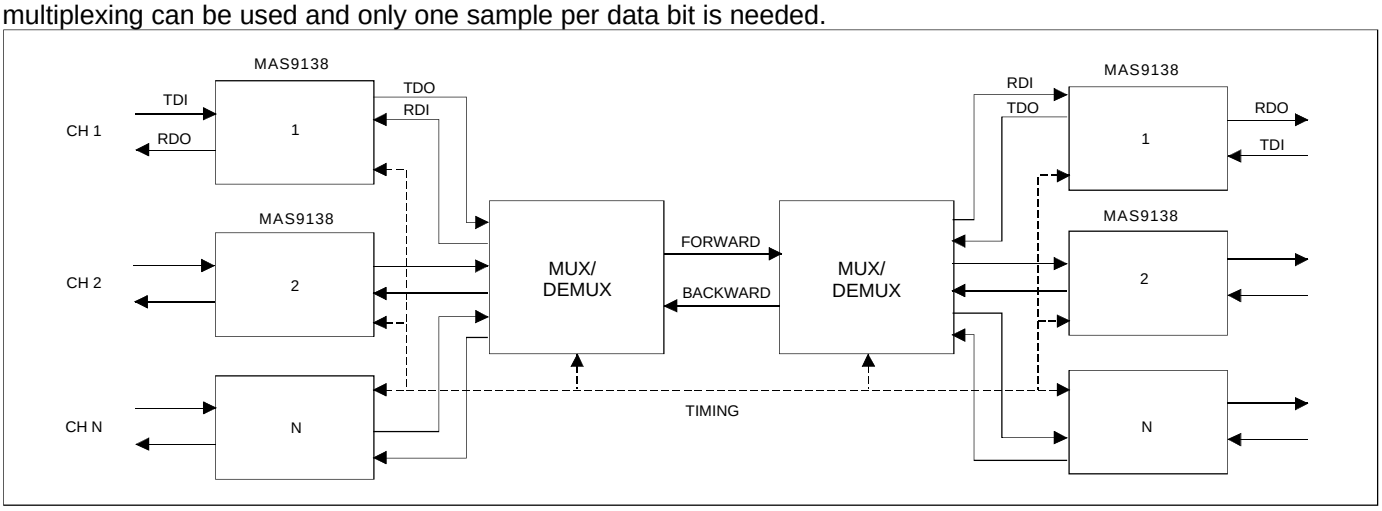
Another application is a synchronous serial interface for uP which uses UART as a data source. The concept is illustrated below.



APPLICATION INFORMATION

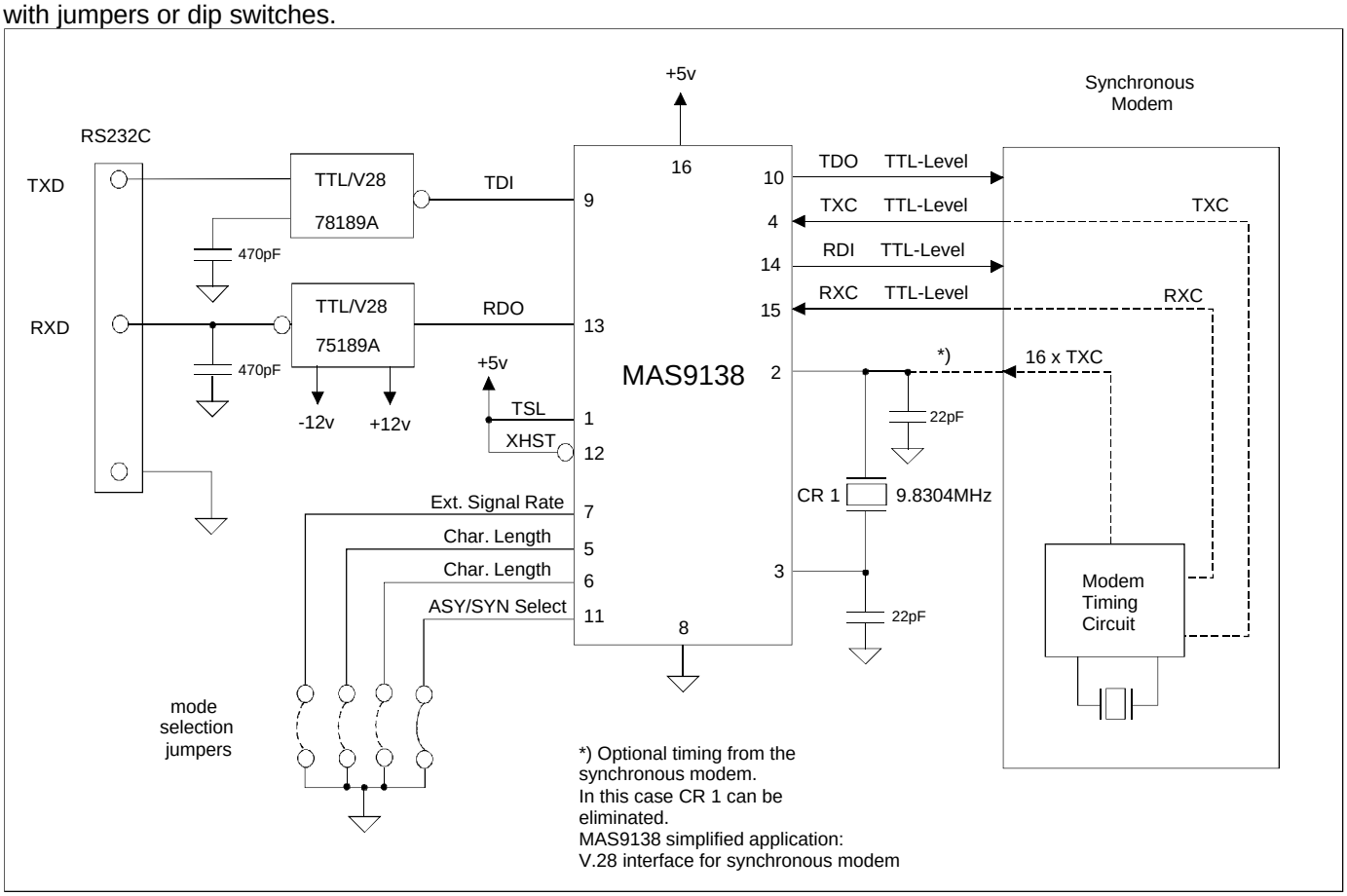
◆ Data multiplexer

A third application is a data multiplexing/demultiplexing system. The system accepts data from several sources. These data lines are sampled and the samples are sent through a multiplexer to a demultiplexer. To accomplish this, either a very high sample rate is needed or first convert the data to synchronous mode, where synchronous multiplexing can be used and only one sample per data bit is needed.



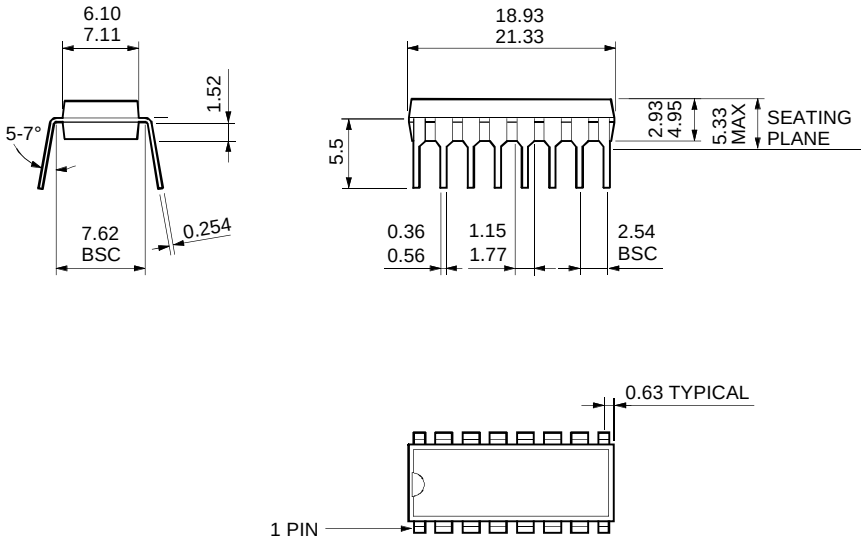
◆ Synchronous modem with asynchronous interface

The following application shows how to add an asynchronous interface to a synchronous modem with MAS9138. TSL and XHST inputs (pins 1 and 12) are connected to VDD. If the crystal is removed and the external 16 x TXC clock signal is used (dotted line) then tie the TSL input to ground. CL1, Cl2, XASY and XHST are user adjustable with jumpers or dip switches.



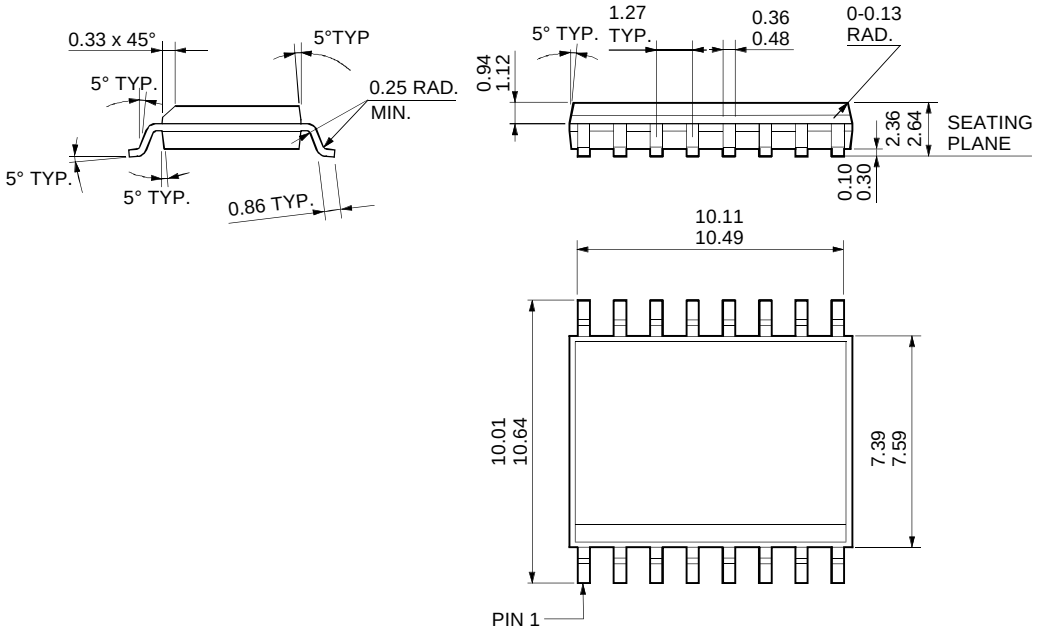
PACKAGE OUTLINES

16 LEAD PDIP OUTLINE (300 MIL BODY)



ALL MEASUREMENTS IN mm

16 LEAD SO OUTLINE (300 MIL BODY)



ALL MEASUREMENTS IN mm

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9138N		PDIP16	
MAS9138S		SO16	
MAS9140N		PDIP16	
MAS9140S		SO16	

LOCAL DISTRIBUTOR

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End of Data Sheet