19-1180; Rev 0; 6/98

MAXIM

Mobile-Radio Analog Controller

General Description

The MAX1007 is a multifunctional integrated circuit designed for high-performance mobile radios. It includes one 8-bit analog-to-digital converter (ADC), and two 7-bit and two 6-bit digital-to-analog converters (DACs) for functions including radio-frequency (RF) power sensing and antenna-diversity selection.

The ADC provides for power sense, receive-signal strength intensity (RSSI) measurements and system supervision. In the power-sense mode, the ADC converts the power-sensing circuitry signal (representing either the transmitted (Tx) or received (Rx) RF power) into a digital code, ensuring optimum Tx power setting and Rx signal analysis. An additional direct input to the ADC provides for system-supervision measurements, such as power-supply voltages, battery voltage, and temperature.

Four DAC blocks typically control DC levels in radios. As part of the Maxim PWT1900 chip set, the two 7-bit DACs control the gain settings and the two 6-bit DACs control the varactor diodes to tune a TCXO and bias a GaAs amplifier. Each DAC register and output can be updated independently, providing maximum flexibility.

For antenna diversity, a magnitude-comparison circuit captures and compares two peak signals. A latched logic-comparator output reveals which signal has the largest magnitude. The MAX1007 also includes an on-board voltage reference for the ADC and DACs.

The MAX1007 offers a high level of signal integrity with minimal power dissipation. Single-supply operation ranges from +2.85V to +3.6V. To further save power, there are two shutdown modes: standby and total shutdown. Standby is a partial shutdown that keeps the bandgap reference and the 2.4V reference generator active. Total shutdown disables all circuit blocks except the serial interface, reducing supply current to less than 1µA.

The MAX1007 is available in a 24-pin SSOP and is specified for commercial and extended temperature ranges.

Applications

PWT1900

Wireless Communications:

Cellular Radios PMR/SMR

PCS Radios WLL

Features

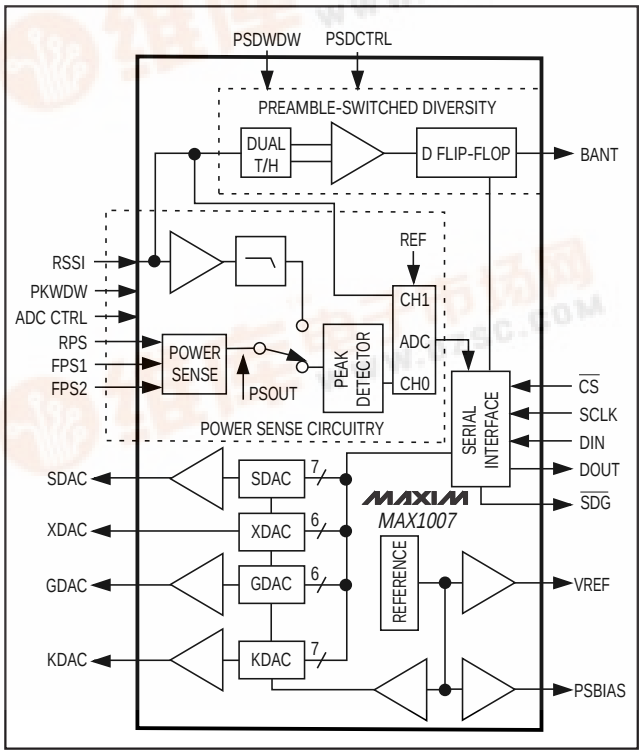
- **Multi-Input 8-Bit ADC**
- **Two 7-Bit DACs with Buffered Outputs**
- **Two 6-Bit DACs: Buffered/Unbuffered**
- **Power-Sense Conditioning Circuitry**
- **RSSI Measurement**
- **Antenna-Diversity Circuitry**
- **Internal Reference**
- **Serial-Logic Interface**
- **+2.85V to +3.6V Single-Supply Operation**
- **Two Shutdown Modes**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1007CAG	0°C to +70°C	24 SSOP
MAX1007EAG	-40°C to +85°C	24 SSOP

Pin Configuration appears at end of data sheet.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

AV_{DD} or DV_{DD} to AGND or DGND .....-0.3V to +6V
Digital Inputs to DGND .....-0.3V to +6V
Analog Inputs to AGND .....-0.3V to +6V
REF to AGND .....-0.3V to +6V
AGND to DGND .....± 0.3V
AV_{DD} to DV_{DD} .....± 0.3V
Maximum Current into Any Pin 50mA

Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 8.0mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX1007CAG .....0°C to +70°C
MAX1007EAG .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = +2.85V to +3.6V, f_{SCLK} = 1.152MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS					
Supply Voltages	AV_{DD}, DV_{DD}	2.85	3.0	3.6	V
SUPPLY CURRENTS [I(AV_{DD}) + I(DV_{DD})] (Note 1)					
Transmit Mode 1: All DACs, Ref, RefBuf Active	RxEN = 0, TxEN = 1; AV_{DD} = DV_{DD} = 3V; PKWDW = ADCCTRL = DGND		1.8	5.0	mA
Transmit Mode 2: All DACs, PGA, REF, Peak Detector, PSBIAS, I_{SOURCE}, RefBuf Active	RxEN = 0, TxEN = 1; AV_{DD} = DV_{DD} = 3V; PKWDW and ADCCTRL as per state B on Figure 1		4.7		mA
Transmit Mode 3: All DACs, PGA, REF, Peak Detector, PSBIAS, I_{SOURCE}, RefBuf, ADC Active	RxEN = 0, TxEN = 1; AV_{DD} = DV_{DD} = 3V; PKWDW and ADCCTRL as per state C on Figure 1		12.2	32	mA
Receive Mode 1: KDAC, XDAC, Ref, RefBuf Active	RxEN = 1, TxEN = 0; AV_{DD} = DV_{DD} = 3V; PKWDW = ADCCTRL = DGND		1.24	3.5	mA
Receive Mode 2: KDAC, XDAC, Peak Detector, RSSI Buffer, Ref, RefBuf Active	RxEN = 1, TxEN = 0; AV_{DD} = DV_{DD} = 3V; PKWDW and ADCCTRL as per state B on Figure 1		2.95		mA
Receive Mode 3: KDAC, XDAC, ADC, Peak Detector RSSI Buffer, Ref, RefBuf Active	RxEN = 1, TxEN = 0; AV_{DD} = DV_{DD} = 3V; PKWDW and ADCCTRL as per state C on Figure 1		11.2	31	mA
Receive Mode 4: KDAC, XDAC, ADC, RSSI Buffer, Ref, RefBuf, PSD Circuit Active	RxEN = 1, TxEN = 0; AV_{DD} = DV_{DD} = 3V; PKWDW and ADCCTRL as per state B on Figure 1. PSDWDW and PSD-CNTRL as per state D on Figure 2		4.07	10.5	mA
Standby: XDAC, GDAC, Ref, RefBuf Active	RxEN = 1, TxEN = 1; AV_{DD} = DV_{DD} = 3V		1.24	3.5	mA
Total Shutdown	RxEN = 0, TxEN = 0; AV_{DD} = DV_{DD} = 3V; ADCCTRL = PSDCTRL = PKWDW = PSDWDW = DGND; SCLK not active, either high or low		1	10	µA

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +2.85V to +3.6V, f_{SCLK} = 1.152MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
XDAC					
Resolution		6			Bits
Differential Nonlinearity	2 < code ≤ FS			±1	LSB
Integral Nonlinearity	2 < code ≤ FS		±1/2		LSB
Offset Error			±1		LSB
Gain Error	(Note 2)		±10		%FSR
Full-Scale Output Swing	No resistive load	2.1	2.42	2.75	V
Output Resistance			30		kΩ
GDAC					
Resolution		6			Bits
Differential Nonlinearity	2 < code ≤ FS			±1	LSB
Integral Nonlinearity	2 < code ≤ FS		±1		LSB
Offset Error	C_L = 30pF, R_L = 40kΩ		±1		LSB
Gain Error	(Note 2)		±10		%FSR
Output Slew Rate			0.1		V/µs
Full-Scale Output Swing	R_L = 40kΩ	2.1	2.42	2.75	V
Full-Scale Step Response Time	C_L = 30pF, R_L = 40kΩ, settling to 5% of final value		4		µs
SDAC, KDAC					
Resolution		7			Bits
Differential Nonlinearity	2 < code ≤ FS			±1	LSB
Integral Nonlinearity	2 < code ≤ FS		±1		LSB
Offset Error			±1		LSB
Gain Error	(Note 2)		±10		%FSR
Output Slew Rate	C_L = 30pF, R_L = 40kΩ		0.1		V/µs
Full-Scale Output Swing	R_L = 40kΩ	2.1	2.42	2.75	V
Full-Scale Step Response Time	C_L = 30pF, R_L = 40kΩ, settling to 2% of final value		4		µs
Power-Up Time from Standby	C_L = 30pF, R_L = 40kΩ, settling to within 2% of final value		4		µs
ADC					
Resolution		8			Bits
Input Signal Range		0		V_{REF}	V
Differential Nonlinearity	V_{REF} = 1.028V (typ)			±1	LSB
Integral Nonlinearity	V_{REF} = 1.028V (typ)		±1		LSB
Conversion Time				5.2	µs
Offset Error			±2		LSB
Gain Error	With respect to V_{REF}		±5		LSB
Reference Voltage			1.028		V
ADC Power-Up Time from Standby		1.74			µs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +2.85V to +3.6V, f_{SCLK} = 1.152MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RSSI CIRCUIT						
Lowpass-Filter Time Constant			10	20		µs
Minimum Peak Level Detected				100	300	mV
Maximum Peak Level Detected				V_{REF}		V
TRANSMIT POWER SENSE						
Offset Voltage		RPS, FPS1, FPS2 to ADC input		150		mV
Power-Sense Amp Gain (PGA)		Forward transmit		-0.53		V/V
		Reflected transmit, class 1		-6		
		Reflected transmit, classes 2, 3, 4		-0.44		
Current Source		Figure 3b	50	100	180	µA
Pull-Down Input Resistance		RPS, FPS1, FPS2 pulled to AGND when not selected		200		Ω
REFERENCE						
Output Voltage			0.96	1.028	1.1	V
PS Bias Voltage Output		R_S in series with C_L, C_L = 1nF, 200Ω ≤ R_S ≤ 1kΩ		1.87		V
PS Bias Sink Current			200			µA
Internal DAC Reference		R_S in series with C_L, C_L = 1nF, 200Ω ≤ R_S ≤ 1kΩ		2.42		V
SERIAL-LOGIC INTERFACE						
Digital Inputs ($\overline{CS}$, SCLK, DIN, PKWDW, ADCCTRL, PSDWDW, PSDCTRL)						
Input Voltage High	V_{IH}		0.7V_{DD}			V
Input Voltage Low	V_{IL}				0.3V_{DD}	V
Input Current	I_{IN}	Excluding PSDCTRL, PSDWDW			±1	µA
Input Resistance	R_{IN}	PSDCTRL, PSDWDW	20			kΩ
Inpt Capacitance	C_{IN}	Digital inputs			10	pF
Digital Outputs (DOUT, BANT, $\overline{SDG}$)						
Output Voltage High	V_{OH}	C_L = 20pF, R_L = 100kΩ	V_{DD} - 0.4			V
Output Voltage Low	V_{OL}	C_L = 20pF, R_L = 100kΩ			0.4	V
TIMING SPECIFICATIONS (Figure 4)						
DIN Valid to SCLK Setup	t_1		100			ns
DIN to SCLK Hold	t_2		0			ns
$\overline{CS}$ Low to SCLK High	t_3		20			ns
$\overline{CS}$ Low to DOUT Valid	t_4		100			ns
SCLK High to DOUT Valid	t_5				150	ns
SCLK Pulse Width High	t_6		200	434		ns
SCLK Pulse Width Low	t_7		200	434		ns
$\overline{CS}$ High to DOUT Disable	t_8	C_L = 20pF			100	ns
ADC Data Output Delay After End of ADC Conversion (Figure 4b)	t_9		500			ns

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +2.85V to +3.6V, f_{SCLK} = 1.152MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

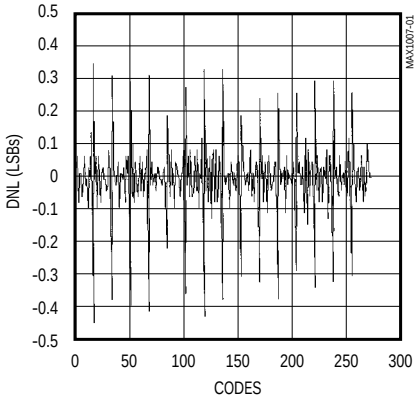
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADCCTRL Low to RF input	t_{10}	RF input on RSSI, RPS, FPS1, FPS2, or PSBIAS, (Figure 4c)		200		ns
PSDWDW Low to BANT Valid	t_{11}	C_L = 20pF (Figure 4c)		100		ns
SCLK Duty Cycle				50		%

Note 1: All digital inputs at DV_{DD} or DGND.
Note 2: All DACs use an internal reference voltage of 2.42V.

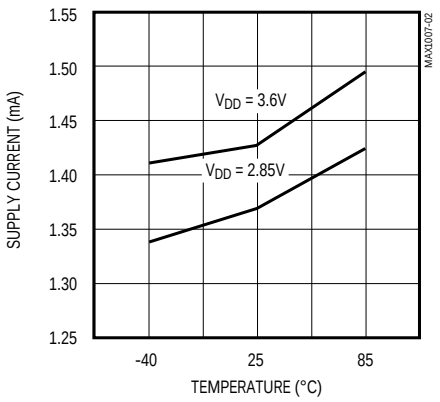
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

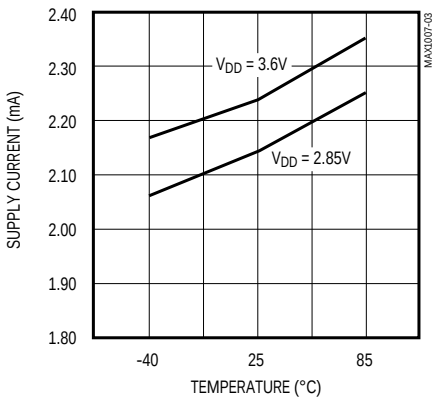
DIFFERENTIAL NONLINEARITY



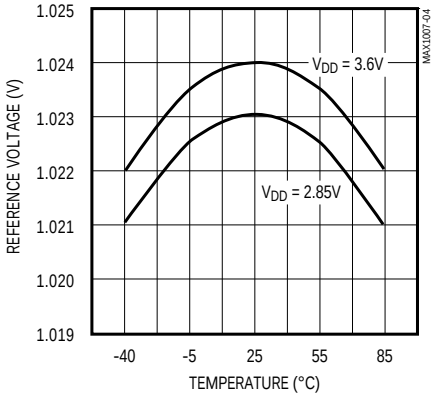
SUPPLY CURRENT vs. TEMPERATURE (Tx MODE)



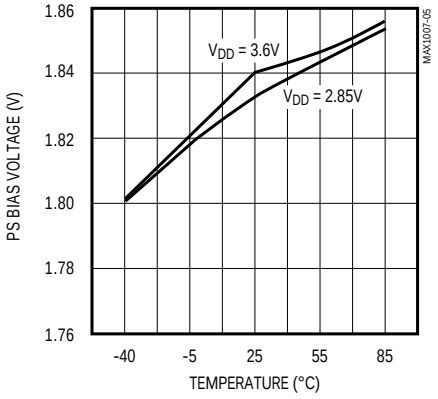
SUPPLY CURRENT vs. TEMPERATURE (Rx MODE)



REFERENCE VOLTAGE vs. TEMPERATURE



PS BIAS VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	RPS	Used to measure reverse-transmit power level. Only active in transmit mode when PKWDW = 1, SDAC[F/R] = Reverse. When not selected, this pin is internally pulled to AGND through a 200Ω switch.
2	FPS2	Used to measure forward power-sense class 2/3/4. Only active in transmit mode when GDAC[Power Class] = Class 2/3/4, PKWDW = 1, and SDAC[F/R] = Forward. When not selected, this pin is internally pulled to AGND through a 200Ω switch.
3	FPS1	Used to measure forward power-sense level 1. Only active in transmit mode when GDAC[Power Class] = Class 1, PKWDW = 1, and SDAC[F/R] = Forward. When not selected, this pin is internally pulled to AGND through a 200Ω switch.
4	SDAC	Buffered output of 7-bit DAC. Controls gain stage in up/down converter.
5	AV_{DD}	Analog Supply Voltage
6	XDAC	Unbuffered output of 6-bit DAC. Used to control VCXO frequency.
7	AGND	Analog Ground
8	REF	1.028V Reference Voltage Output
9	KDAC	Buffered output of 7-bit DAC. Controls gain stage in external modulator block.
10	GDAC	Buffered output of 6-bit DAC. Controls negative gate bias voltage of external power amplifier.
11	$\overline{SDG}$	Software-Programmable Logic Output. Can be used to shut down external bias generator.
12	BANT	Best-Antenna Digital Output. Result of preamble-switched diversity measurement (Figure 2). “0” indicates more power was sensed from period A with respect to period B. “1” means vice versa. Period A is sensed in the first 12 clock periods following the PSDWDW rising edge.
13	PSDCTRL	Preamble-Switched Diversity Measurement-Control Signal (Figure 2). This pin has a 20kΩ pull-down resistor to digital ground.
14	PSDWDW	Preamble-Switched Diversity Measurement Window (Figure 2). This pin has a 20kΩ pull-down resistor to digital ground.
15	ADCCTRL	RSSI/Power-Sense Measurement-Control Input (Figure 1)
16	PKWDW	RSSI/Power-Sense Measurement-Window Digital Input (Figure 1)
17	DOUT	Serial-Data Output. Enabled when $\overline{CS}$ is low.
18	DGND	Digital Ground
19	SCLK	Serial-Clock Input. Clock can be stopped and resumed at any time (40% to 60% duty cycle).
20	DV_{DD}	Digital Supply Voltage
21	DIN	Serial-Data Input
22	$\overline{CS}$	Chip Select Input. Enables serial interface when low.
23	PSBIAS	Power-Sense Measurement Buffered-Bias Output Voltage. Active only during power sensing.
24	RSSI	Received-Signal Strength Indicator Analog Input for power-sense and antenna diversity measurements. Signal goes into peak-detector circuit and is sampled at the end of the measurement window by the 8-bit ADC. Only active in receive mode when PKWDW = 1. Peak-detector circuit can be bypassed by using CH1 as the ADC input.

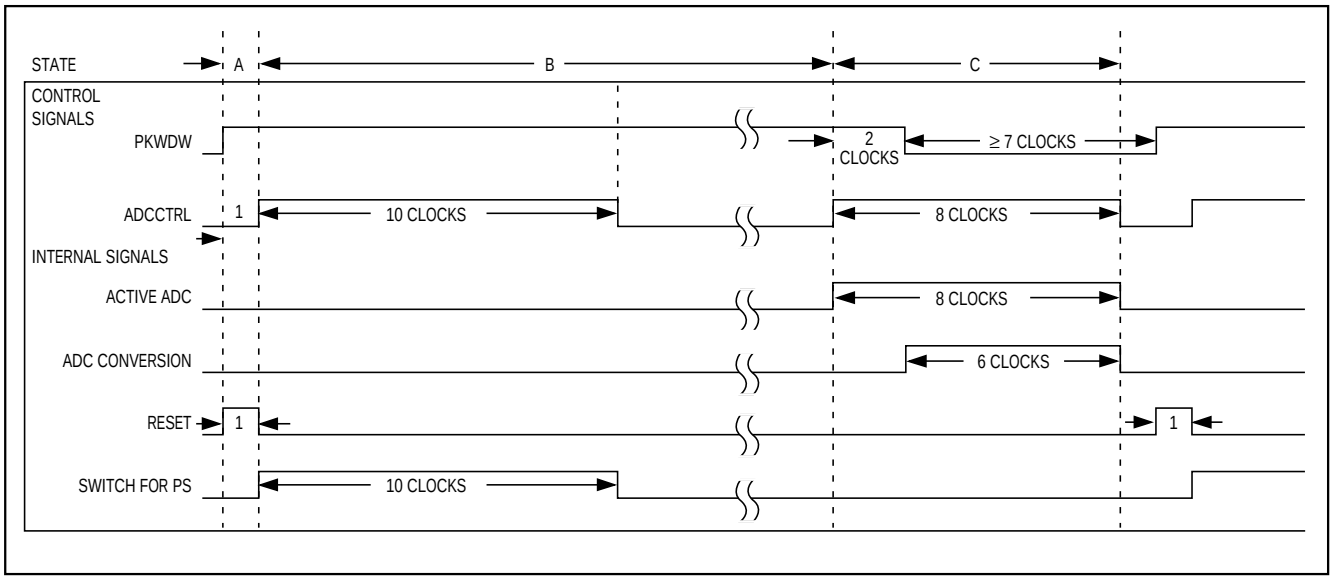


Figure 1. RSSI/Power-Sense Control Signals

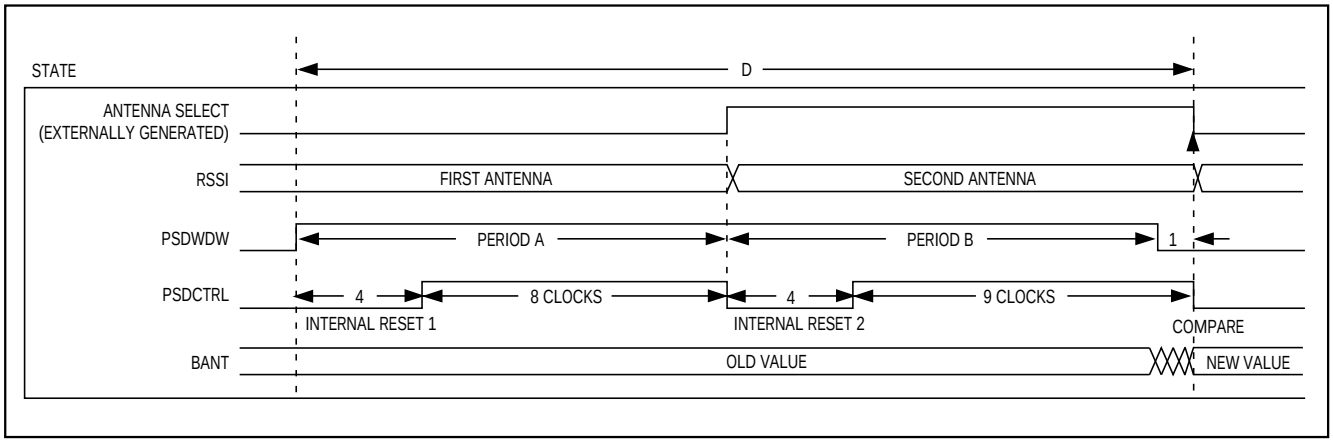


Figure 2. Antenna-Diversity Control Signals

Detailed Description

The MAX1007 comprises several blocks for measuring and controlling radio-frequency (RF) signals. The measurement blocks, including power sense, antenna or preamble-switched diversity, and the analog-to-digital converter (ADC), allow the comparison of various RF inputs. The control blocks, including four digital-to-analog converters (DACs), digital outputs BANT and $\overline{SDG}$, and the serial interface, aid frequency tuning and allow the optimization of transceiver gain under microprocessor control.

Power Sense

The power-sense circuit consists of a multiplexer (mux), a programmable gain amplifier (PGA), a peak detector, and a buffer. The circuit amplifies/attenuates the demodulated RF waveform, peak-holds the signal, and buffers the outputs to the ADC for power-sense measurement.

The demodulation process with external circuitry for one channel is shown in Figures 3a and 3b. This circuit typically recovers the negative envelope of the RF waveform. The 1.87V PSBIAS voltage and the 100µA current source are both generated by the MAX1007.

In Figure 3b, the mux selects the signal from one of three input channels: RPS, FPS1, and FPS2. The PGA then amplifies or attenuates the input signal according to the signal power-class level and the transmission mode (forward or reverse) (Table 1). Three gain settings are provided in the PGA: -0.53, -0.44, and -6. The voltage range at the internal node PSOUT is equal to the ADC's input range.

After the PGA, the signal is fed to a peak detector, which tracks the input and holds the positive peak voltage until the ADC starts a conversion.

Table 1. Data-Byte Definitions

A [2:0]	NAME	D [7:0]	DESCRIPTION
0 0 0	XDAC	Write [7,6]: [5:0]:	Reserved XDAC value [5:0]; LSB is bit 0, binary.
0 0 1	SDAC	Write [7]: [6:0]:	F/R bit, defines forward or reverse power-sense measurement 0 = Reverse power-sense measurement; RPS pin 1 = Forward power-sense measurement; FPS1/FPS2 pin SDAC value [6:0]; LSB is bit 0, binary.
0 1 0	KDAC	Write [7]: [6:0]:	ADC channel selection: 0 = Power sense or RSSI via peak-hold circuit connected to ADC (CH0) 1 = RSSI pin connected to ADC directly (CH1) KDAC value [6:0]; LSB is bit 0, binary.
0 1 1	GDAC	Write [7,6]: [6:0]:	Power class: 00 = Class 1 01 = Class 2 10 = Class 3 11 = Class 4 GDAC value [5:0]; LSB is bit 0, binary.
1 0 0			Reserved
1 0 1			Reserved
1 1 0			Reserved
1 1 1	ADC	Read [7:0]:	ADC value [7:0]; LSB is bit 0, binary.

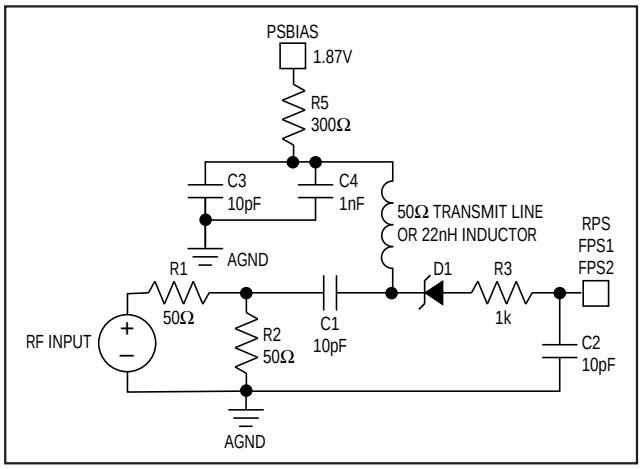


Figure 3a. External Circuit for Envelope Detection (one channel)

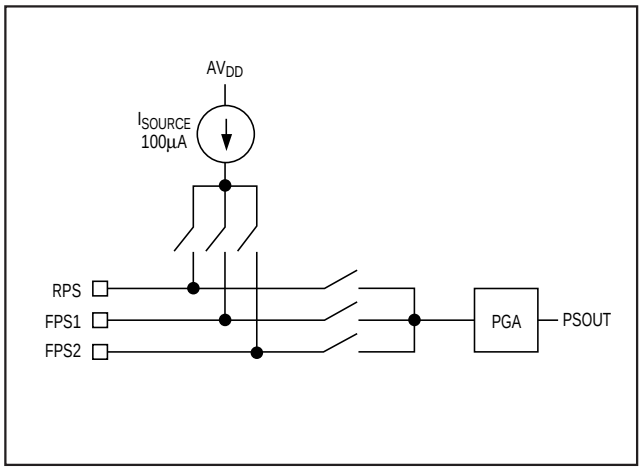


Figure 3b. Power-Sense Block

RSSI

The RSSI input provides a filtered input and a direct input to the ADC. The filtered signal path consists of a unity-gain buffer, an RC lowpass filter, and a peak detector to condition the signal for the ADC. The lowpass filter's time constant is 10µs (min). The mux at the ADC's input selects CH0 (filtered input) or CH1 (direct RSSI input).

Control Timing

The power-sense circuit is activated by the externally generated PKWDW signal (Figure 1) when the MAX1007 is either in transmit or receive mode. When the PKWDW signal goes high, the entire power-sense circuit turns on. However, since the PGA is active only in the transmit mode, it remains shut down during RSSI power measurements to conserve power.

Antenna Diversity

The antenna or preamble-switched diversity (PSD) circuit compares the signal amplitude presented at RSSI during two different time periods and latches the result at BANT (Best Antenna). The circuit consists of a dual track/hold (T/H) stage, a comparator, and an output latch (D flip-flop).

The comparison begins with the signal from the first antenna applied to the RSSI pin (Figure 2). PSDWDW goes high, and the PSD circuit is turned on. A power-on-reset signal initializes the D flip-flop so that it always starts with BANT low. After 4 clocks to reset the peak detector, PSDCTRL goes high to start the measurement. The T/H stage acquires the signal for 8 clocks while PSDCTRL is high, then holds the peak value while the second antenna is switched externally to the RSSI pin and the T/H is zeroed. PSDCTRL goes low for another 4 clocks, then goes high to enable the peak detector again. The peak detector is active for another 8 clocks while the output is compared with the peak value for the first antenna. When PSDWDW goes low at the end of the comparison phase, the comparator's output is clocked into the D flip-flop. The D flip-flop's output, BANT, is low if the first antenna signal is greater than the second, and high if the second signal is greater than the first. PSDCTRL goes low one clock period after PSDWDW goes low to power down the PSD circuitry.

Analog-to-Digital Converter

The ADC is an 8-bit, half-flash ADC with a T/H and two inputs (CH0, CH1). When selected, the acquisition time is 1.74µs. The ADC input range is equal to the 1.028V internal reference.

Reference

The bandgap voltage reference supports several blocks of the MAX1007. The nominal 1.21V output is scaled and buffered for the power-sense bias, the PGA, the ADC, and the DACs. The PSBIAS output voltage is 1.87V nominal. The ADC reference is 1.028V. It is buffered to isolate switching noise and to allow external capacitor bypassing (0.014µF to 0.05µF) for AC stability. A buffered gain supplies all DACs with a nominal 2.42V reference voltage.

Digital-to-Analog Converters

All four DAC outputs are reset to zero at power-up. Preset DACs to output voltages other than zero in total shutdown mode and update DACs by settling the LD bit in the command byte.

XDAC

XDAC is a 6-bit voltage-output DAC intended to drive varactor diodes to tune a voltage-controlled crystal oscillator. The input is double-buffered for independent updates. The inverted R-2R ladder output is unbuffered since the load is strictly capacitive. The maximum output voltage is 2.42V nominal, and the maximum output resistance is 30kΩ. The output is reset to zero at power-up and is active instantly. When XDAC is disabled, the DAC output is actively pulled to AGND.

GDAC

GDAC is a 6-bit voltage-output DAC intended to control an external negative bias generator, such as the MAX840, for a GaAs amplifier. The digital input is double-buffered. The inverted R-2R ladder output is buffered and can drive a 5kΩ load. The maximum output voltage is 2.42V nominal. The DAC output is reset to zero at power-up and is active in standby. A programmable logic output ($\overline{SDG}$) is provided to shut down the external bias generator.

SDAC and KDAC

SDAC and KDAC are 7-bit voltage-output DACs intended to tune power levels of an up/downconverter or a modulator. The digital inputs are double-buffered. The inverted R-2R ladder outputs are buffered and can drive 5kΩ loads. The maximum output voltage is 2.42V nominal. The SDAC and KDAC DAC outputs are reset to zero at power-up.

Serial-Interface and Control Logic

The serial interface is a 4-wire implementation with $\overline{CS}$, SCLK, and DIN inputs and a DOUT output. The hardware consists of a 7-bit command register, an 8-bit data input register, an 8-bit data output register, a counter, and control logic. Communication is framed in 16-bit words (8 command bits followed by 8 data bits)

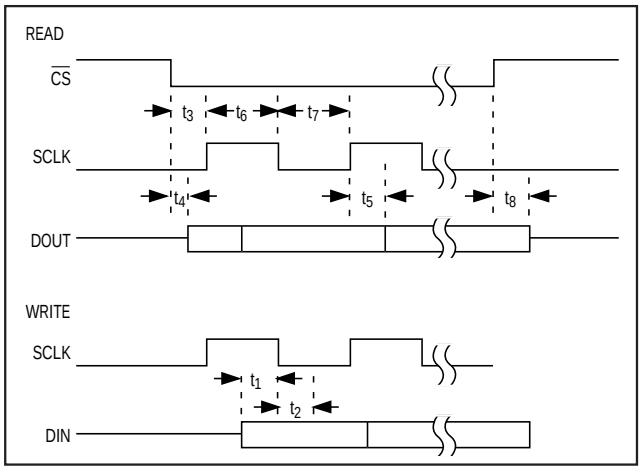


Figure 4a. Read/Write Detailed Interface Timing

by the counter. Data is clocked into DIN or the falling edge of SCLK, and is clocked out of DOUT on SCLK's rising edge. The serial interface is always active.

The SCLK and DIN idle state is low (Figure 4). The first "1" clocked in after $\overline{CS}$ goes low is the start bit, signifying the beginning of a 16-bit data word. The command and data input registers are cleared and the counter is started. The next 7 bits are latched in the command register.

Command Byte

The command byte (Figure 4d) consists of three address bits (A2, A1, A0), two power-mode bits (RxEN, TxEN), a shutdown control bit (SD), and a load data bit (LD). Table 1 lists the address and data-byte definitions.

SD is the software control for the GaAs FET bias generator shutdown pin and GDAC. Resetting SD to "0" causes $\overline{SDG}$ to go low and disables GDAC. The $\overline{SDG}$ output is updated if LD is set high.

LD is the software control to update the output registers. During a write operation, the addressed DAC's input buffer is updated. With LD reset to "0," the DAC register and DAC output remain unchanged. With LD set to "1," all DACs and power-class registers are simultaneously updated to the values in their input registers immediately after the last data bit (including DAC values, power-class bits, F/R bit, RSSI and ADC input selections, $\overline{SDG}$, and power-down bits).

After a 16-bit read cycle, pull $\overline{CS}$ high. The interface is now ready for a new command sequence. During a read operation, the ADC conversion result is output to DOUT. With LD set to "1," all other outputs and power-class registers are also updated.

Write Command

The 8 data bits are latched in the data input register. The command byte is decoded, and the data bits are transferred to the appropriate registers.

Read Command

After the command byte is decoded, the last 8 clocks output data, MSB first, from the ADC output register to DOUT (Figure 4b). After a 16-bit read cycle, pull $\overline{CS}$ high. The interface is now ready for a new command sequence.

To minimize the delay between the power-sense measurement and the ADC output, program a 'READ ADC' command prior to making the power-sense measurement and clock out the data as soon as the conversion is complete (Figure 4b). This reduces the delay by 8 clock cycles.

To minimize the delay between the power-sense measurement and the ADC output, program a "READ ADC" command prior to making the power-sense measurement and clock out the data as soon as the conversion is complete (Figure 4b). This reduces the delay by F clock cycles.

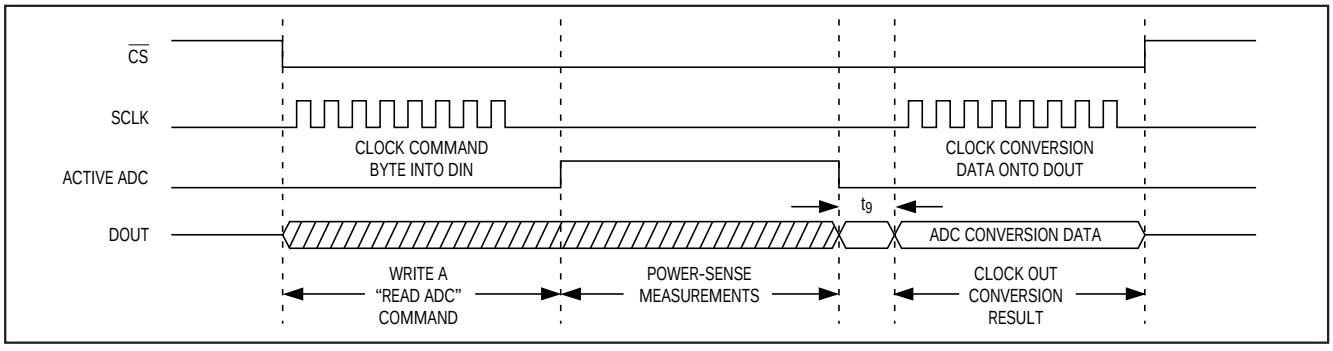


Figure 4b. Clock Command Conversion

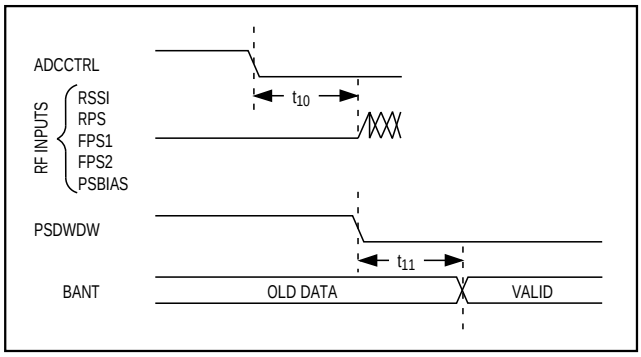


Figure 4c. Power-Sense/Best-Antenna Detailed Interface

Table 2. Power Modes

RxEN, TxEN	DESCRIPTION
0 0	Total shutdown
0 1	Transmit mode, all DACs enabled
1 0	Receive mode, SDAC and GDAC outputs disabled
1 1	Standby: REF, GDAC, and XDAC enabled. Rest of IC is shut down.

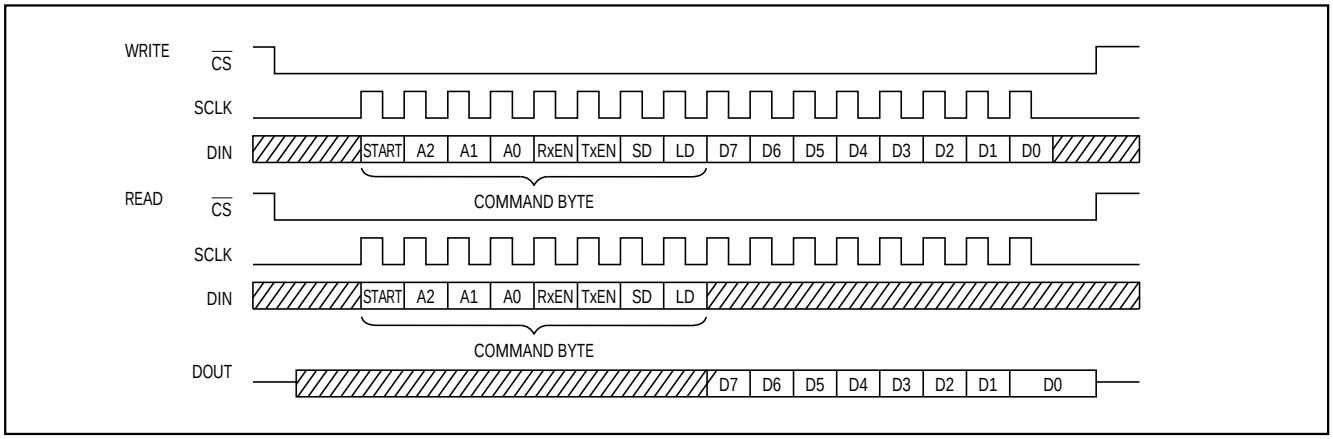


Figure 4d. Serial-Interface Timing

Applications Information

Precautions must be taken to minimize RF coupling through the IC.

Shutdown Modes

At power-up, the device initializes in total shutdown mode. The digital interface is always active. Table 2 describes the various power modes available.

When the PGA is not on (in shutdown, standby, or receive mode, or when PKWDW is low), the PS input pins (RPS, FPS1, FPS2) are pulled down to ground. To minimize RF coupling, the unselected channels are also pulled down to ground when the circuit is active. The current source and the 1.87V PSBIAS voltage generator are turned on only when the device is performing the transmit power-sense measurement.

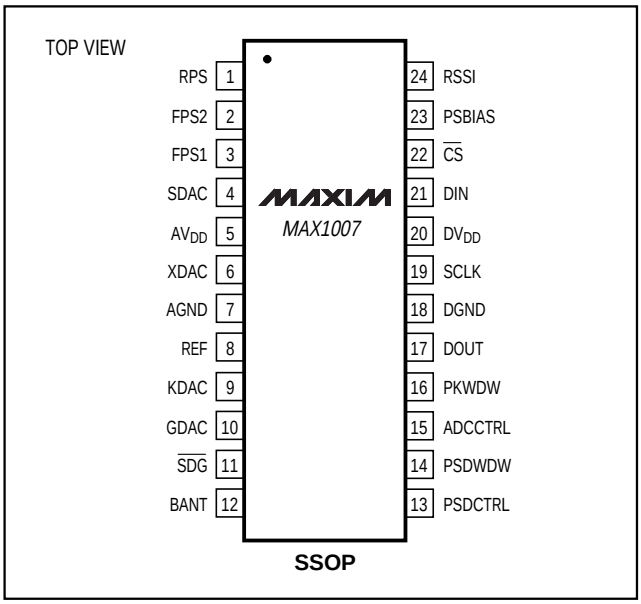
Power-Supply Bypassing and Ground Management

Optimum system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

Bypass AV_{DD} with a 0.1µF ceramic capacitor connected between AV_{DD} and AGND. Mount it with short leads close to the device. Similarly bypass DV_{DD} with a 0.1µF ceramic capacitor connected between DV_{DD} and DGND. Ferrite beads may also be used to further isolate the analog and digital power supplies.

Mobile-Radio Analog Controller

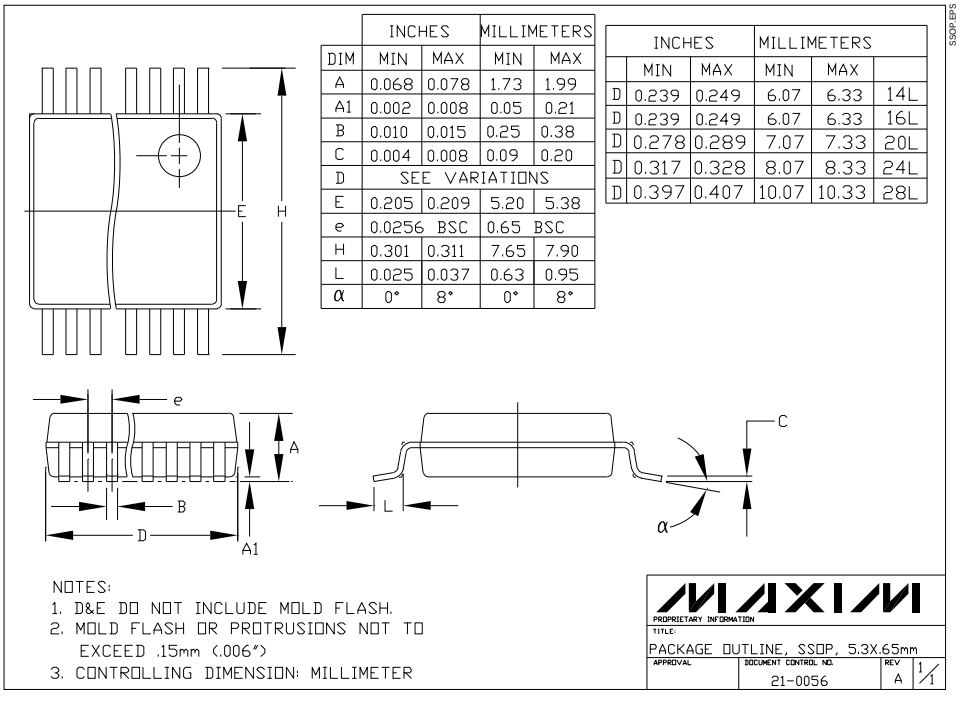
Pin Configuration



Chip Information

TRANSISTOR COUNT: 6744

Package Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L