19-2006; Rev 0; 5/01

MAXIM

Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

General Description

The MAX105 is a dual, 6-bit, analog-to-digital converter (ADC) designed to allow fast and precise digitizing of in-phase (I) and quadrature (Q) baseband signals. The MAX105 converts the analog signals of both I and Q components to digital outputs at 800Msps while achieving a signal-to-noise ratio (SNR) of typically 37dB with an input frequency of 200MHz, and an integral nonlinearity (INL) and differential nonlinearity (DNL) of ±0.25 LSB. The MAX105 analog input preamplifiers feature a 400MHz, -0.5dB, and a 1.5GHz, -3dB analog input bandwidth. Matching channel-to-channel performance is typically 0.04dB gain, 0.1LSB offset, and 0.2 degrees phase. Dynamic performance is 36.4dB signal-to-noise plus distortion (SINAD) with a 200MHz analog input signal and a sampling speed of 800MHz. A fully differential comparator design and encoding circuits reduce out-of-sequence errors, and ensure excellent metastable performance of only one error per 10^{16} clock cycles.

In addition, the MAX105 provides LVDS digital outputs with an internal 6:12 demultiplexer that reduces the output data rate to one-half the sample clock rate. Data is output in two's complement format. The MAX105 operates from a +5V analog supply and the LVDS output ports operate at +3.3V. The data converter's typical power dissipation is 2.6W. The device is packaged in an 80-pin, TQFP package with exposed paddle, and is specified for the extended (-40°C to +85°C) temperature range. For a lower-speed, 400Msps version of the MAX105, please refer to the MAX107 data sheet.

Applications

VSAT Receivers

WLANs

Test Instrumentation

Communications Systems

Pin Configuration appears at end of data sheet.

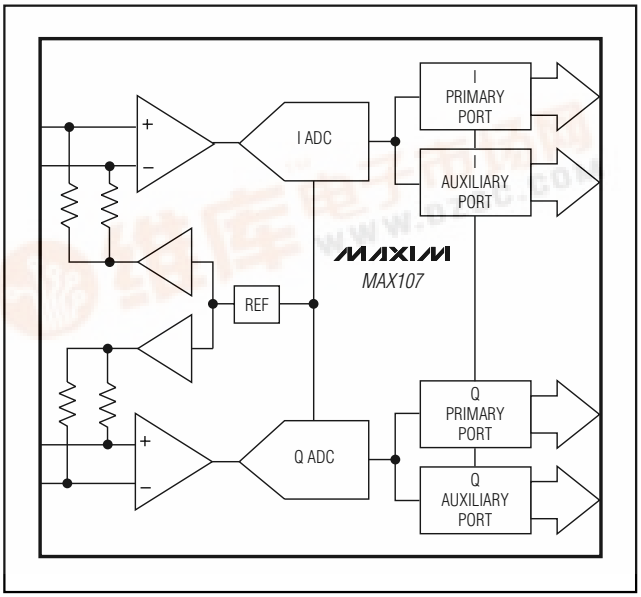
Features

- **Two Matched 6-Bit, 800Msps ADCs**
- **Excellent Dynamic Performance**
  36.4dB SINAD at $f_{IN} \approx$ 200MHz and $f_{CLK} \approx$ 800MHz
- **Typical INL and DNL: ±0.25LSB**
- **Channel-to-Channel Phase Matching: ±0.2°**
- **Channel-to-Channel Gain Matching: ±0.04dB**
- **6:12 Demultiplexer reduces the Data Rates to 400MHz**
- **Low Error Rate: 10^{16} Metastable States at 800Msps**
- **LVDS Digital Outputs in Two's Complement Format**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX105ECS	-40°C to +85°C	80-Pin TQFP-EP

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

AV_{CC}, $AV_{CC}I$, $AV_{CC}Q$ and $AV_{CC}R$ to AGND.....-0.3V to +6V
$OV_{CC}I$ and $OV_{CC}Q$ to OGND.....-0.3V to +4V
AGND to OGND ..... -0.3V to +0.3V
P0I± to P5I± and A0I± to A5I±
DREADY+, DREADY- to OGNDI.....-0.3V to $OV_{CC}I$+0.3V
P0Q± to P5Q±, A0Q± to A5Q±
DOR+ and DOR- to OGNDQ .....-0.3V to $OV_{CC}Q$+0.3V
REF to AGNDR.....-0.3V to $AV_{CC}R$+0.3V
Differential Voltage Between INI+ and INI- .....-2V, +2V
Differential Voltage Between INQ+ and INQ-.....-2V, +2V
Differential Voltage Between CLK+ and CLK- .....-2V, +2V
Maximum Current Into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
80-Pin TQFP (derate 44mW/°C above +70°C).....3.5W
Operating Temperature Range
MAX105ECS .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{CC} = $AV_{CC}I$ = $AV_{CC}Q$ = $AV_{CC}R$ = +5V, $OV_{CC}I$ = $OV_{CC}Q$ = +3.3V, AGND = AGNDI = AGNDQ = AGNDR = 0, OGNDI = OGNDQ = 0, f_{CLK} = 802.816MHz, C_L = 1µF to AGND at REF, R_L = 100Ω ±1% applied to digital LVDS outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution	RES		6			Bits
Integral Nonlinearity (Note 1)	INL		-1	±0.2	1	LSB
Differential Nonlinearity (Note 1)	DNL	No missing codes guaranteed	-1	±0.25	1	LSB
Offset Voltage	V_{OS}	(Note 2)	-1	±0.25	1	LSB
Offset Matching Between ADCs	OM	(Note 2)	-0.5	±0.1	0.5	LSB
ANALOG INPUTS (INI+, INI-, INQ+, INQ-)						
Input Open-Circuit Voltage	V_{AOC}		2.4	2.5	2.6	V
Input Open-Circuit Voltage Matching		$(V_{INI+} - V_{IN-}) - (V_{INQ+} - V_{INQ-})$			±7.5	mV
Common Mode Input Voltage Range (Note 3)	V_{CM}	Signal + Offset w.r.t. AGND	1.85		3.05	V
Full-Scale Analog Input Voltage Range (Note 4)	V_{FSR}		0.76	0.8	0.84	V_{p-p}
Input Resistance	R_{IN}		1.7	2		kΩ
Input Capacitance	C_{IN}			1.5		pF
Input Resistance Temperature Coefficient	TCR_{IN}			150		ppm/°C
Full-Power Analog Input BW	$FPBW_{-0.5dB}$			400		MHz
REFERENCE OUTPUT						
Reference Output Resistance	R_{REF}	Referenced to AGNDR		5		Ω
Reference Output Voltage	$\sqrt{REF}$	I_{SOURCE} = 500µA	2.45	2.50	2.55	V

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = $AV_{CC}I$ = $AV_{CC}Q$ = $AV_{CC}R$ = +5V, $OV_{CC}I$ = $OV_{CC}Q$ = +3.3V, AGND = AGNDI = AGNDQ = AGNDR = 0, OGNDI = OGNDQ = 0, f_{CLK} = 802.816MHz, C_L = 1µF to AGND at REF, R_L = 100Ω ±1% applied to digital LVDS outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CLOCK INPUTS (CLK+, CLK-)							
Clock Input Resistance	R_{CLK}	CLK+ and CLK- to AGND			5		kΩ
Clock Input Resistance Temperature Coefficient	TCR_{CLK}				150		ppm/°C
Minimum Clock Input Amplitude				500			mV_{p-p}
LVDS OUTPUTS (P0I± TO P5I±, P0Q± TO P5Q±, A0I± TO A5I±, A0Q± TO A5Q±, DREADY+, DREADY-, DOR+, DOR-)							
Differential Output Voltage	$\lvert V_{OD} \rvert$			247		400	mV
Change in Magnitude of $\lvert V_{OD} \rvert$ Between "0" and "1" States	$\Delta\lvert V_{OD} \rvert$					±25	mV
Steady-State Common Mode Output Voltage	$V_{OC(SS)}$			1.125		1.375	V
Change in Magnitude of V_{OC} Between "0" and "1" States	$\Delta\lvert V_{OC} \rvert$					±25	mV
Differential Output Resistance				80		160	Ω
Output Current		Short output together			2.5		mA
		Short to OGNDI = OGNDQ			25		
DYNAMIC SPECIFICATION							
Effective Number of Bits (Note 8)	ENOB	f_{IN} = 200.018MHz at -0.5dB FS (Note 9)	Differential	5.4	5.8		Bits
			Single-ended		5.75		
		f_{IN} = 400.134MHz at -0.5dB FS	Differential		5.65		
Signal-to-Noise Ratio (Notes 10, 11)	SNR	f_{IN} = 200.018MHz at -0.5dB FS (Note 9)	Differential	35	37		dB
			Single-ended		36.7		
		f_{IN} = 400.134MHz at -0.5dB FS	Differential		36.5		
Total Harmonic Distortion (Note 11)	THD	f_{IN} = 200.018MHz at -0.5dB FS (Note 9)	Differential		-44.5	-41	dBc
			Single-ended		-44.5		
		f_{IN} = 400.134MHz at -0.5dB FS	Differential		-41		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 200.018MHz at -0.5dB FS (Note 9)	Differential	41	45		dB
			Single-ended		45		
		f_{IN} = 400.134MHz at -0.5dB FS	Differential		41.5		

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ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = $AV_{CC}I$ = $AV_{CC}Q$ = $AV_{CC}R$ = +5V, $OV_{CC}I$ = $OV_{CC}Q$ = +3.3V, AGND = AGNDI = AGNDQ = AGNDR = 0, OGNDI = OGNDQ = 0, f_{CLK} = 802.816MHz, C_L = 1µF to AGND at REF, R_L = 100Ω ±1% applied to digital LVDS outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Signal-to-Noise Plus Distortion Ratio	SINAD	f_{IN} = 200.018MHz at -0.5dB FS (Note 9)	Differential	34	36.4		dB
			Single-ended		36.1		
		f_{IN} = 400.134MHz at -0.5dB FS	Differential		35.2		
Two-Tone Intermodulation	TTIMD	f_{IN1} = 124.1660MHz, f_{IN2} = 126.1260MHz at -7dBFS			-52		dBc
Crosstalk Between ADCs	XTLK	f_{INI} = 200.0180MHz, f_{INQ} = 210.0140MHz at -0.5dB FS			-70		dB
Gain Match Between ADCs	GM	(Note 12)		-0.3	±0.04	+0.3	dB
Phase Match Between ADCs	PM	(Note 12)		-2	±0.2	+2	deg
Metastable Error Rate				Less than 1 in 10^{16}			Clock Cycles
POWER REQUIREMENTS							
Analog Supply Voltage	$AV_{CC\_}$	AV_{CC} = $AV_{CC}I$ = $AV_{CC}Q$ = $AV_{CC}R$			5 ±5%		V
Digital Supply Voltage	$OV_{CC\_}$	$OV_{CC}I$ = $OV_{CC}Q$			3.3 ±10%		V
Analog Supply Current	I_{CC}	I_{CC} = $AI_{CC}R$ + $AI_{CC}I$ + $AI_{CC}Q$ + AI_{CC}			250	320	mA
Output Supply Current	OI_{CC}	OI_{CC} = $OI_{CC}I$ + $OI_{CC}Q$			400	510	mA
Analog Power Dissipation	P_{DISS}				2.6		W
Common-Mode Rejection Ratio	CMRR	V_{IN_+} = V_{IN_-} = ±0.1V (Note 6)		40	60		dB
Power-Supply Rejection Ratio	PSRR	AV_{CC} = $AV_{CC}I$ = $AV_{CC}Q$ = $AV_{CC}R$ = +4.75V to +5.25V (Note 7)		40	57		dB
TIMING CHARACTERISTICS							
Maximum Sample Rate	f_{MAX}			800			Msps
Clock Pulse Width Low	t_{PWL}			0.56			ns
Clock Pulse Width High	t_{PWH}			0.56			ns
Aperture Delay	t_{AD}				100		ps
Aperture Jitter	t_{AJ}				1.5		ps_{RMS}
CLK-to-DREADY Propagation Delay	t_{PD1}	(Note 13)			1.5		ns
DREADY-to-DATA Propagation Delay	t_{PD2}	(Notes 5, 13)		0	120	300	ps

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = $AV_{CC}I$ = $AV_{CC}Q$ = $AV_{CC}R$ = +5V, $OV_{CC}I$ = $OV_{CC}Q$ = +3.3V, AGND = AGNDI = AGNDQ = AGNDR = 0, OGNDI = OGNDQ = 0, f_{CLK} = 802.816MHz, C_L= 1µF to AGND at REF, R_L = 100Ω ±1% applied to digital LVDS outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DREADY Duty Cycle		(Notes 5, 13)	47		53	%
LVDS Output Rise-Time	t_{RDATA}	20% to 80% (Notes 5, 13)	200		500	ps
LVDS Output Fall-Time	t_{FDATA}	20% to 80% (Notes 5, 13)	200		500	ps
LVDS Differential Skew	t_{SKEW1}	Any differential pair		<65		ps
		Any two LVDS output signals except DREADY		<100		ps
DREADY Rise-Time	$t_{RDREADY}$	20% to 80% (Notes 5, 13)	200		500	ps
DREADY Fall-Time	$t_{FDREADY}$	20% to 80% (Notes 5, 13)	200		500	ps
Primary Port Pipeline Delay	t_{PDP}			5		Clock Cycles
Auxiliary Port Pipeline Delay	t_{PDA}			6		Clock Cycles

Note 1: NL and DNL is measured using a sine-histogram method.
Note 2: Input offset is the voltage required to cause a transition between codes 0 and -1.
Note 3: Numbers provided are for DC-coupled case. The user has the choice of AC-coupling, in which case, the DC input voltage level does not matter.
Note 4: The peak-to-peak input voltage required, causing a full-scale digitized output when using a trigonometric curve-fitting algorithm (e.g. FFT).
Note 5: Guaranteed by design and characterization.
Note 6: Common-mode rejection ratio is defined as the ratio of the change in the offset voltage to the change in the common-mode voltage expressed in dB.
Note 7: Measured with analog power supplies tied to the same potential.
Note 8: Effective number of bits (ENOB) is computed from a curve-fit referenced to the theoretical full-scale range.
Note 9: The clock and input frequencies are chosen so that there are 2041 cycles in an 8,192-long record.
Note 10: Signal-to-noise-ratio (SNR) is measured both with the other channel idling and converting an out-of-phase signal. The worst case number is presented. Harmonic distortion components two through five are excluded from the noise.
Note 11: Harmonic distortion components two through five are included in the total harmonic distortion specification.
Note 12: Both I and Q inputs are effectively tied together (e.g. driven by power splitter). Signal amplitude is -0.5dB FS at an input frequency of f_{IN} = 200.0180 MHz.
Note 13: Measured with a differential probe, 1pF capacitance.

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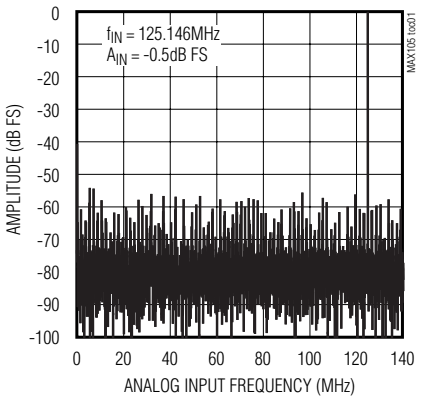
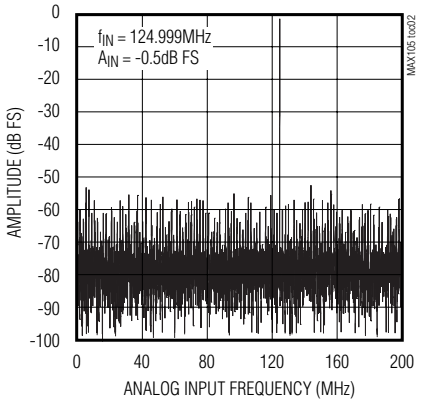
Typical Operating Characteristics

(AV_{CC} = $AV_{CC}I$ = $AV_{CC}Q$ = $AV_{CC}R$ = +5V, $OV_{CC}I$ = $OV_{CC}Q$ = +3.3V, AGND = AGNDI = AGNDQ = AGNDR = 0, OGNDI = OGNDQ = 0, f_{CLK} = 802.816MHz, differential input at -0.5dB FS, C_L = 1µF to AGND at REF, R_L = 100Ω ±1% applied to digital LVDS outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

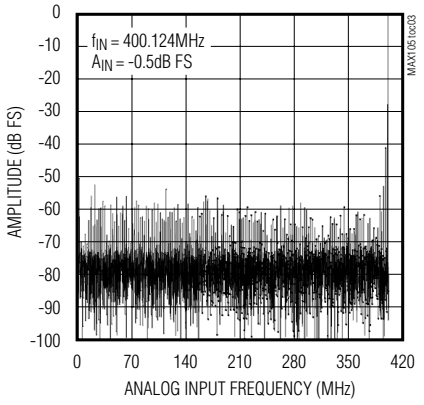
8192-POINT FFT, DIFFERENTIAL INPUT



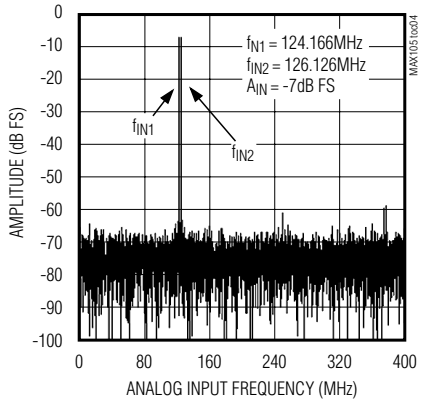
8192-POINT FFT, DIFFERENTIAL INPUT



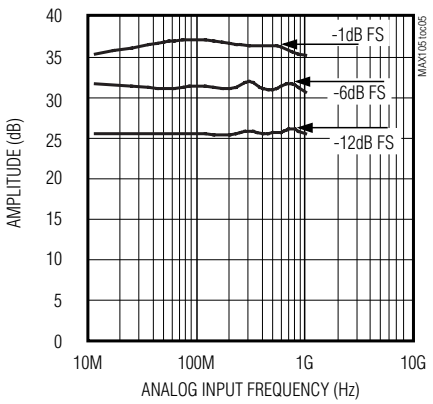
8192-POINT FFT, DIFFERENTIAL INPUT



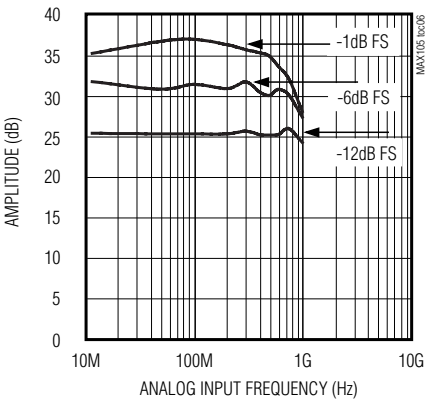
TWO-TONE IMD (8192-POINT RECORD), DIFFERENTIAL INPUT



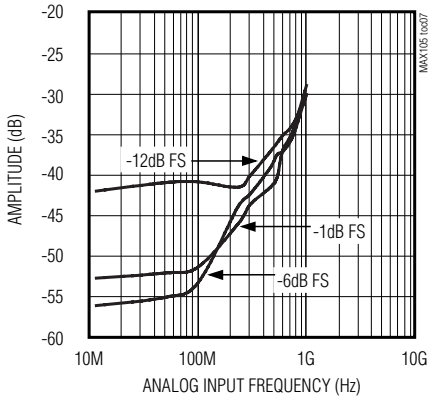
SNR vs. ANALOG INPUT FREQUENCY, DIFFERENTIAL INPUT



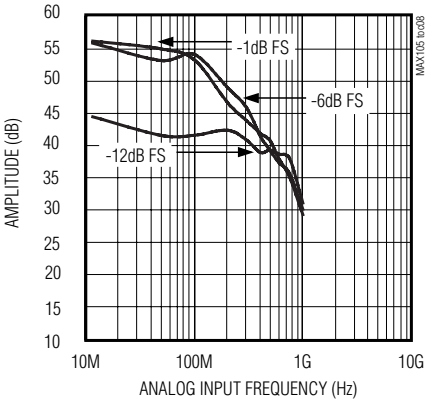
SINAD vs. ANALOG INPUT FREQUENCY, DIFFERENTIAL INPUT



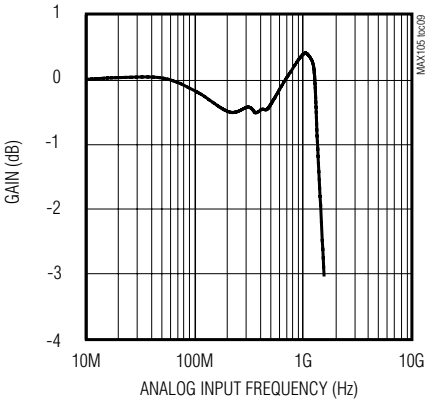
THD vs. ANALOG INPUT FREQUENCY, DIFFERENTIAL INPUT



SFDR vs. ANALOG INPUT FREQUENCY, DIFFERENTIAL INPUT



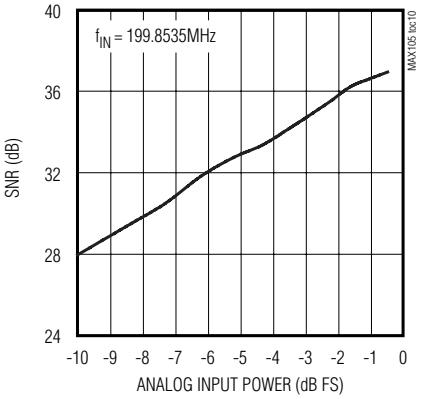
FULL-POWER INPUT BANDWIDTH SINGLE-ENDED INPUT



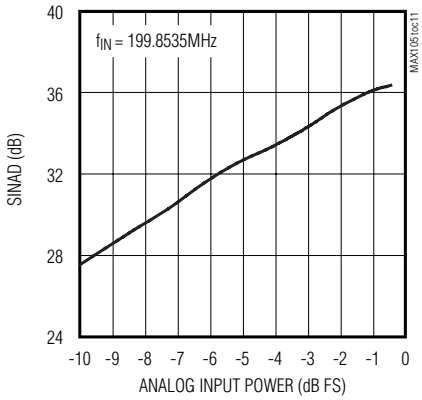
Typical Operating Characteristics (continued)

(AV_{CC} = $AV_{CC}I$ = $AV_{CC}Q$ = $AV_{CC}R$ = +5V, $OV_{CC}I$ = $OV_{CC}Q$ = +3.3V, AGND = AGNDI = AGNDQ = AGNDR = 0, OGNDI = OGNDQ = 0, f_{CLK} = 802.816MHz, differential input at -0.5dB FS, C_L = 1µF to AGND at REF, R_L = 100Ω ±1% applied to digital LVDS outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

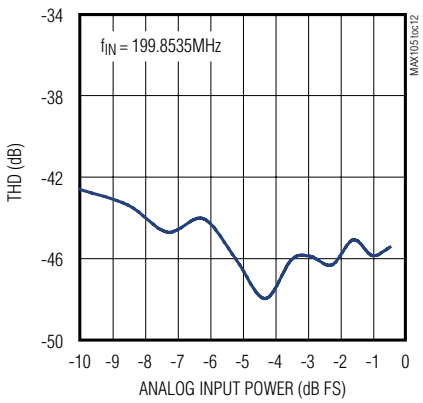
SNR vs. ANALOG INPUT POWER, DIFFERENTIAL INPUT



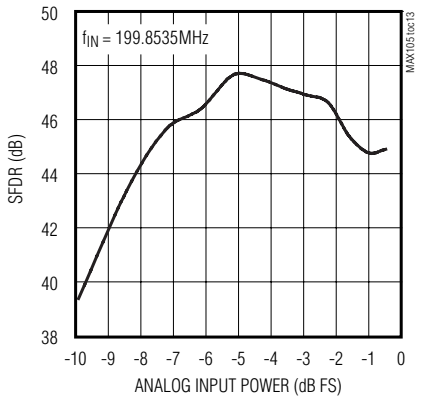
SINAD vs. ANALOG INPUT POWER, DIFFERENTIAL INPUT



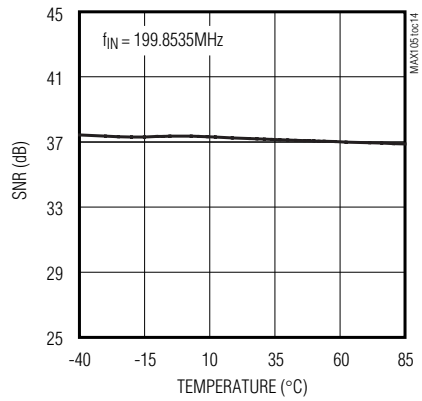
THD vs. ANALOG INPUT POWER, DIFFERENTIAL INPUT



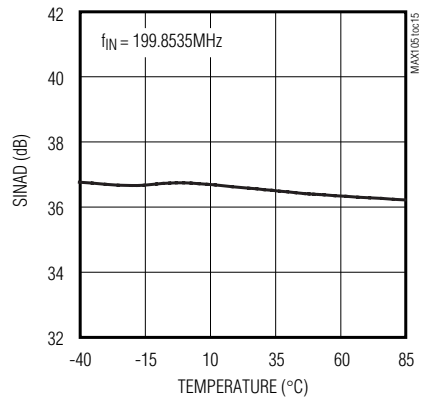
SFDR vs. ANALOG INPUT POWER, DIFFERENTIAL INPUT



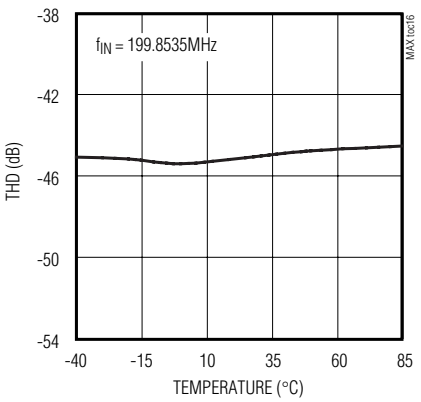
SNR vs. TEMPERATURE



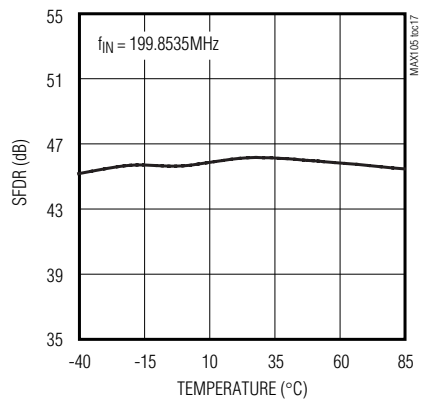
SINAD vs. TEMPERATURE



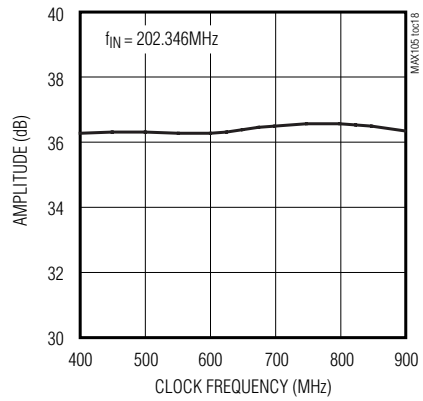
THD vs. TEMPERATURE



SFDR vs. TEMPERATURE



SNR vs. CLOCK FREQUENCY, DIFFERENTIAL INPUT (-1dB FS)

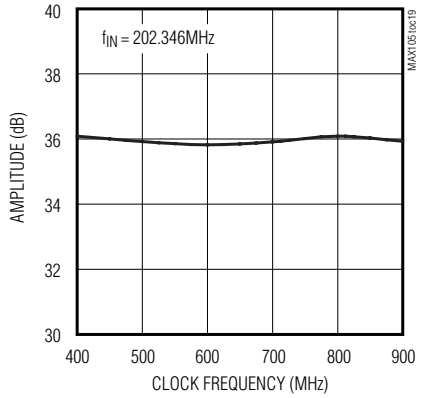


Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

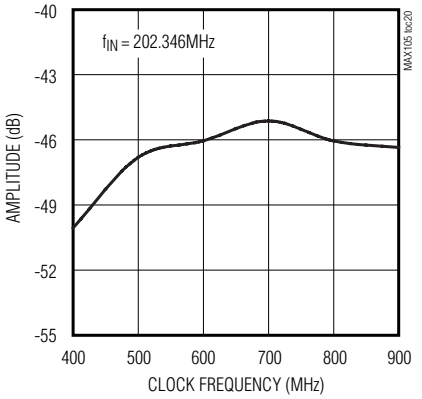
Typical Operating Characteristics (continued)

(AV_{CC} = $AV_{CC}I$ = $AV_{CC}Q$ = $AV_{CC}R$ = +5V, $OV_{CC}I$ = $OV_{CC}Q$ = +3.3V, AGND = AGNDI = AGNDQ = AGNDR = 0, OGNDI = OGNDQ = 0, f_{CLK} = 802.816MHz, differential input at -0.5dB FS, C_L = 1µF to AGND at REF, R_L = 100Ω ±1% applied to digital LVDS outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

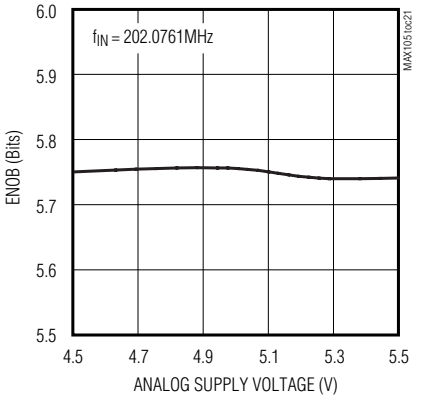
SINAD vs. CLOCK FREQUENCY, DIFFERENTIAL INPUT (-1dB FS)



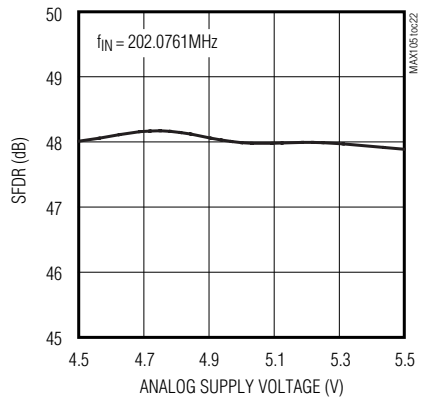
THD vs. CLOCK FREQUENCY, DIFFERENTIAL INPUT (-1dB FS)



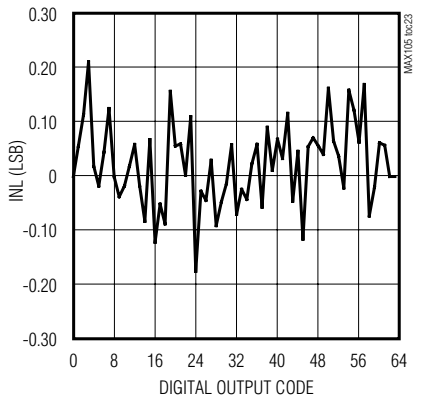
ENOB vs. ANALOG SUPPLY VOLTAGE, DIFFERENTIAL INPUT (-1dB FS)



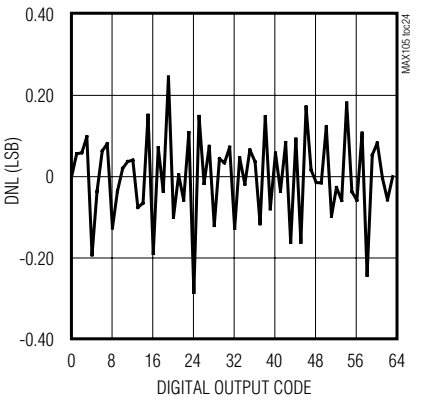
SFDR vs. ANALOG SUPPLY VOLTAGE, DIFFERENTIAL INPUT (-1dB FS)



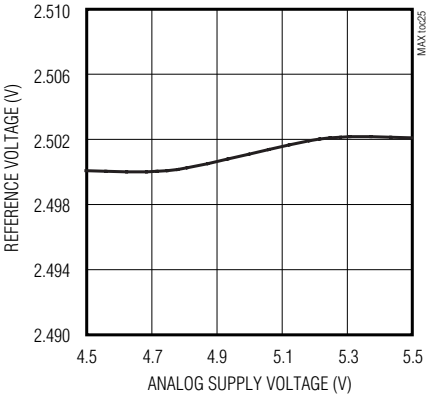
INL vs. DIGITAL OUTPUT CODE



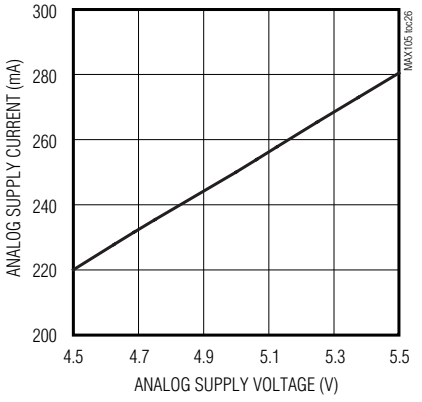
DNL vs. DIGITAL OUTPUT CODE



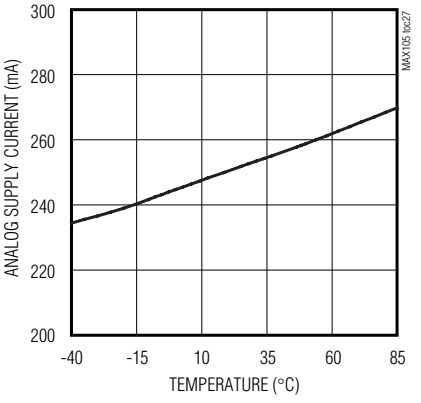
REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



ANALOG SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 20	T.P.	Test Point. **Do not connect.**
2	REF	Reference Output
3	$AV_{CC}R$	Analog Reference Supply. Supply voltage for the internal bandgap reference. Bypass to AGNDR with 0.01µF in parallel with 47pF for proper operation.
4	AGNDR	Reference, Analog Ground. **Connect to AGND for proper operation.**
5, 8	AGNDI	I-Channel, Analog Ground. **Connect to AGND for proper operation.**
6	INI-	I-Channel, Differential Input. Negative terminal.
7	INI+	I Channel, Differential Input. Positive terminal.
9	$AV_{CC}I$	I-Channel, Analog Supply. Supplies I-channel common-mode buffer, pre-amplifier and quantizer. Bypass to AGNDI with 0.01µF in parallel with 47pF for proper operation.
10	CLK+	Sampling Clock Input
11	CLK-	Complementary Sampling Clock Input
12	$AV_{CC}Q$	Q-Channel, Analog Supply. Supplies Q-channel common-mode buffer, pre-amplifier and quantizer. Bypass to AGNDQ with 0.01µF in parallel with 47pF for proper operation.
13, 16	AGNDQ	Q-Channel, Analog Ground. **Connect to AGND for proper operation.**
14	INQ+	Q-Channel, Differential Input. Positive terminal.
15	INQ-	Q-Channel, Differential Input. Negative terminal.
17, 18	AGND	Analog Ground
19	AV_{CC}	Analog Supply. Bypass to AGND with 0.01µF in parallel with 47pF for proper operation.
21	A5Q+	Auxiliary Output Data Bit 5 (MSB), Q-Channel
22	A5Q-	Complementary Auxiliary Output Data Bit 5 (MSB), Q-Channel
23	P5Q+	Primary Output Data Bit 5 (MSB), Q-Channel
24	P5Q-	Complementary Primary Output Data Bit 5 (MSB), Q-Channel
25	A4Q+	Auxiliary Output Data Bit 4, Q-Channel
26	A4Q-	Complementary Auxiliary Output Data Bit 4, Q-Channel
27	P4Q+	Primary Output Data Bit 4, Q-Channel
28	P4Q-	Complementary Primary Output Data Bit 4, Q-Channel
29, 35	$OV_{CC}Q$	Q-Channel Outputs, Digital Supply. Supplies Q-channel output drivers and DOR logic. Bypass to OGND with 0.01µF in parallel with 47pF for proper operation.
30, 36	OGNDQ	Q-Channel Outputs, Digital Ground. **Connect to designated digital ground (OGND) on PC board for proper operation.**

Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

Pin Description (continued)

PIN	NAME	FUNCTION
31	A3Q+	Auxiliary Output Data Bit 3, Q-Channel
32	A3Q-	Complementary Auxiliary Output Data Bit 3, Q-Channel
33	P3Q+	Primary Output Data Bit 3, Q-Channel
34	P3Q-	Complementary Primary Output Data Bit 3, Q-Channel
37	A2Q+	Auxiliary Output Data Bit 2, Q-Channel
38	A2Q-	Complementary Auxiliary Output Data Bit 2, Q-Channel
39	P2Q+	Primary Output Data Bit 2, Q-Channel
40	P2Q-	Complementary Primary Output Data Bit 2, Q-Channel
41	A1Q+	Auxiliary Output Data Bit 1, Q-Channel
42	A1Q-	Complementary Auxiliary Output Data Bit 1, Q-Channel
43	P1Q+	Primary Output Data Bit 1, Q-Channel
44	P1Q-	Complementary Primary Output Data Bit 1, Q-Channel
45	A0Q+	Auxiliary Output Data Bit 0 (LSB), Q-Channel
46	A0Q-	Complementary Auxiliary Output Data Bit 0 (LSB), Q-Channel
47	P0Q+	Primary Output Data Bit 0 (LSB), Q-Channel
48	P0Q-	Complementary Primary Output Data Bit 0 (LSB), Q-Channel
49	DOR+	Complementary LVDS Out-Of-Range Bit
50	DOR-	LVDS Out-of-Range Bit
51	DREADY-	Complementary Data-Ready Clock
52	DREADY+	Data Ready Clock
53	P0I-	Complementary Primary Output Data Bit 0 (LSB), I-Channel
54	P0I+	Primary Output Data Bit 0 (LSB), I-Channel
55	A0I-	Complementary Auxiliary Output Data Bit 0 (LSB), I-Channel
56	A0I+	Auxiliary Output Data Bit 0 (LSB), I-Channel
57	P1I-	Complementary Primary Output Data Bit 1, I-Channel
58	P1I+	Primary Output Data Bit 1, I-Channel
59	A1I-	Complementary Auxiliary Output Data Bit 1, I-Channel
60	A1I+	Auxiliary Output Data Bit 1, I-Channel
61	P2I-	Complementary Primary Output Data Bit 2, I-Channel

Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

Pin Description (continued)

PIN	NAME	FUNCTION
62	P2I+	Primary Output Data Bit 2, I-Channel
63	A2I-	Complementary Auxiliary Output Data Bit 2, I-Channel
64	A2I+	Auxiliary Output Data Bit 2, I-Channel
65, 72	$OV_{CC}I$	I-Channel Outputs, Digital Supply. Supplies I-channel output drivers and DREADY circuit. Bypass to OGND with 0.01µF in parallel with 47pF for proper operation.
66, 71	OGNDI	I-Channel Outputs, Digital Ground. **Connect to designated digital ground (OGND) on PC board for proper operation.**
67	P3I-	Complementary Primary Output Data Bit 3, I-Channel
68	P3I+	Primary Output Data Bit 3, I-Channel
69	A3I-	Complementary Auxiliary Output Data Bit 3, I-Channel
70	A3I+	Auxiliary Output Data Bit 3, I-Channel
73	P4I-	Complementary Primary Output Data Bit 4, I-Channel
74	P4I+	Primary Output Data Bit 4, I-Channel
75	A4I-	Complementary Auxiliary Output Data Bit 4, I-Channel
76	A4I+	Auxiliary Output Data Bit 4, I-Channel
77	P5I-	Complementary Primary Output Data Bit 5, I-Channel
78	P5I+	Primary Output Data Bit 5, I-Channel
79	A5I-	Complementary Auxiliary Output Data Bit 5, I-Channel
80	A5I+	Auxiliary Output Data Bit 5, I-Channel

Detailed Description

The MAX105 is a dual, +5V, 6-bit, 800Msps flash analog-to-digital converter (ADC), designed for high-speed, high-bandwidth I&Q digitizing. Each ADC (Figure 1) employs a fully differential, wide bandwidth input stage, 6-bit quantizers and a unique encoding scheme to limit metastable states to typically one error per 10^{16} clock cycles, with no error exceeding a maximum of 1LSB. An integrated 6:12 output demultiplexer simplifies interfacing to the part by reducing the output data rate to one-half the sampling clock rate. The MAX105 outputs data in LVDS two's complement format.

When clocked at 800Msps, the MAX105 provides a typical signal-to-noise plus distortion (SINAD) of 36.4dB with a 200MHz input tone. The analog input of the MAX105 is designed for differential or single-ended use with a ±400mV full-scale input range. In addition, the MAX105 features an on-board +2.5V precision bandgap reference, which is scaled to meet the analog input full-scale range.

Principle of Operation

The MAX105 employs a flash or parallel architecture. The key to this high-speed flash architecture is the use of an innovative, high-performance comparator design. Each quantizer and downstream logic translates the comparator outputs into 6-bit, parallel codes in two's complement format and passes them on to the internal 6:12 demultiplexer. The demultiplexer enables the ADCs to provide their output data at half the sampling speed on primary and auxiliary ports. LVDS data is available at speeds of up to 400MHz per output port.

Input Amplifier Circuits

As with all ADCs, if the input waveform is changing rapidly during conversion, effective number of bits (ENOB), signal-to-noise plus distortion (SINAD), and

Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

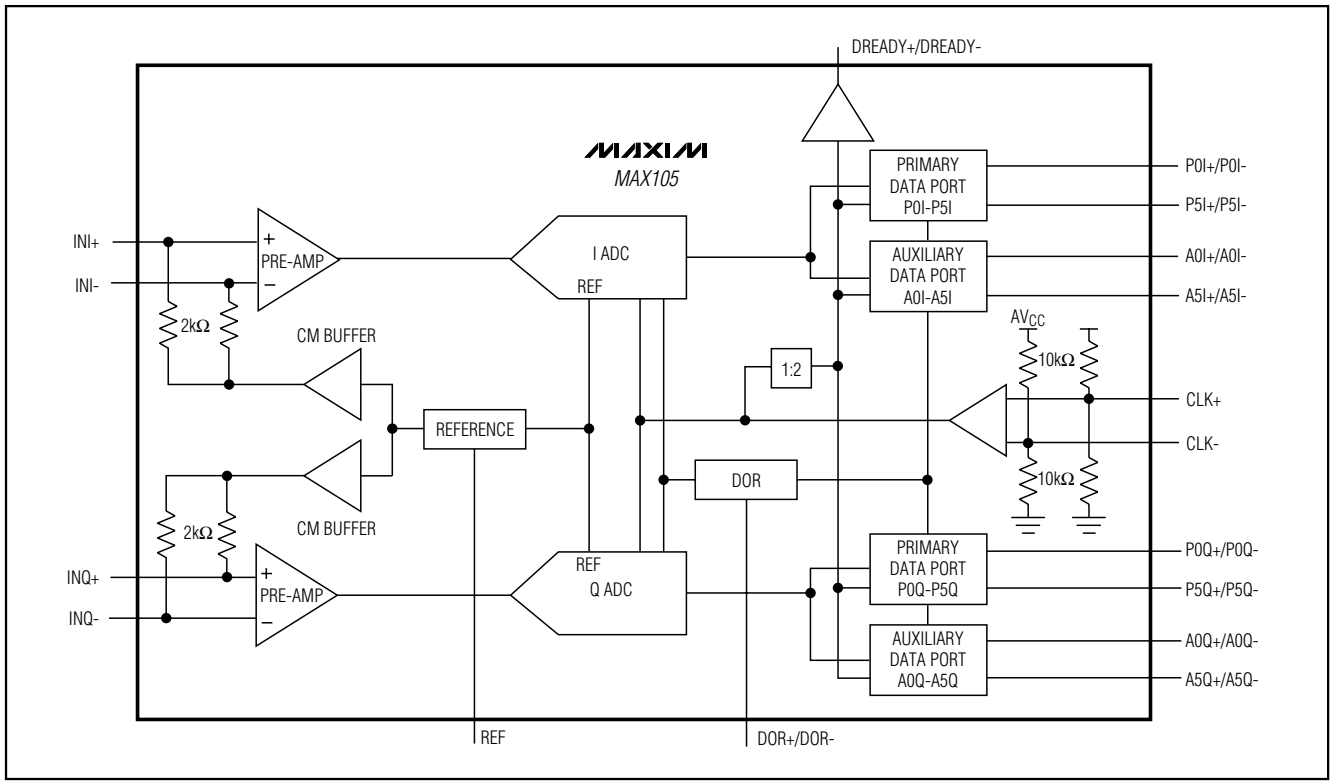


Figure 1. MAX105 Flash Converter Architecture

signal-to-noise ratio (SNR) specifications will degrade. The MAX105's on-board, wide-bandwidth input amplifiers (I&Q) reduce this effect significantly, allowing precise digitizing of fast analog data at high conversion rates. The input amplifiers buffer the input signal and allow a full-scale signal input range of ±400mV ($800mV_{p-p}$).

Internal Reference

The MAX105 features an integrated, buffered +2.5V precision bandgap reference. This reference is internally scaled to match the analog input range specification of ±400mV. The data converter's reference output (REF) can source up to 500µA. REF should be buffered, if used to supply external devices.

LVDS Digital Outputs

The MAX105 provides data in two's complement format to differential LVDS outputs. A simplified circuit schematic of the LVDS output cells is shown in Figure 2. All LVDS outputs are powered from separate I-channel $OV_{CC}I$ and Q-channel $OV_{CC}Q$ (Q-channel) power supplies, which may be operated at +3.3V ±10%. The

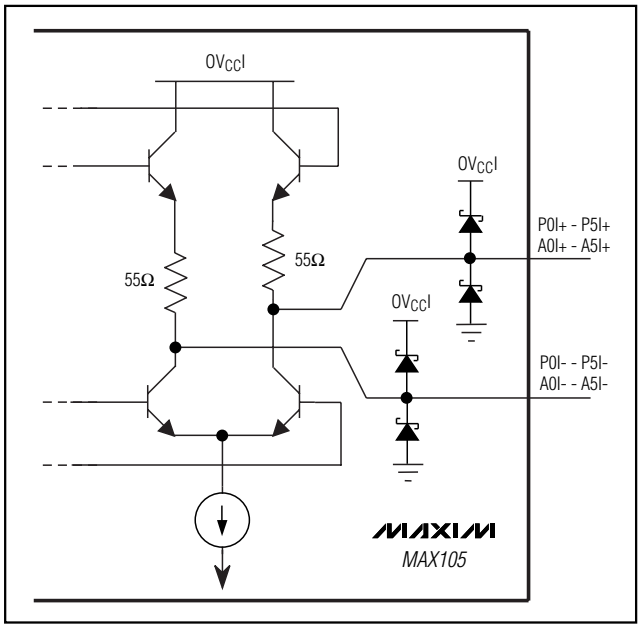


Figure 2. Simplified LVDS Output Model

Table 1. Digital Output Codes Corresponding to a DC-Coupled Single-Ended Analog Input

IN-PHASE INPUTS (INI+, INQ+)	INVERTED INPUTS (INI-, INQ-)	OUT-OF-RANGE BIT (DOR+, DOR-)	OUTPUT CODE
> +400mV + V_{REF}	AC – Coupled to AGND_	1	011111
+400mV - 0.5LSB + V_{REF}	AC – Coupled to AGND_	0	011111
0V + V_{REF}	AC – Coupled to AGND_	0	000000/111111
-400mV + 0.5LSB + V_{REF}	AC – Coupled to AGND_	0	100000
< -400mV + V_{REF}	AC – Coupled to AGND_	1	100000

Table 2. Digital Output Codes Corresponding to a DC-Coupled Differential Analog Input

IN-PHASE INPUTS (INI+, INQ+)	INVERTED INPUTS (INI-, INQ-)	OUT-OF-RANGE BIT (DOR+, DOR-)	OUTPUT CODE
>+200mV + V_{REF}	<-200mV + V_{REF}	1	011111
+200mV - 0.25LSB + V_{REF}	-200mV + 0.25LSB + V_{REF}	0	011111
0V + V_{REF}	0V + V_{REF}	0	000000/111111
-200mV + 0.25LSB + V_{REF}	+200mV - 0.25LSB + V_{REF}	0	100000
<-200mV + V_{REF}	>+200mV + V_{REF}	1	100000

MAX105 LVDS-outputs provide a typical ±270mV voltage swing around a common mode voltage of roughly +1.2V, and must be differentially terminated at the far end of each transmission line pair (true and complementary) with 100Ω.

Out-Of-Range Operation

A single output pair (DOR+, DOR-) is provided to flag an out-of-range condition, if either the I or Q channel is out-of-range, where out-of-range is above +FS or below -FS. It features the same latency as the ADCs output data and is demultiplexed in a similar fashion. With a 800MHz system clock, DOR+ and DOR- are clocked at up to 400MHz.

Applications Information

Single-Ended Analog Inputs

The MAX105 is designed to work at full-speed for both single-ended and differential analog inputs without significant degradation in its dynamic performance. Both input channels I (INI+, INI-) and Q (INQ+, INQ-) have 2kΩ impedance and allow for AC- and DC-coupled input signals. In a typical DC-coupled single-ended configuration (Table 1), the analog input signals enter the analog input amplifier stages at the in-phase-input pins INI+/INQ+, while the inverted phase input INI-/INQ- pins are AC-coupled to AGNDI/AGNDQ. Single-ended operation allows for an input amplitude of 800mV_{p-p}, centered around V_{REF}.

Differential Analog Inputs

To obtain +FS digital outputs with differential input drive (Table 2), 400mV must be applied between INI+ (INQ+) and INI- (INQ-). Midscale digital output codes occur when there is no voltage difference between INI+ (INQ+) and INI- (INQ-). For a -FS digital output code both in-phase (INI+, INQ+) and inverted input (INI-, INQ-) must see -400mV.

Single-Ended to Differential Conversion Using a Balun

An RF balun (Figure 3) provides an excellent solution to convert a single-ended signal to a fully differential signal, required by the MAX105 for optimum performance. At higher frequencies, the MAX105 provides better SFDR and THD with fully differential input signals over single-ended input signals. In differential input mode, even-order harmonics are suppressed and each input requires only half the signal-swing compared to single-ended mode.

Clock Input

The MAX105 features clock inputs designed for either single-ended or differential operation with very flexible input drive requirements. The clock inputs (AC- or DC-coupled) provide a 5kΩ input impedance to $AV_{CC}/2$

Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

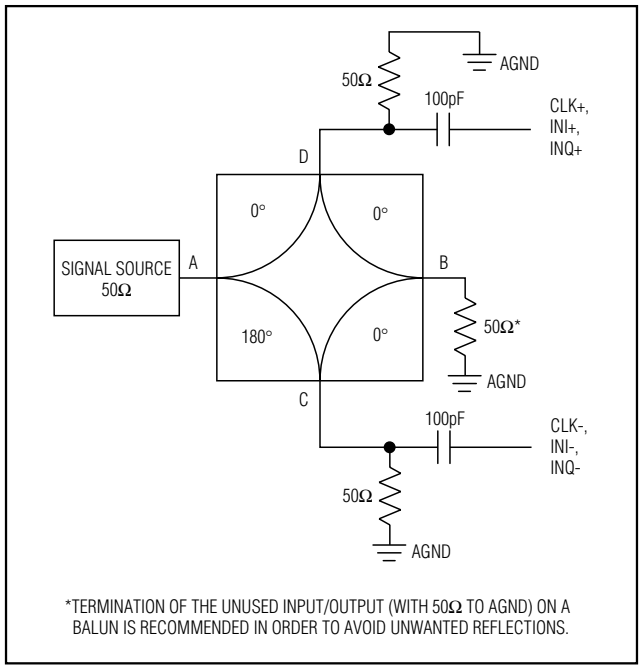


Figure 3. Single-Ended to Differential Conversion Using a Balun

and are internally buffered with a preamplifier to ensure proper operation of the converter even with small-amplitude sine-wave sources. The MAX105 was designed for single-ended, low-phase noise sine wave clock signals with as little as 500mV$_{P-P}$ amplitude (-2dBm).

Single-Ended Clock (Sine-Wave Drive)

Excellent performance is obtained by AC- or DC-coupling a low-phase noise sine-wave source into a single clock input (Figure 4). Essentially, the dynamic performance of the converter is unaffected by clock-drive power levels from -2dBm (500mV$_{p-p}$ clock signal amplitude) to +10dBm (2V$_{P-P}$ clock signal amplitude). The MAX105 dynamic performance specifications are determined by a single-ended clock drive of -2dBm (500mVp-p clock signal amplitude). To avoid saturation of the input amplifier stage, limit the clock power level to a maximum of +10dBm.

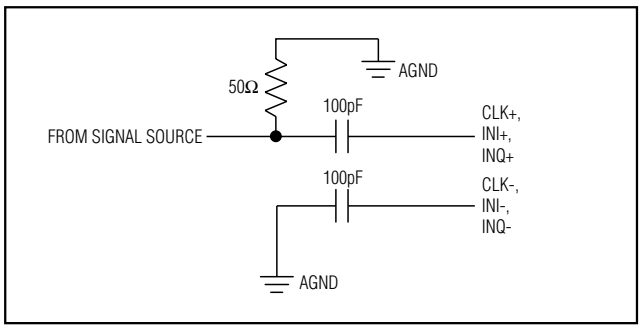


Figure 4. Single-Ended Clock Input With AC-Coupled Input Drive (CLK, INI, INQ)

Differential Clock (Sine-Wave Drive)

The advantages of differential clock drive (Figure 5) can be obtained by using an appropriate balun or transformer to convert single-ended sine-wave sources into differential drives. Refer to *Single-Ended Clock Inputs (Sine-Wave Drive)* for proper input amplitude requirements.

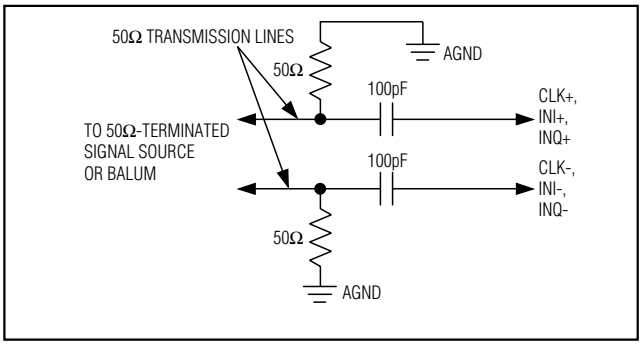


Figure 5. Differential AC-Coupled Input Drive (CLK, INI, INQ)

LVDS, ECL and PECL Clock

The innovative input architecture of the MAX105 clock also allows these inputs to be driven by LVDS-, ECL-, or PECL-compatible input levels, ranging from 500mV$_{p-p}$ to 2V$_{p-p}$ (Figure 6).

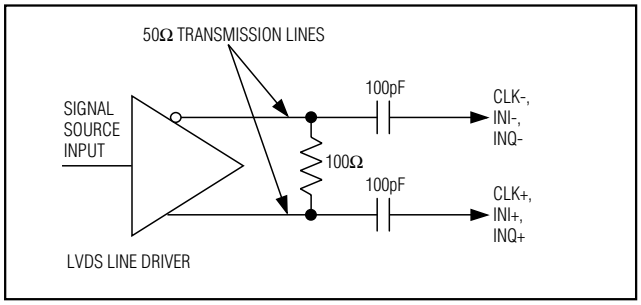
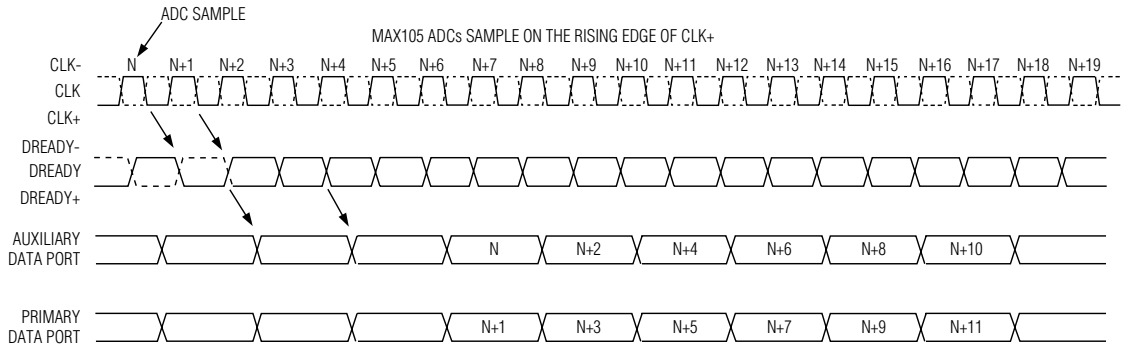


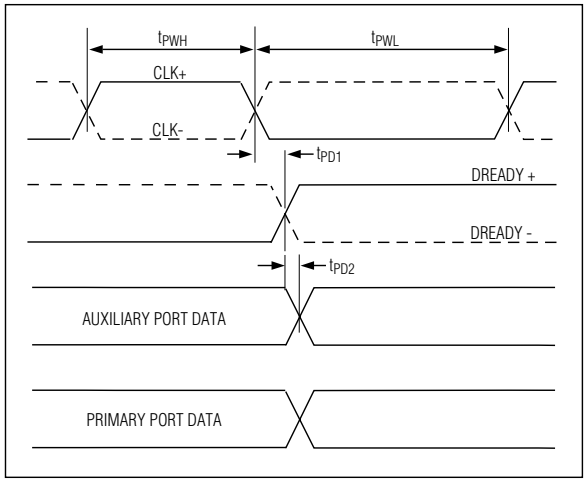
Figure 6. LVDS Input Drive (CLK, INI, INQ)

Timing Requirements

The MAX105 features a 6:12 demultiplexer, which reduces the output data rate (including DREADY and DOR signals) to one-half of the sample clock rate. The



NOTE: THE LATENCY TO THE PRIMARY PORT IS FIVE CLOCK CYCLES, THE LATENCY TO THE AUXILIARY PORT IS SIX CLOCK CYCLES. BOTH PRIMARY AND AUXILIARY DATA PORTS ARE UPDATED ON THE RISING EDGE OF THE DREADY+ CLOCK.



MAXIM
MAX105

Figure 7. Output Timing Relationship Between CLK and DREADY Signals and Primary/Auxiliary Output Ports

demultiplexed outputs are presented in dual 6-bit two's complement format with two consecutive samples in the primary and auxiliary output ports on the rising edge of the data ready clock. The auxiliary data port always contains the older sample. The primary output always contains the most recent data sample, regardless of the DREADY clock phase. Figure 7 shows the timing and data alignment of the auxiliary and primary output ports in relationship with the CLK and DREADY signals. Data in the primary port is delayed by five clock cycles while data in the auxiliary port is delayed by six clock cycles.

Typical I/Q Application

Quadrature amplitude modulation (QAM) is frequently used in digital communication systems to increase channel capacity. A QAM signal is modulated in both amplitude and phase. With a demodulator, this QAM signal gets downconverted and separated in its in-phase (I) and quadrature (Q) components. Both I&Q channels are digitized by an ADC at the baseband level in order to recover the transmitted information. Figure 8 shows a typical application circuit to directly tune L-band signals to baseband, incorporating a direct conversion tuner (MAX2108) and the MAX105 to digitize I&Q channels with excellent phase- and gain-matching. A front-end L-C filter is required for anti-aliasing purposes.

Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

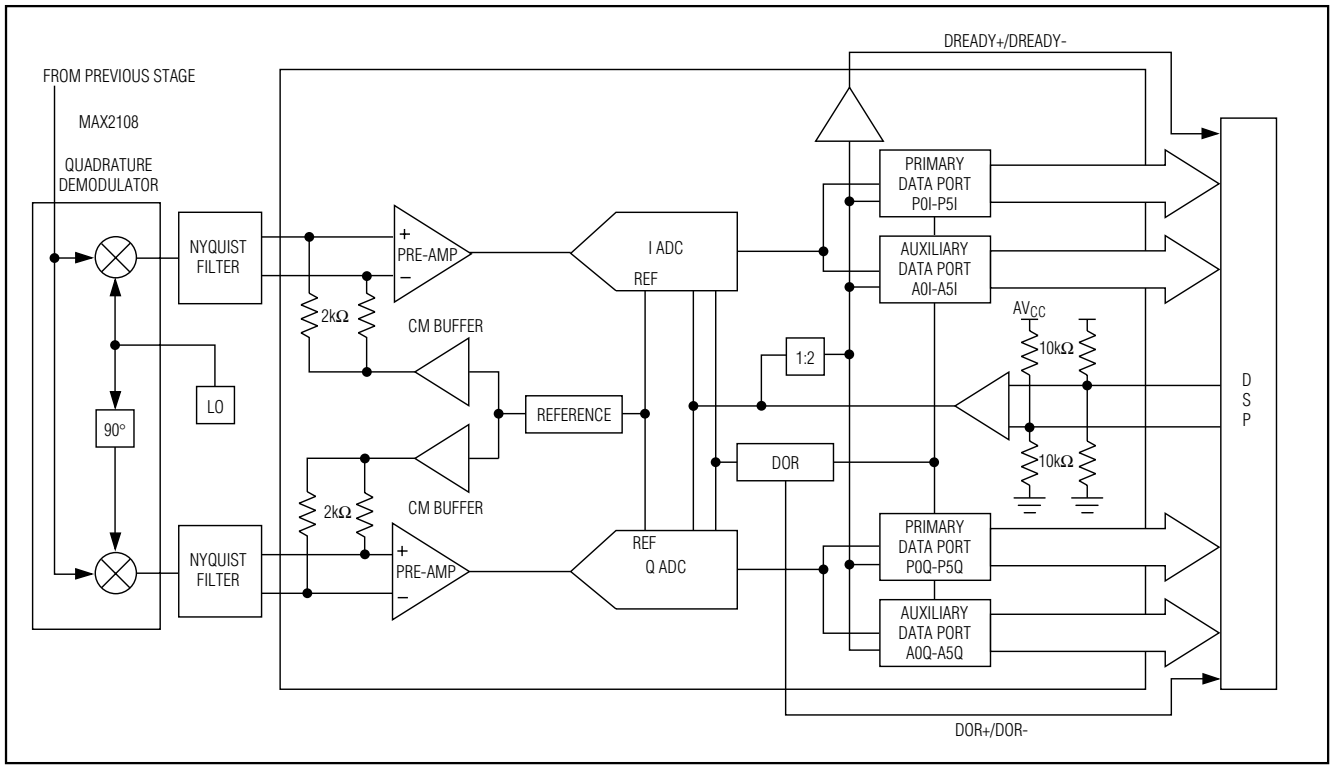


Figure 8. Typical I/Q Application

Grounding, Bypassing, and Board Layout

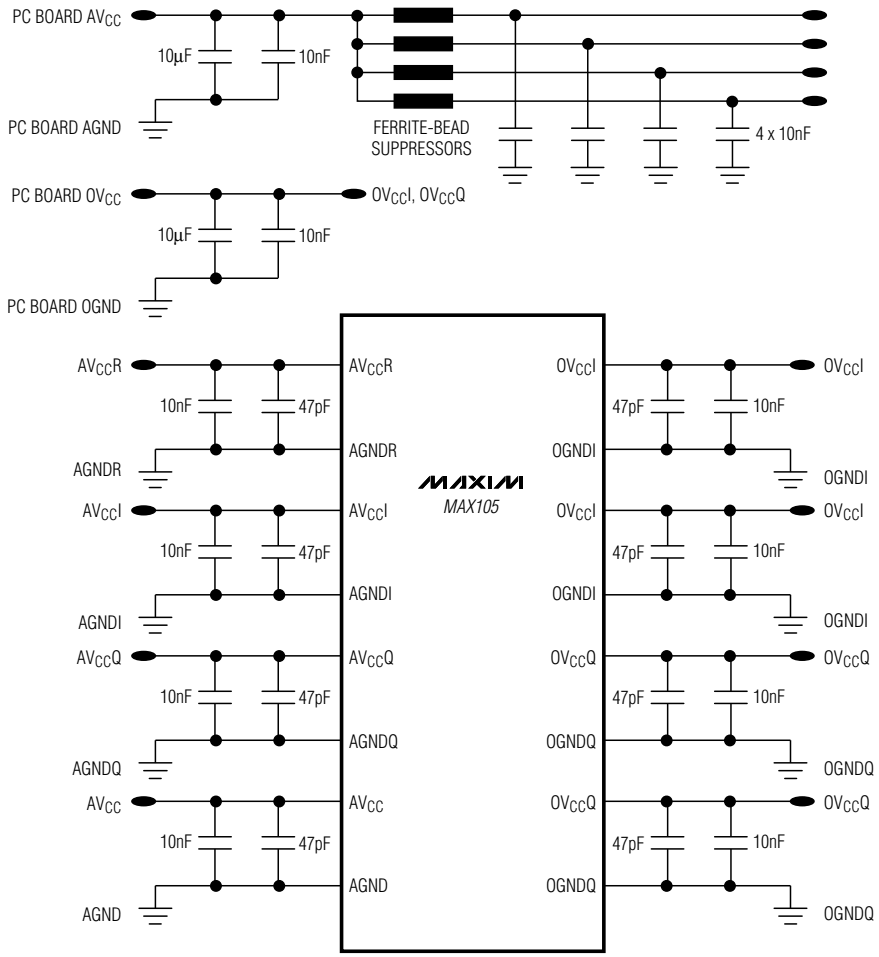
Grounding and power supply decoupling strongly influence the MAX105's performance. At 800MHz clock frequency and 6-bit resolution, unwanted digital crosstalk may couple through the input, reference, power supply, ground connections, and adversely influence the dynamic performance of the ADC. In addition, the I&Q inputs may crosstalk through poorly designed decoupling circuits. Therefore, closely follow the grounding and power-supply decoupling guidelines in Figure 9.

Maxim strongly recommends using a multilayer printed circuit board (PC board) with separate ground and power supply planes. Since the MAX105 has separate analog and digital ground connections (AGND, AGNDI, AGNDQ, AGNDR, OGNDI, and OGNDQ, respectively). The PC board should feature separate sections designated to analog (AGND) and digital (OGND), connected at only one point. Digital signals should run above the digital ground plane and analog signals should run above the analog ground plane. Keep digital signals far away from the sensitive analog inputs, reference inputs, and clock inputs. High-speed signals, including clocks, analog inputs, and digital outputs, should be routed on 50Ω microstrip lines, such as those employed on the MAX105EV kit.

The MAX105 has separate analog and digital power-supply inputs:

- AV_{CC} = +5V ±5%: Power supply for the analog input section of the clock circuit.
- $AV_{CC}I$ = +5V ±5%: Power supply for the I-channel common-mode buffer, pre-amp and quantizer.
- $AV_{CC}Q$ = +5V ±5%: Power supply for the Q-channel common-mode buffer, pre-amp and quantizer.
- $AV_{CC}R$ = +5V ±5%: Power supply for the on-chip bandgap reference.
- $OV_{CC}I$ = +3.3V ±10%: Power supply for the I-channel output drivers and DREADY circuitry.
- $OV_{CC}Q$ = +3.3V ±10%: Power supply for the Q-channel output drivers and DOR circuitry.

All supplies should be decoupled with large tantalum or electrolytic capacitors at the point they enter the PC board. For best performance, bypass all power sup-



NOTE:
LOCATE ALL 47pF AND 10nF CAPACITORS, WHICH DECOUPLE $AV_{CC}I$, $AV_{CC}Q$, $AV_{CC}R$, $OV_{CC}I$, AND $OV_{CC}Q$ AS CLOSE AS POSSIBLE TO THE CHIP. IT IS ALSO RECOMMENDED TO CONNECT ALL ANALOG GROUND CONNECTIONS TO A COMMON ANALOG GROUND PLANE AND ALL DIGITAL GROUND CONNECTIONS TO ONE COMMON DIGITAL GROUND PLANE ON THE PC BOARD. A SIMILAR TECHNIQUE CAN BE USED FOR ALL ANALOG AND DIGITAL POWER SUPPLIES.

$AV_{CC} = AV_{CC}I = AV_{CC}Q = AV_{CC}R = +5V \pm 5\%$

$OV_{CC}I = OV_{CC}Q = +3.3V \pm 10\%$

Figure 9. MAX105 Decoupling, Bypassing and Grounding

plies to the appropriate ground with a 10µF tantalum capacitor, to filter power supply noise, in parallel with a 0.1µF capacitor. A combination of 0.01µF in parallel with high quality 47pF ceramic chip capacitor located very close to the MAX105 device filters high frequency noise. A properly designed PC board (see MAX105EV Kit data sheet) allows the user to connect all analog supplies and all digital supplies together thereby requiring only two separate power sources. Decoupling AV_{CC}, $AV_{CC}I$, $AV_{CC}Q$ and $AV_{CC}R$ with ferrite-bead suppressors prevents further crosstalk between the individual analog supply pins

Thermal Management

The MAX105 is designed for a thermally enhanced 80-pin TQFP package, providing greater design flexibility, increased thermal efficiency and a low thermal junction-case (θjc) resistance of ≈1.26°C/W. In this pack-

Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

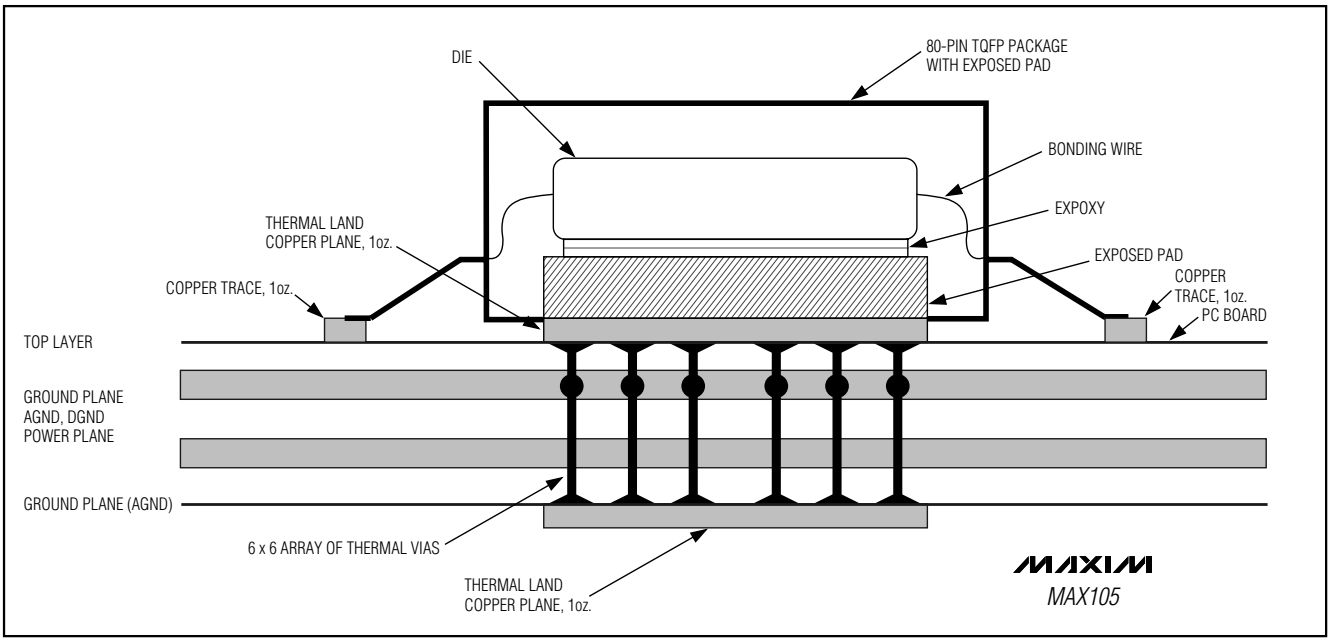


Figure 10. MAX105 Exposed Pad Package Cross-Section

age, the data converter die is attached to an exposed pad (EP) leadframe using a thermally conductive epoxy. The package is molded in a way, that this leadframe is exposed at the surface, facing the printed circuit board (PC board) side of the package (Figure 10). This allows the package to be attached to the PC board with standard infrared (IR) flow soldering techniques. A specially created land pattern on the PC board, matching the size of the EP (7.5mm x 7.5mm) does not only guarantee proper attachment of the chip, but can also be used for heat-sinking purposes. Designing thermal vias* into the land area and implementing large ground planes in the PC board design, further enhance the thermal conductivity between board and package. To remove heat from an 80-pin TQFP package efficiently, an array of 6 x 6 vias (≤ 0.3mm diameter per via hole and 1.2mm pitch between via holes) is required.

Note: Efficient thermal management for the MAX105 is strongly depending on PC board and circuit design, component placement, and installation. Therefore, exact performance figures cannot be provided. However, the MAX105EV kit exhibits a typical θja of 18°C/W. For more information on proper design techniques and recommendations to enhance the thermal performance of parts such as the MAX105, please refer to Amkor Technology's website at www.amkor.com.

**Connects the land pattern to internal or external copper planes.*

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line is drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX105 are measured using the sine-histogram method.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step-width and the ideal value of 1LSB. A DNL error specification of greater than -1LSB guarantees no missing codes and a monotonic transfer function.

Dynamic Parameter Definitions

Aperture Jitter and Delay

Aperture uncertainties affect the dynamic performance of high-speed converters. Aperture jitter, in particular, directly influences SNR and limits the maximum slew rate (dV/dt) that can be digitized without significant error. Aperture jitter limits the SNR performance of the ADC, according to the following relationship:

$$SNR_{dB} = 20 \times \log_{10} [1 / (2 \times \pi \times f_{IN} \times t_{AJ[RMS]})],$$

where f_{IN} represents the analog input frequency and t_{AJ} is the RMS aperture jitter. The MAX105's innovative

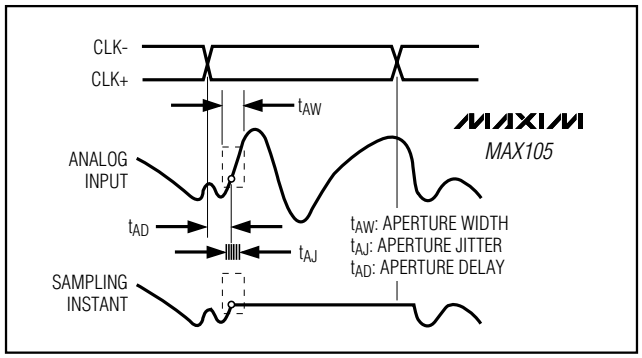


Figure 11. Aperture Timing

clock design limits aperture jitter to typically 1.5ps$_{RMS}$. Figure 11 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay. Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 11).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N-Bits):

$$SNR_{MAX[dB]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter (see *Aperture Uncertainties*). SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first four harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components minus the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency, amplitude, and sampling rate relative to an ideal ADC's quantization noise. For a full-scale input ENOB is computed from:

$$ENOB = (SINAD - 1.76_{dB}) / 6.02_{dB}$$

Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the first four harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)/V_1^2)}$$

where V1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental to the RMS value of the next largest spurious component, excluding DC offset.

Two-Tone Intermodulation Distortion (IMD)

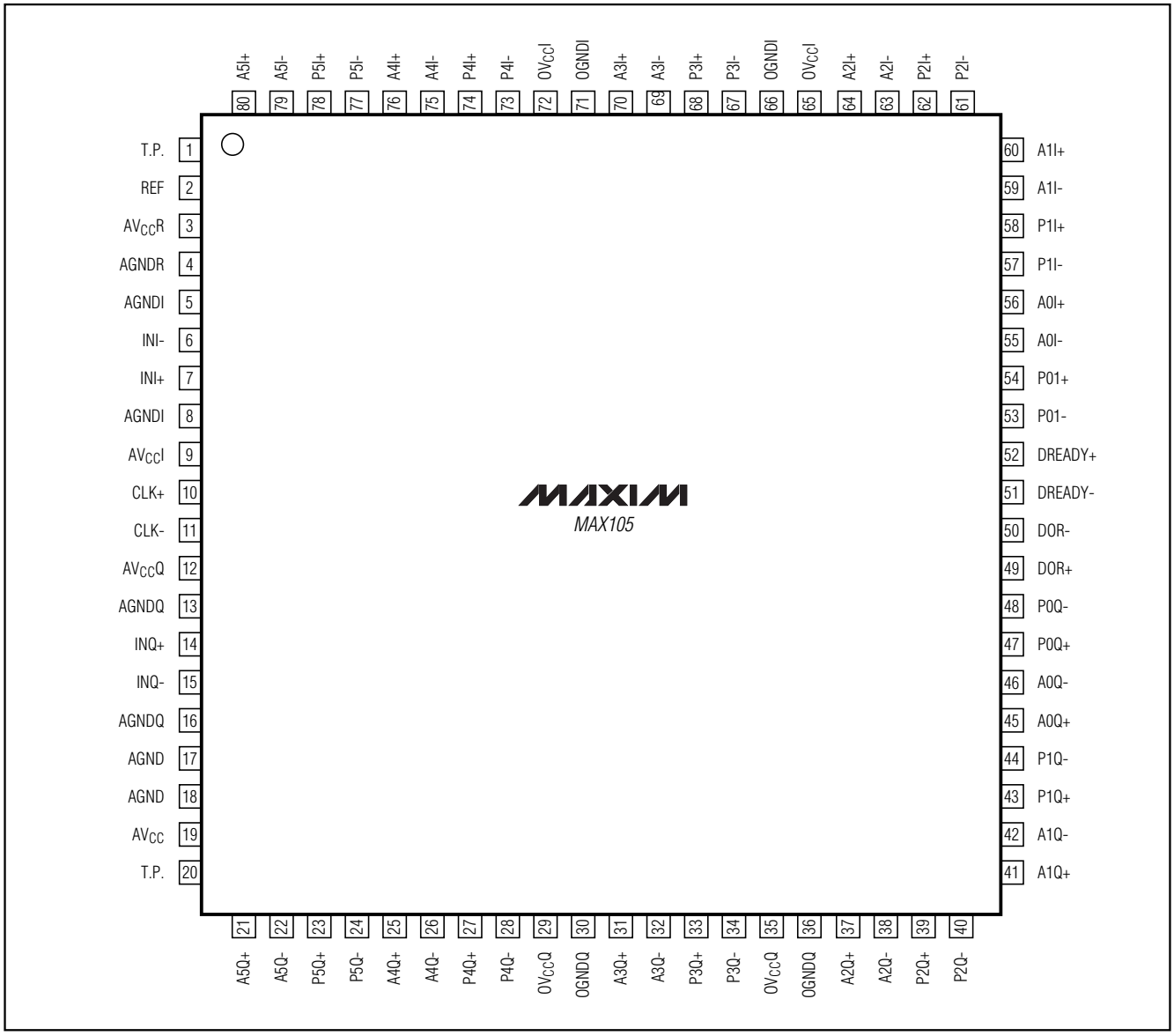
The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) intermodulation products. The individual input tone levels are at -7dB full-scale and their envelope peaks at -1dB full-scale.

Chip Information

TRANSISTOR COUNT: 12,286

Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

Pin Configuration



Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier

Package Information