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MB15U36

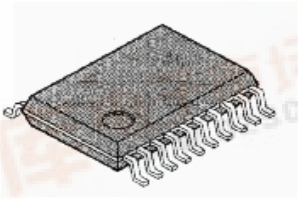
Dual PLL Frequency Synthesizer with On-Chip Prescaler

FUJITSU

Description

The Fujitsu MB15U36 dual PLL is a serial input frequency synthesizer with 2.0 GHz and 1.2 GHz prescalers. The prescalers both have a selectable dual modulus division ratio of 64/65 or 128/129 enabling pulse swallow operation. The MB15U36 utilizes a refined charge pump design (Fujitsu's Super Charger)that provides fast tuning along with low spurious noise and phase noise characteristics. The MB15U36 is ideally suited for digital mobile communications, including GSM, DCS1800, PCS1900, IS-136, IS-95 and ISM-band applications.

Packages



20-pin plastic SSOP, FPT-20P-M03

Features

- Very low spurious and phase noise characteristics
- Wide operating voltage: 3.0 to 5.5 volts
- Low operating current: 6.0 mA @ V_{CC} = 3 volts (typical)
- Power-saving current: 10µA (typical)
- Wide operating temperature: –40 to +85°C
- Plastic 20-pin SSOP package
- Reference counter:
  - 15-bit programmable divider: 3 to 32767
- 18-bit programmable divider:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2047
- Software selectable charge pump current:
  - Do output ±1.0 or ±4.0 mA @ V_{CC} = 3V
- Evaluation Kits available

Parameter	MB15U36
RF frequency of operation, max.	2.0 GHz
IF/RF frequency of operation, max	1.2 GHz
Low power supply voltage	3 - 5.5V
Low power supply current	6.0 mA @ 3V
Prescaler divide ratios	RF1, RF2 = 64/65 or 128/129
Power-saving function	10µA typical

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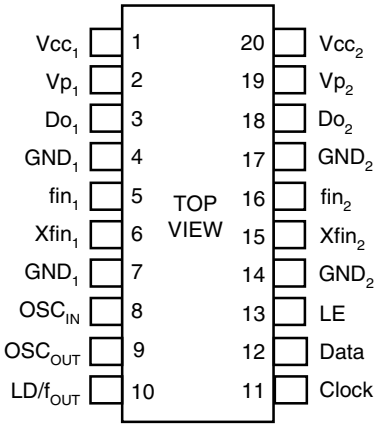
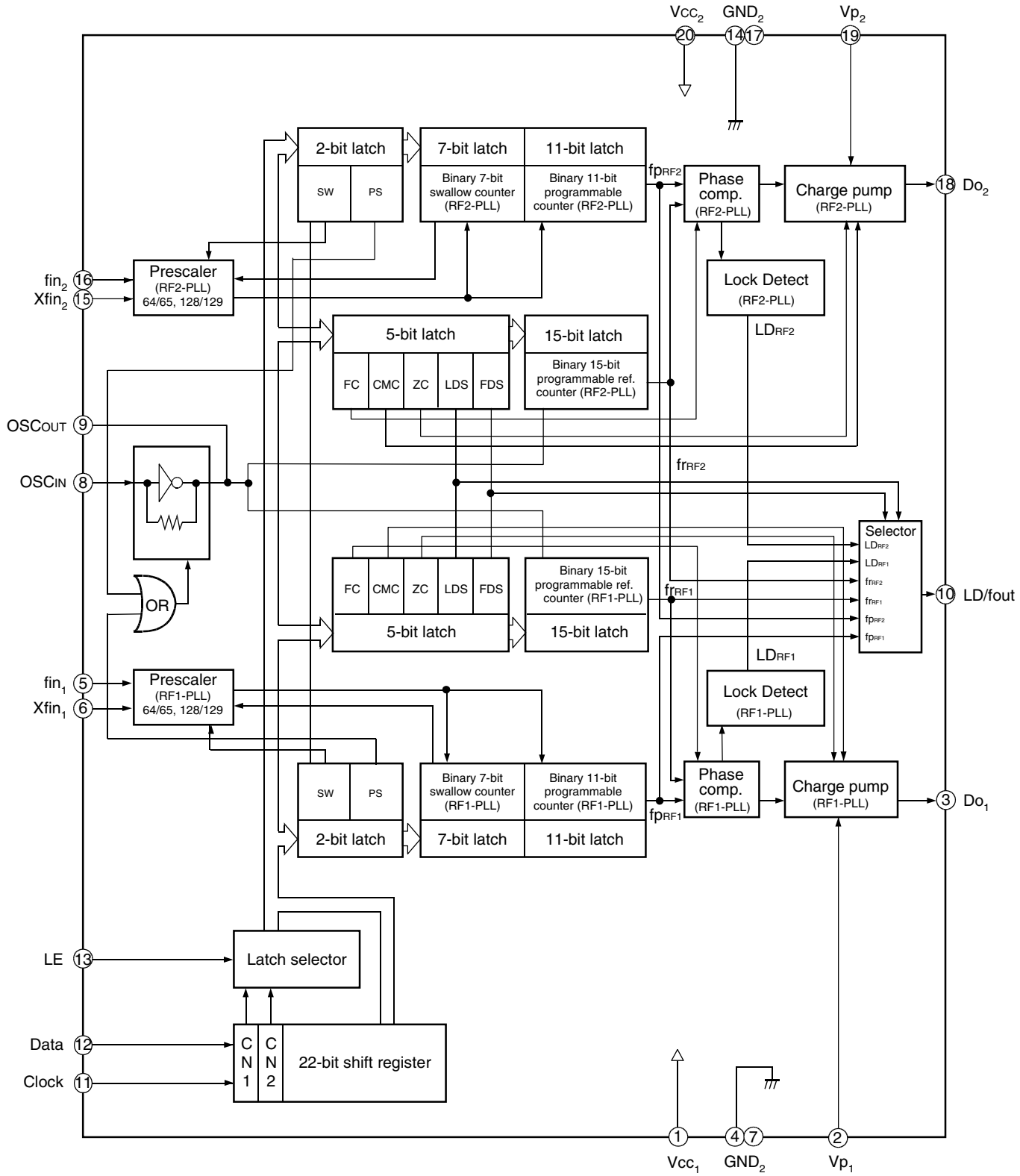
Pin Descriptions: MB15U36

Pin No. SSOP	Pin Name	I/O	Descriptions
1	Vcc_1	–	Power supply voltage input pin for the RF1-PLL section, the shift register, and the oscillator input buffer. When poweris OFF, latched data for RF1-PLL is lost.
2	Vp_1	I	Power supply for the RF1-PLL charge pump. (Independent of pin 19)
3	Do_1	O	Charge pump output for the RF1-PLL section. Phase detector characteristics can be reversed using the FC-bit.
4	GND1	–	Ground for the RF1-PLL section.
5	fin_1	I	Prescaler input for the RF1-PLL. Connection to an external VCO should be via AC coupling.
6	$Xfin_1$	I	Prescaler complimentary input for the RF1-PLL section. This pin should be grounded via a small capacitor.
7	GND1	–	Ground for the RF1-PLL section.
8	OSC_{IN}	I	External TCXO reference oscillator input or connection to crystal. TCXO should be connected via AC coupling.
9	OSC_{OUT}	O	Oscillator output or connection to crystal.
10	LD/f_{OUT}	O	Lock detect signal output (LD) or phase comparator monitoring output (f_{out}). The output signal is selected by the LDS and FDS bits in the serial programming data.
11	Clock	I	Clock input for the 22-bit shift register. One bit of data is shifted into the shift register on a rising edge of the clock.
12	Data	I	Serial data input. Data is transferred to the corresponding latch (RF1-ref counter, RF1-prog. counter, RF2-ref. counter, RF2-prog. counter) according to the control bits settings in the serial programming data.
13	LE	I	Load enable signal input. When the LE bit is set to “H”, data in the shift register is transferred to the corresponding latch ac cording to the control bits settings in the serial programming data.
14	GND2	–	Ground for the RF2-PLL section.
15	$Xfin_2$	I	Prescaler complimentary input for the RF2-PLL section. This pin should be grounded via a small capacitor.
16	fin_2	I	Prescaler input for the RF2-PLL. Connection to an external VCO should be via AC coupling.
17	GND2	–	Ground for the RF2-PLL section.
18	Do_2	O	Charge pump output for the RF2-PLL section. Phase detector characteristics can be reversed using the FC-bit.
19	Vp_2	I	Power supply for the RF2-PLL charge pump. (Independent of pin 2)
20	Vcc_2	–	Power supply voltage input pin for the RF2-PLL section. When power is OFF, latched data for RF2-PLL is lost.



(FPT-20P-M03)

Block Diagram: MB15U36



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Power supply voltage	$Vcc_{1,2}$	–0.5 to +6.5	V	
	$Vp_{1,2}$	–0.5 to +6.5	V	
Input voltage	V_I	–0.5 to +6.5	V	
Output voltage	V_O	–0.5 to +6.5	V	
Storage temperature	T_{STG}	–55 to +125	°C	

WARNING: Semiconductor devices can be permanently damaged by the application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power supply voltage	Vcc	3.0	5.0	5.5	V	$Vcc_1 = Vcc_2$
	Vp	3.0	5.0	5.5	V	$Vcc_1 = Vcc_2$ *1
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

*1: Prescaler divide ratio is only 64/65 (SW = "L") at RF1.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Fujitsu representative beforehand.

Handling Precautions

- This device should be transported and stored in anti-static containers
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

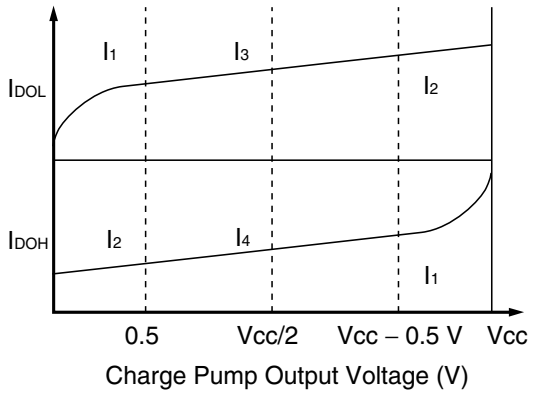
Electrical Characteristics

(V_{CC} =3.0 to 5.5V,Ta = –40 to +85°C)

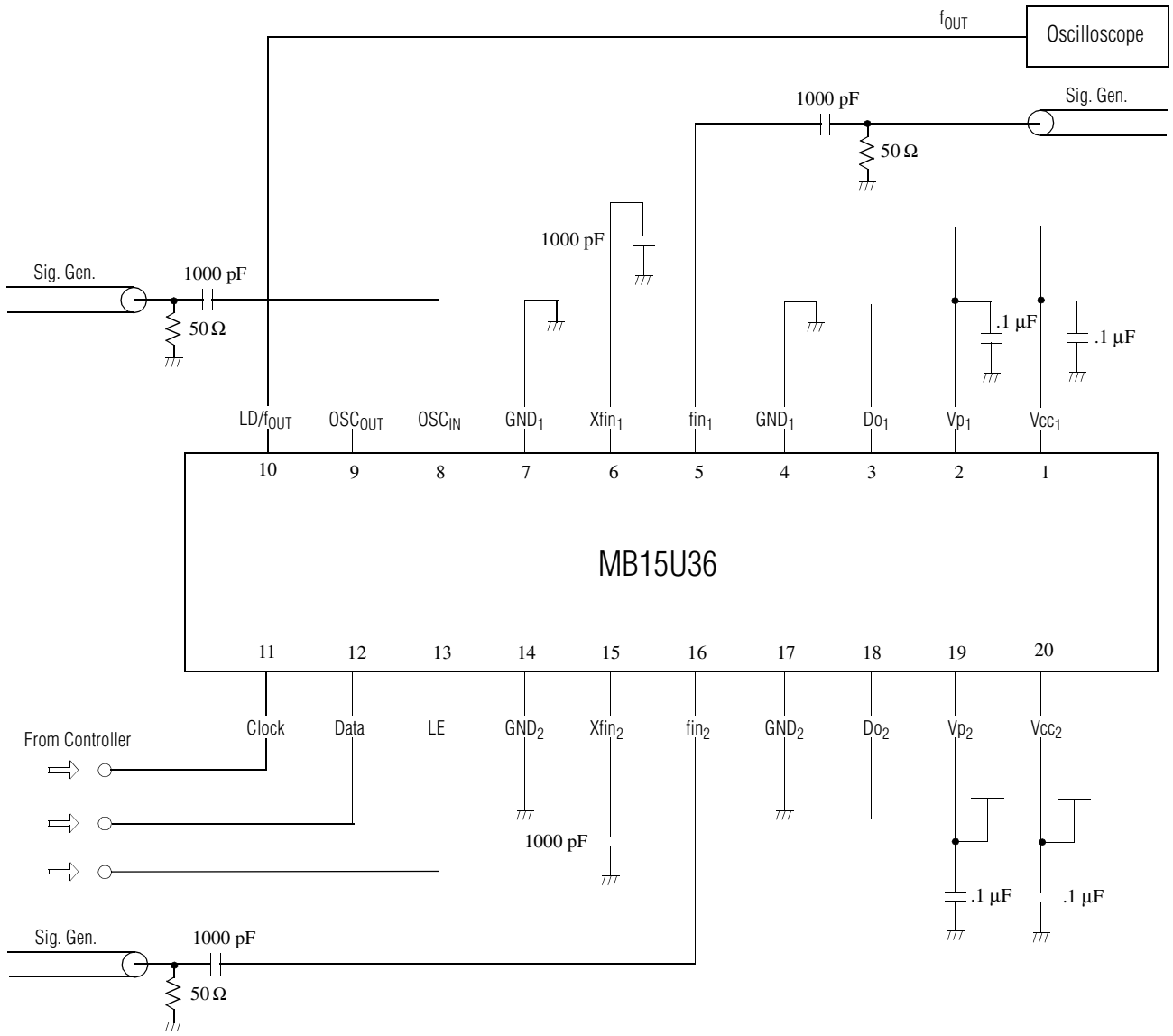
Parameter		Symbol	Condition		Value Min.	Value Typ.	Value Max.	Unit
Power supply current		Icc1*1	fin_1 = 2000 MHz fosc = 12 MHz	Vcc = 5V	–	6.0	–	mA
				Vcc = 3V	–	3.5	–	mA
		Icc2*2	fin_2 = 1200 MHz fosc = 12 MHz	Vcc = 5V	–	3.0	–	mA
				Vcc = 3V	–	2.5	–	mA
Power saving current		Ips_1	Vcc1 current at PS $bit_{RF1, RF2}$ ="H"		–	0.1*3	10	µA
		Ips_2	Vcc1 current at PS bit $_{RF2}$ ="H"		–	0.1*3	10	µA
Operating frequency		fin_1*4	RF1-PLL		100	–	2000	MHz
		fin_2*4	RF2-PLL		50	–	1200	MHz
		f_{OSC}	500mVp-p minimm		3	–	40	MHz
Input sensitivity	$fin_{RF1-PLL}$	$Pfin_{RF1-PLL}$	50Ω load system (Refer to measurement circuit.)		–10	–	+2	dBm
	$fin_{RF2-PLL}$	$Pfin_{RF2-PLL}$	50Ω load system (Refer to measurement circuit.)		–10	–	+2	dBm
	OSC_{IN}	V_{OSC}			0.5	–	V_{CC}	Vp-p
Input voltage	Data, Clock, LE	V_{IH}			$V_{CC} \times 0.8$	–	–	V
		V_{IL}			–	–	$V_{CC} \times 0.2$	V
Input current	Data, Clock, LE	I_{IH}*5	V_{IH} = Vcc		–1.0	–	+1.0	µA
		I_{IL}*5	V_{IL} = Vcc		–1.0	–	+1.0	µA
	OSC_{IN}	I_{IH}	V_{IH} = Vcc		0	–	+100	µA
		I_{IL}*5	V_{IL} = Vcc		–100	–	0	µA
Output voltage	LD/f_{OUT}	V_{OH}	I_{OH} = –1 mA		Vcc –0.4	–	–	V
		V_{OL}	I_{OL} = 1 mA		–	–	0.4	V
	Do_1, Do_2	V_{DOH}	I_{OH} = –0.5 mA		Vcc –0.4	–	–	V
		V_{DOL}	I_{OL} = 0 .5 mA		–	–	0.4	V
High impedance cutoff current	Do_1, Do_2	I_{OFF}	V_{CC} = Vp = 5.0V 0.5V ≤ V_{DO} ≤ Vp – 0.5V		–	–	3.0	nA
Output current	LD/f_{OUT}	I_{OH}*5	V_{CC} = 5.0V		–1.0	–	–	mA
		I_{OL}	V_{CC} = 5.0V		–	–	1.0	mA
	Do_1, Do_2	I_{DOH}*5	V_{CC} = Vp = 5.0V	CMC bit = "L"	–	–1.25	–	mA
			V_{CC} = Vp = 3.0V	CMC bit = "L"	–	–1.0	–	mA
		I_{DOL}	V_{CC} = Vp = 5.0V	CMC bit = "L"	–	1.25	–	mA
			V_{CC} = Vp = 3.0V	CMC bit = "L"	–	1.0	–	mA
		I_{DOH}*5	V_{CC} = Vp = 5.0V	CMC bit = "H"	–	–5.0	–	mA
			V_{CC} = Vp = 3.0V	CMC bit = "H"	–	–4.0	–	mA
		I_{DOL}	V_{CC} = Vp = 5.0V	CMC bit = "H"	–	5.0	–	mA
			V_{CC} = 3.0V	CMC bit = "H"	–	4.0	–	mA

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Charge pump current characteristics	I_{DOL}/I_{DOH}	I_{DOMT}*6	$V_{DO} = V_{CC}/2$	–	3	–	%
	I_{DO} vs V_{DO}	I_{DOVD}*7	$0.5V \leq V_{DO} \leq V_{CC} - 0.5V$	–	15	–	%
	I_{DO} vs Ta	I_{DOTA}*8	$-40 \times C \leq Ta \leq +85°C$, $V_{DO} = Vp/2$	–	10	–	%

*1: Conditions: Vcc_1 = 5.0V, Ta = +25°C, in locking state.
*2: Conditions: Vcc_2 = 5.0V, Ta = +25°C, in locking state.
*3: Conditions: Vcc = 5.0V, fOSC = 12.8MHz (-2dBm),Ta = +25°C
*4: AC coupling, 1000pF capacitor is connected under the condition of min. operating frequency.
*5: The symbol "–" (minus) means direction of current flow.
*6: V_{CC} = 5.0 V, Ta = +25°C $(|I_3| - |I_4|)/[(|I_3| + |I_4|)/2] \times 100(\%)$
*7: V_{CC} = 5.0 V, Ta = +25°C $[(|I_2| - |I_1|)/2]/[(|I_1| + |I_2|)/2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})
*8: V_{CC} = 5.0 V, $[|I_{DO(85°C)} - I_{DO(-40°C)}|/2]/[|I_{DO(85°C)} + I_{DO(-40°C)}|/2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})

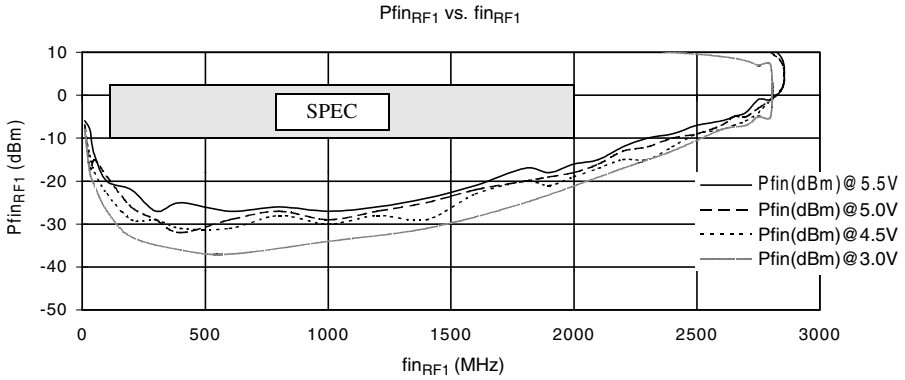


Measurement Circuit (For Measuring Input Sensitivity of fin and OSCin)

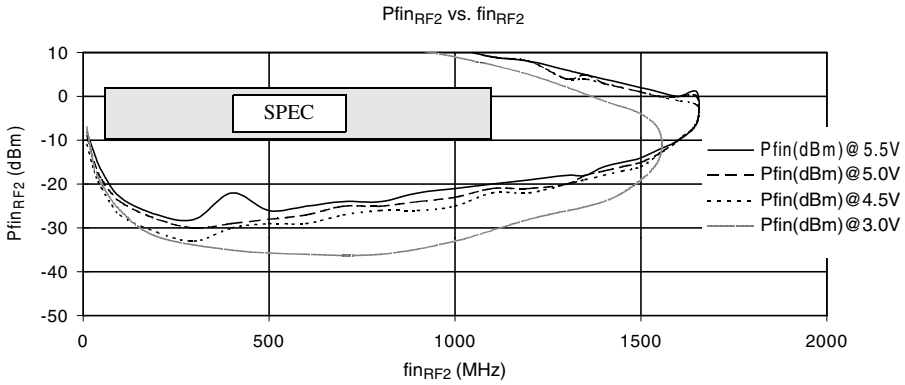


Typical Electrical Characteristics: MB15U36

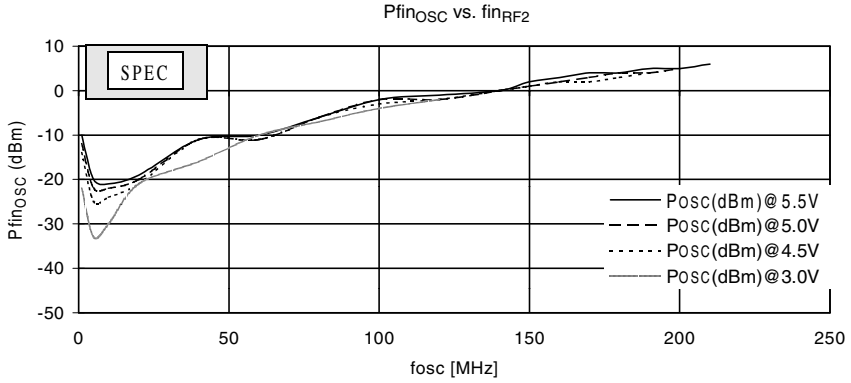
Input Sensivity of fin (RF1) versus Input Frequency



Input Sensivity of fin (RF2) versus Input Frequency



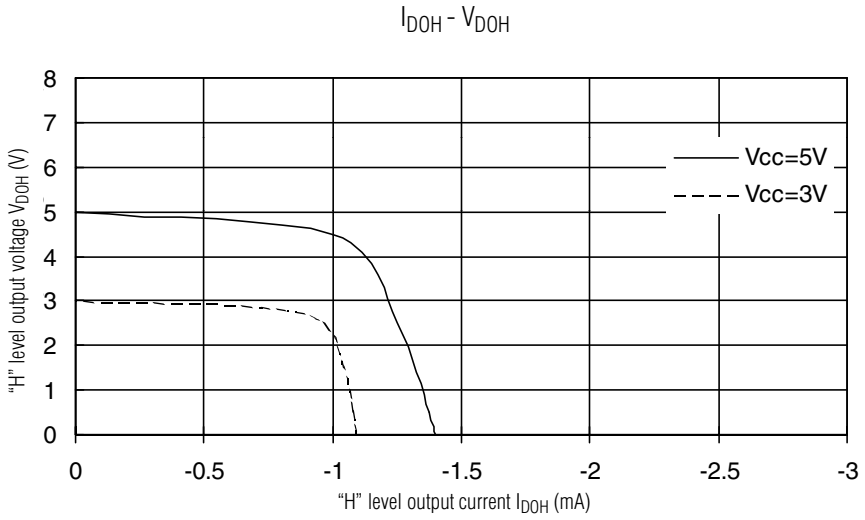
Input Sensivity of OSC_{IN} versus Input Frequency

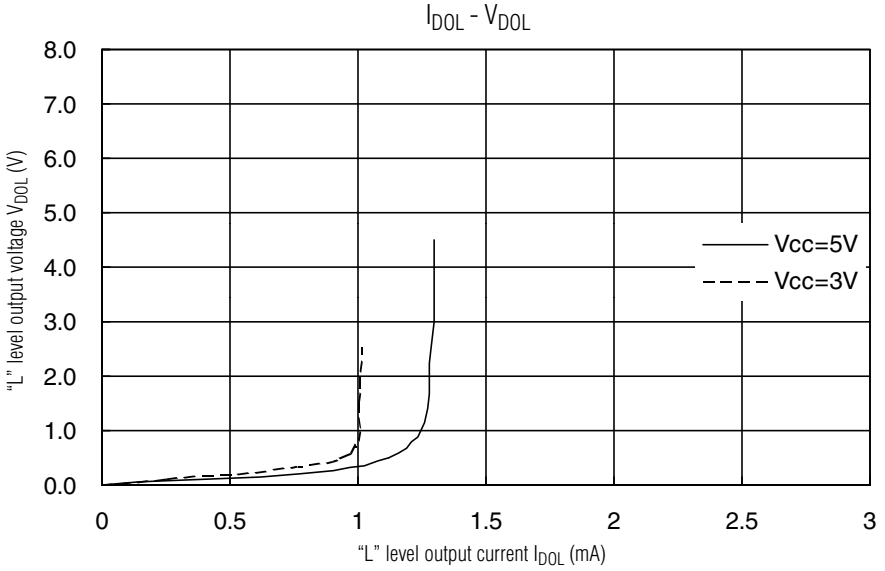


Typical Electrical Characteristics: MB15U36

Conditions: Ta = +25°C

Do output current: 1 x Do mode

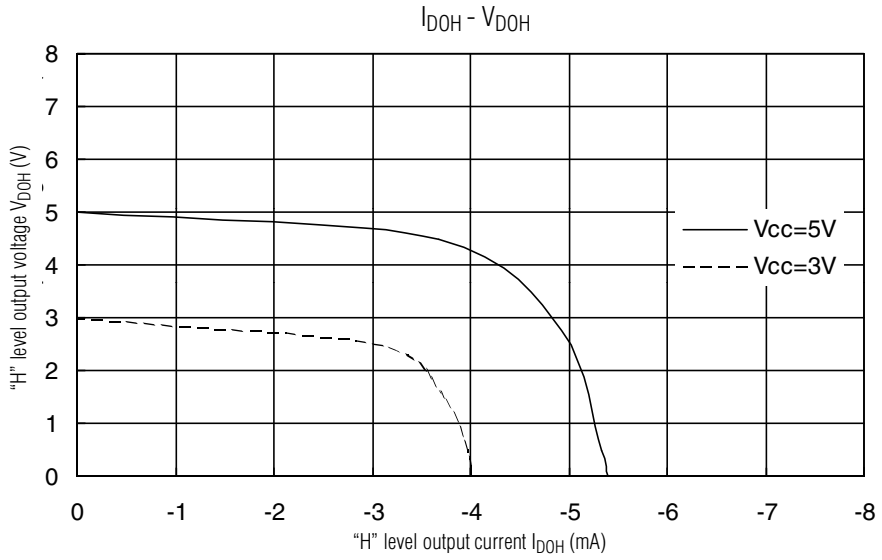


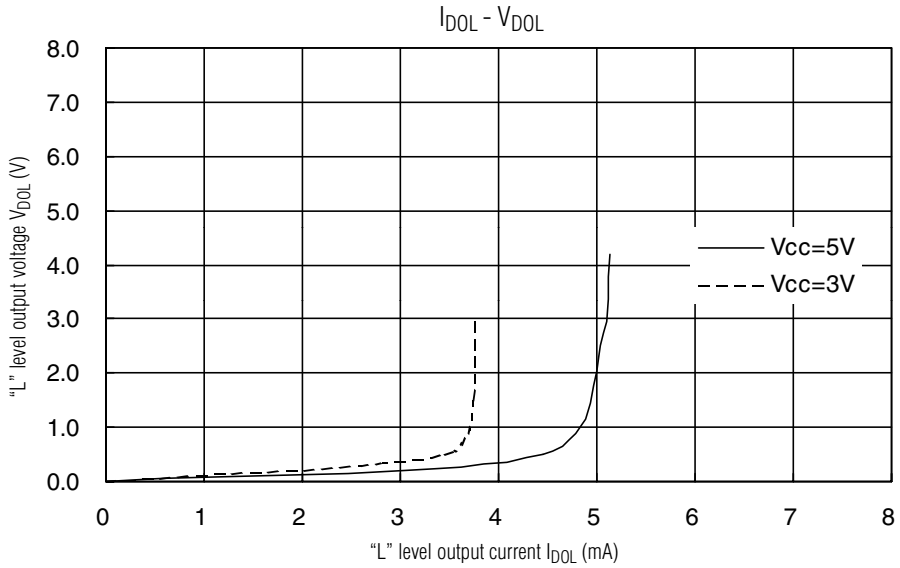


Typical Electrical Characteristics: MB15U36

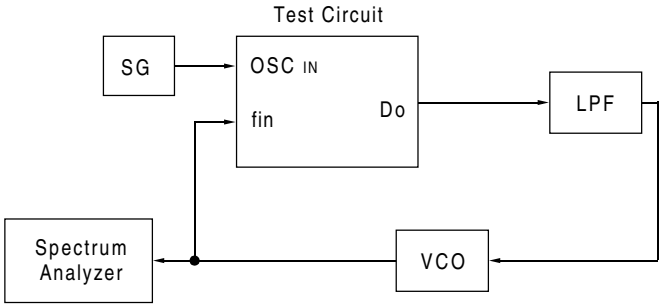
Conditions: Ta = +25°C

Do output current: 4 x Do mode



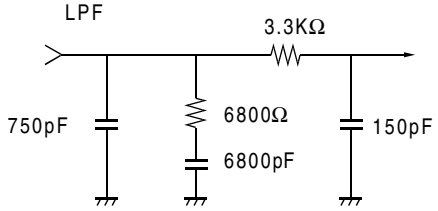


Reference Information: MB15U36



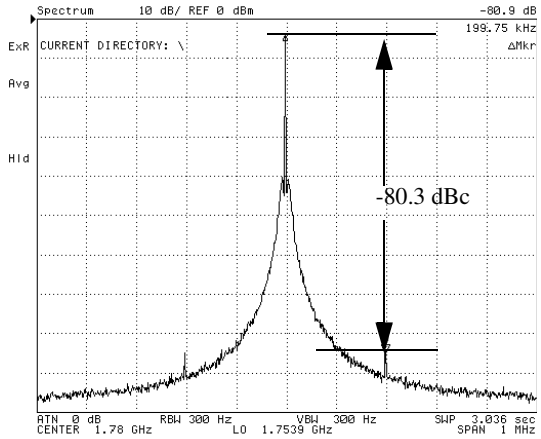
fVCO = 1780 MHz
KV = 58 MHz/V
fr = 200 KHz
fOSC = 10 MHz

VCC = VP = 3.0V
VVCO = 5.0V
Ta = +25 °C
CP: 1mA mode

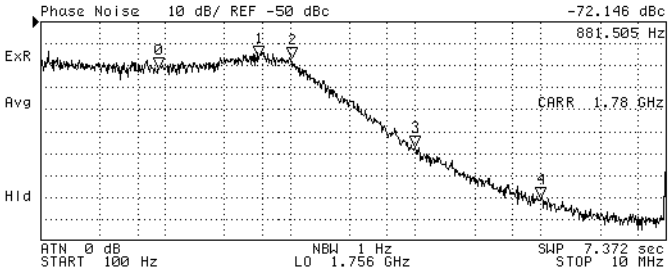


Typical plots measure with the test circuit are shown below. Each plot shows lock up time, phase noise, and reference leakage.

RF PLL Reference Leakage
@ 200 kHz offset = -80.3 dBc

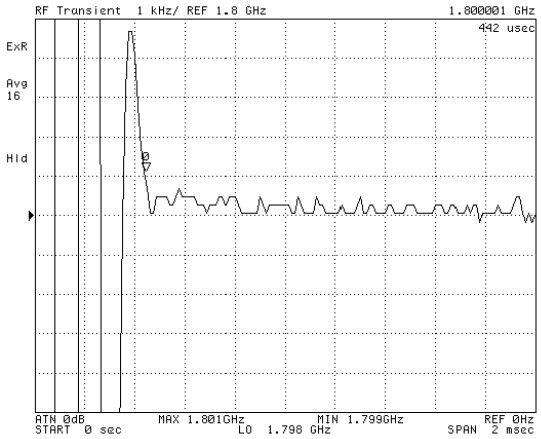


RF PLL Phase Noise
@ max within loop band = -66.5 dBc/Hz

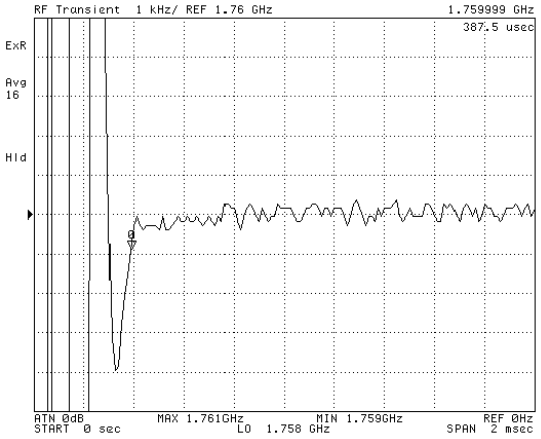


N	SWP PARAM	VAL
0	881.505 Hz	-72.146 dBc
1	5.487057 kHz	-66.501 dBc
2	10 kHz	-67.19 dBc
3	100 kHz	-107.46 dBc
4	1 MHz	-130.83 dBc

RF PLL Lock Up Time = 442µs
(1760.000 MHz → 1800.000 MHz, within ± 1kHz)



RF PLL Lock Up Time = 387µs
(1800.000 MHz → 1760.000 MHz, within ± 1kHz)



Dual PLL Frequency Synthesizer with On-Chip Prescaler

Functional Descriptions

The VCO output frequency can be calculated using the following equation:

$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
M: Preset divide ratio of dual modulus prescaler (64 or 128 for RF1-PLL or RF2-PLL2)
N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC}: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 32,767)

Serial Data Input

Serial data is entered using the Data, Clock, and LE pins. The serial data controls the programmable reference counters and the programmable counters separately.

Binary serial data is entered through the Data pin when the LE pin is held low. One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE signal pin is taken high, entered data is latched into the appropriate counters according to the control bit settings as follows:

Table 1. Control Bits

Control Bits		Destination of Serial Data
CN1	CN2	
L	L	The programmable reference counter for the RF2-PLL
L	H	The programmable reference counter for the RF1-PLL
H	L	The programmable counter and the swallow counter for the RF2-PLL
H	H	The programmable counter and the swallow counter for the RF1-PLL

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
CN1	CN2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	FC	CMC	ZC	LDS	FDS

CNT1, 2	Control bits	[Table 1]
R1 to R15	Divide ratio setting bits for the programmable reference counter (3 to 32,767)	[Table 2]
FC	Phase control bit for the phase detector	[Table 3]
CMC	Charge pump current select bit	[Table 4]
ZC	Forced high impedance control for the charge pump	[Table 5]
LDS/FDS	LD/f_{OUT} signal select bits	[Table 6]

Note: Input Data with MSB first.

Functional Descriptions

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
CN1	CN2	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	SW	PS

CNT1, 2	Control bits	[Table 1]
N1 to N11	Divide ratio setting bits for the programmable counter (3 to 2,047)	[Table 7]
A1 to A7	Divide ratio setting bits for the swallow counter (0 to 127)	[Table 8]
SW	Divide ratio setting bit for the prescalers (64/65 or 128/129 for the RF1-PLL and RF2-PLL)	[Table 9]
PS	Power saving mode control bit	[Table 10]

Note: Input Data with MSB first.

Table 2. Binary 15-bit Programmable Reference Counter Data Setting

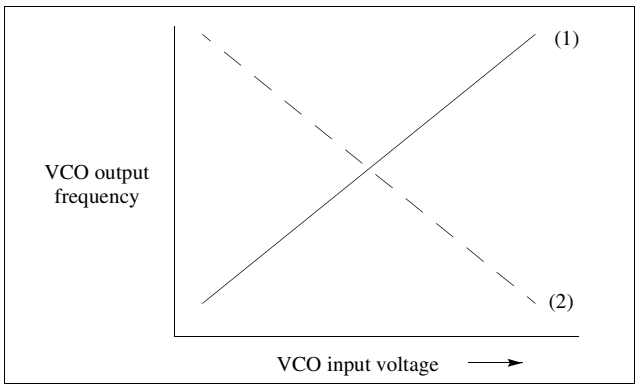
Divide Ratio (R)	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 3. Phase Comparator Phase Switching Data Setting

	$Do_{RF1\text{-}PLL,RF2\text{-}PLL}$	
	$FC_{RF1\text{-}PLL,RF2\text{-}PLL}$ = "H"	$FC_{RF1\text{-}PLL,RF2\text{-}PLL}$ = "L"
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	(1)	(2)

Notes: 1) Z = High-impedance
2) The FC bit should be set depending upon the VCO and LPF polarity



Functional Descriptions

Table 4. Charge Pump Current Setting (CMC)

CMC	Current Value
L	1 x Do
H	4 x Do

Table 5. Charge Pump Output Impedance Setting (ZC)

ZC	Do Output Impedance
L	Normal output
H	High impedance

Table 6. LD/fout Output Select Data Setting

LDS_{RF1}	LDS_{RF2}	FDS_{RF1}	FDS_{RF2}	LD/f_{OUT} Output Signal
L	L	L	L	Disabled
L	H	L	L	LD signal (RF2 lock detect)
H	L	L	L	LD signal (RF1 lock detect)
H	H	L	L	LD signal (RF1/RF2 lock detect)
X	L	L	H	f_{OUT} (Output fr_{RF2})
X	L	H	L	f_{OUT} (Output fr_{RF1})
X	H	L	H	f_{OUT} (Output fp_{RF2})
X	H	H	L	f_{OUT} (Output fp_{RF2})
L	L	H	H	Fastlock
L	H	H	H	RF2 counter reset
H	L	H	H	RF1 counter reset
H	H	H	H	RF1/RF2 counter reset

Note: X = Don't care

Table 7. Binary 11-bit Programmable Counter Data Setting

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Functional Descriptions

Table 8. Binary 7-bit Swallow Counter Data Setting

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

Table 9. Prescaler Data Setting (SW)

Prescaler Divide Ratio	SW = "L"	SW = "H"
RF1-PLL	64/65	128/129
RF2-PLL	64/65	128/129

Power-Saving Mode (Intermittent Mode Control)

- The intermittent mode control circuit greatly reduces the PLL power consumption by shuting down various internal functions, as shown in Table 10, depending upon the settings of the power save (PS) bits. Setting the PS bits to "H" enters the corresponding PLL into the power-saving mode. See the Electrical Characteristics chart for the specific value of current when in the power-saving mode.
- The phase detector output, Do, becomes high impedance.
- Serial data can be entered while in the power-saving mode.
- Setting the PS pins "L" releases the power-saving mode, returning the selected PLL to normal operation.

Note: When power (V_{CC}) is first applied, the device must be in standby mode, PS = High, for at least 1µs.

Table 10. Power Save Internal Shutdown Logic (PS)

PS_{RF2}	PS_{RF1}	RF2-PLL Counters	RF1-PLL Counters	OSC Input Buffer
H	H	OFF	OFF	OFF
L	H	ON	OFF	ON
H	L	OFF	ON	ON
L	L	ON	ON	ON

Serial Data Input Timing

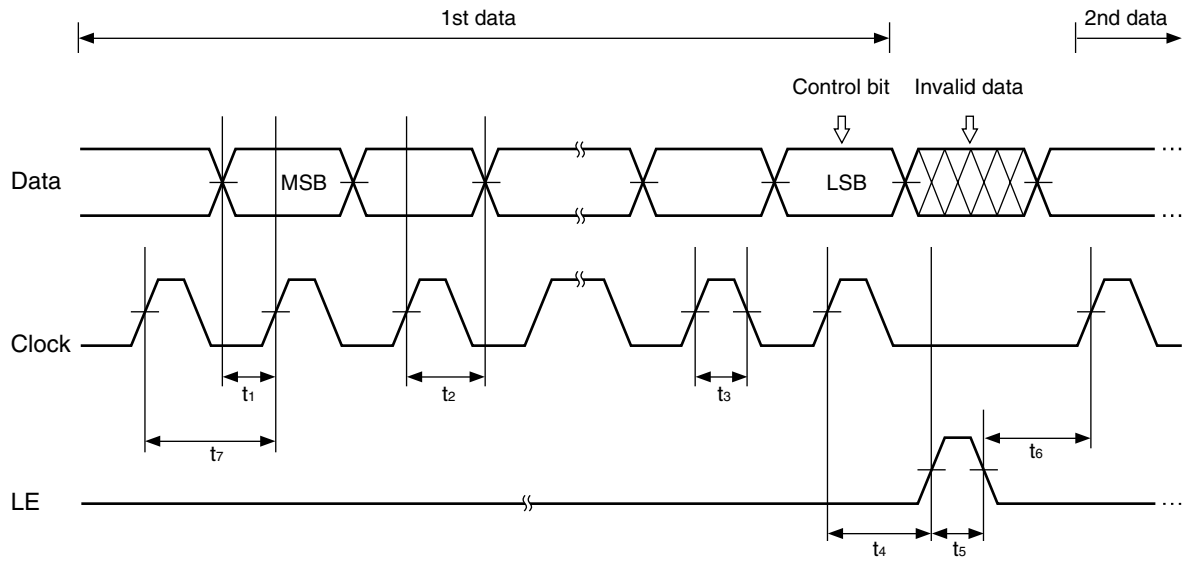
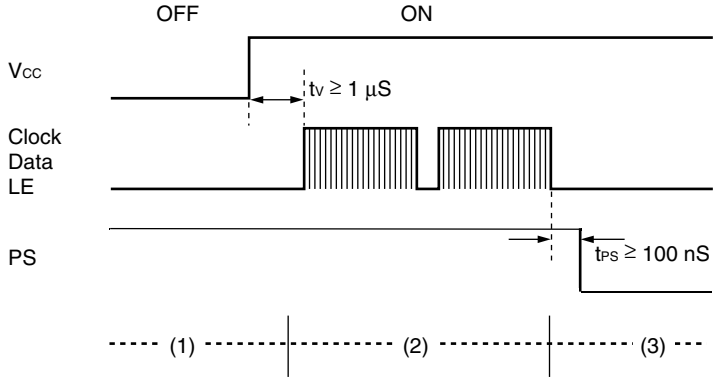


Table 11. Timing Parameters

Parameter	Min.	Typ.	Max.	Unit	Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns	t5	100	–	–	ns
t2	20	–	–	ns	t6	20	–	–	ns
t3	30	–	–	ns	t7	100	–	–	ns
t4	30	–	–	ns					

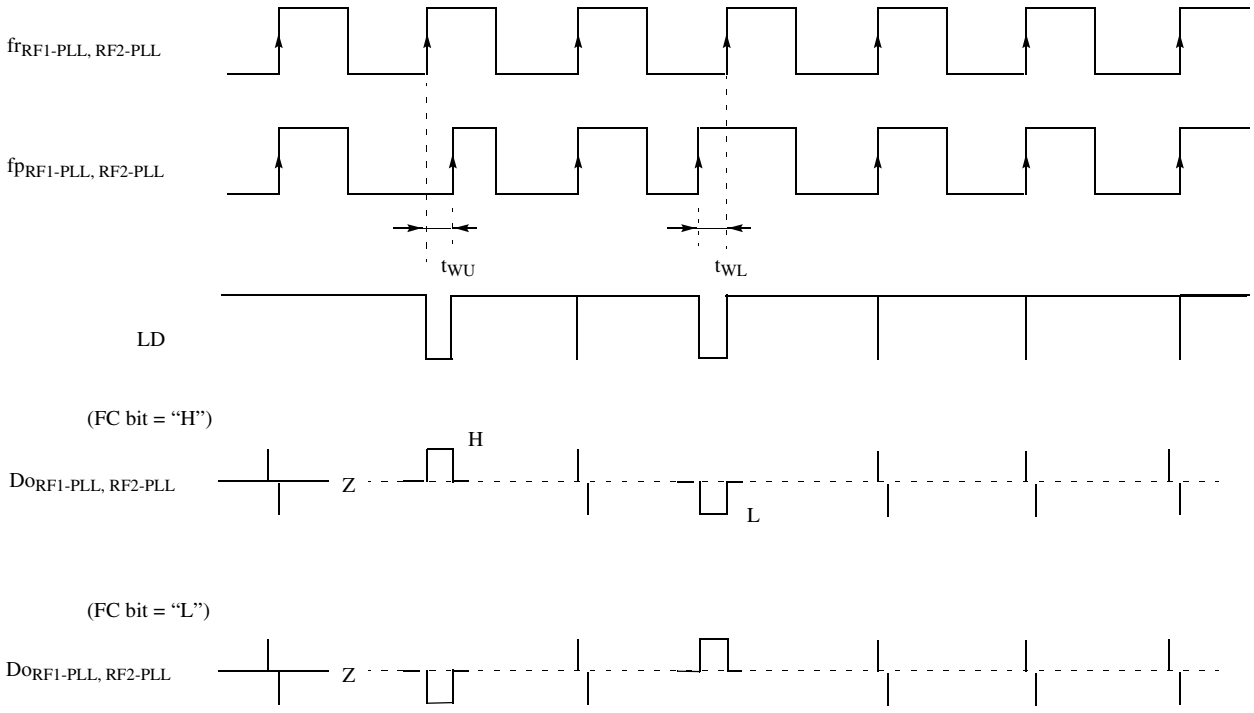
Notes: 1) On the rising edge of the clock, one bit of the data is transferred into the shift register.
2) LE should be set to "L" when the data is transferred into the shift register.

Power-ON Timing



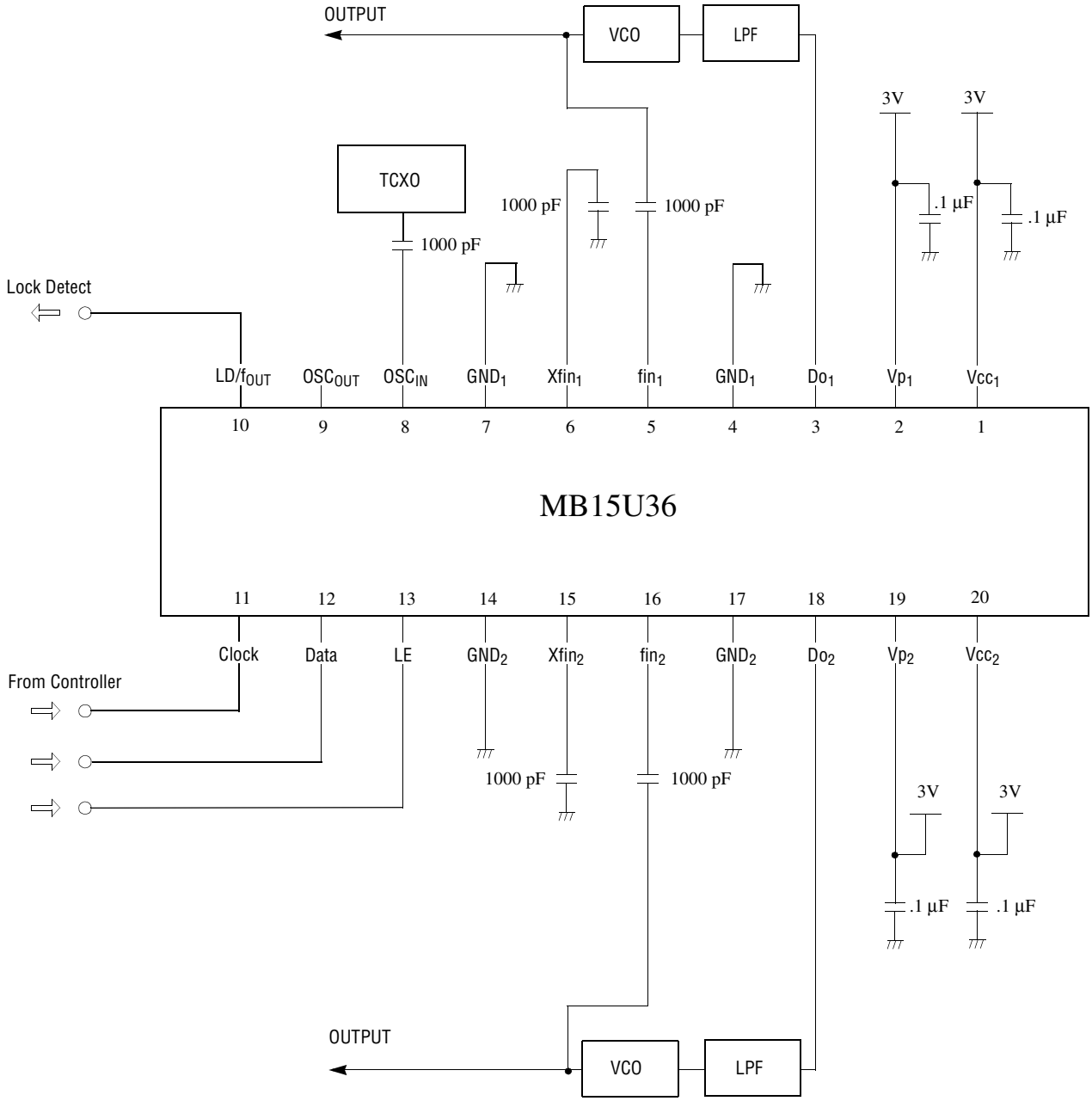
(1) PS = H (power-saving mode) at Power-ON
(2) Input serial data 1µs later after power supply remains stable ($V_{CC} \geq 2.2V$).
(3) Release power-saving mode (PS: H Æ L) 100ns later after setting serial data.

Phase Detector Output Waveform



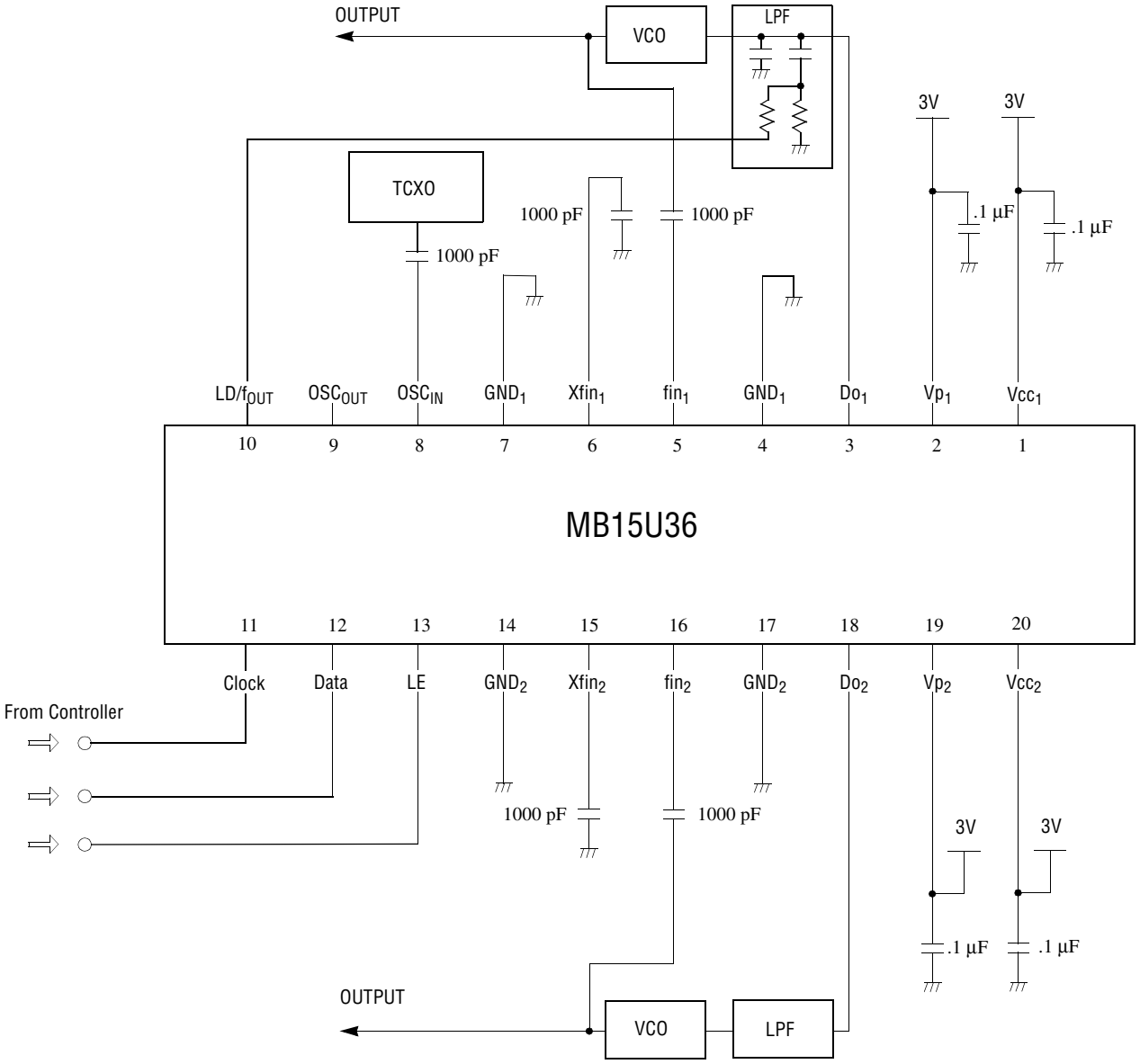
Notes: 1) Phase error detection range: -2π to $+2\pi$
2) Pulses on Do signal during locked state are output to prevent dead zone.

Application Example



Notes: 1) Package Type: 20-pin SSOP
2) Clock, Data, LE: Insert a pull-down or pull-up resistor as needed to prevent oscillation when the terminals are left open.

Application Example: Fastlock Mode



Notes: 1) Package Type: 20-pin SSOP

2) Clock, Data, LE: Insert a pull-down or pull-up resistor as needed to prevent oscillation when the terminals are left open

3) The Fastlock mode is controlled by the LDS/FDS bits and the CMC_{RF1} bit. When the CMC_{RF1} bit is set to "H" (the RF1 charge pump current is increased 4x normal mode), the LD/fout pin (open drain output) is "L", enabling the parallel resistor in the loop filter. This effectively increases the LPF bandwidth, allowing the loop to lock faster. After the loop has locked onto a new frequency, the CMC_{RF1} bit is set to "L", forcing the LD/fout output pin into a high impedance state and returning the LPF bandwidth back to its original value.

Usage Precautions

To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet when transporting a board mounted device.

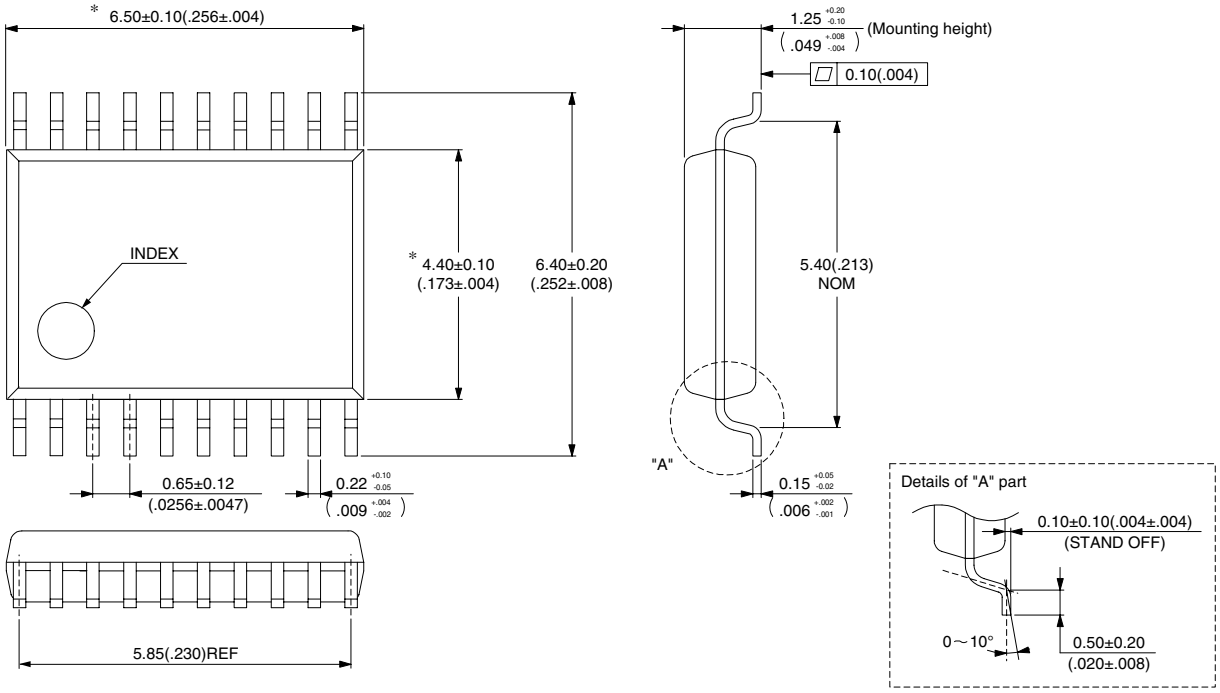
Ordering Information

Part Number	Package
MB15U36PFV	20-pin, Plastic SSOP (FPT-20P-M03)

Package Dimensions

20-pin, Plastic SSOP
(FPT-20P-M03)

* These dimensions do not include resin protrusion



Dimensions in mm (inches)

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