

Dual 9-bit D-type flip-flop with reset and enable (3-State)

MB2823

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset

- Output capability: +64mA–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The MB2823 dual bus interface register is designed to eliminate the extra packages required to buffer existing registers and

provide extra data width for wider data/address paths of buses carrying parity.

The MB2823 has two 9-bit wide buffered registers with Clock Enable ($\overline{nCE}$) and Master Reset ($\overline{nMR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

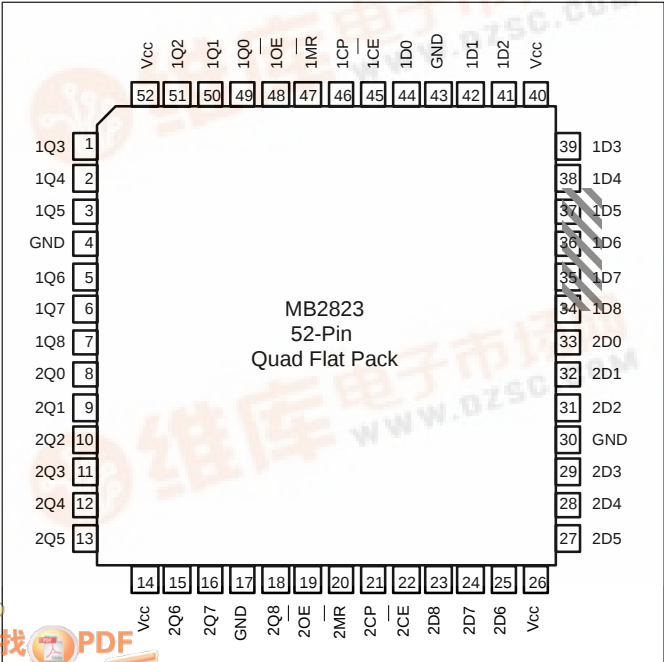
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; $GND = 0V$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	$C_L = 50\text{pF}$; $V_{CC} = 5V$	4.6	ns
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_O = 0V$ or V_{CC} ; 3-state	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5V$	500	nA

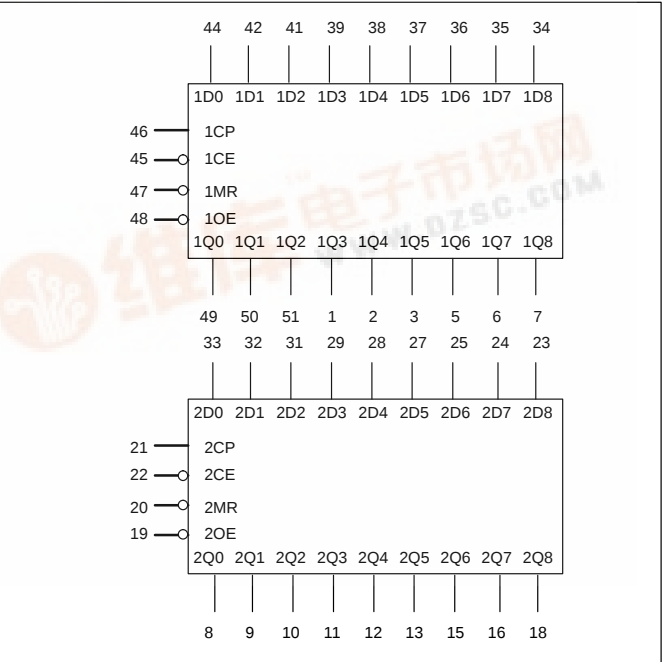
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
52-Pin Plastic Quad Flat Pack	-40°C to $+85^{\circ}\text{C}$	MB2823BB	1418B

PIN CONFIGURATION



LOGIC SYMBOL



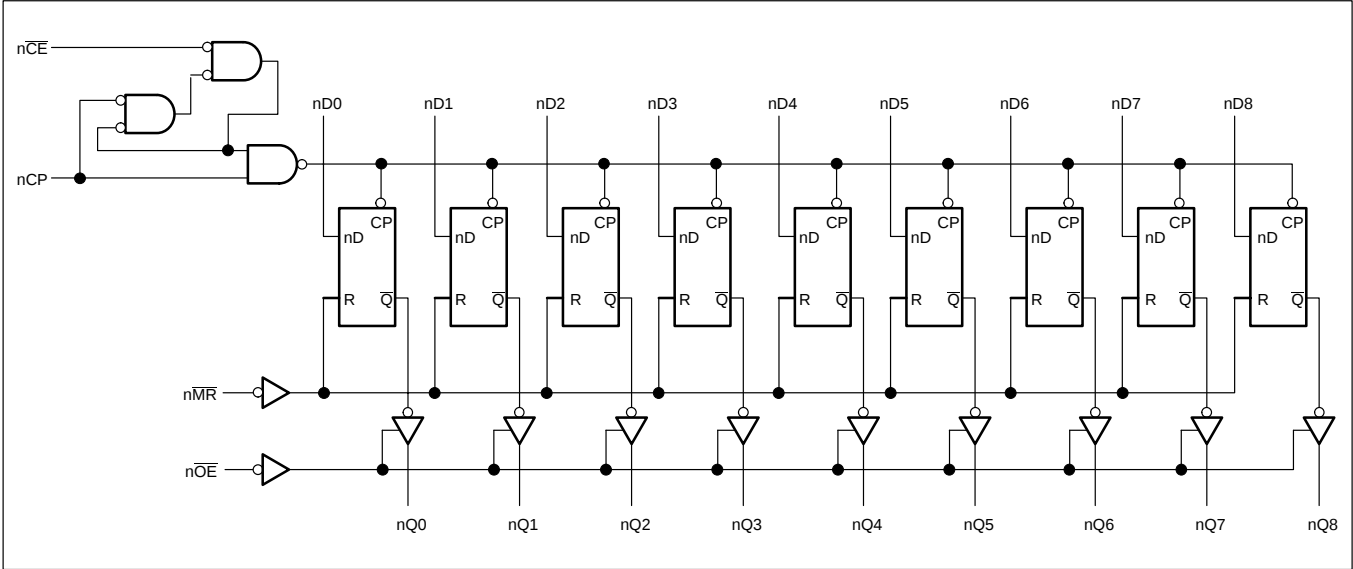
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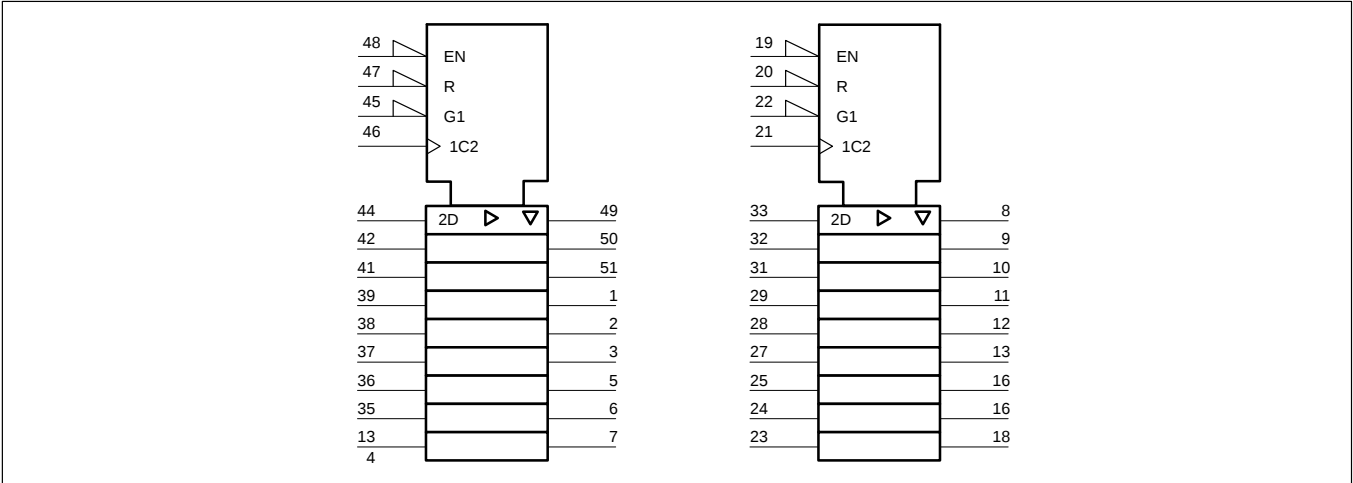
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
48, 19	1OE, 2OE	Output enable input (active-Low)
44, 42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24, 23	1D0-1D8 2D0-2D8	Data inputs
49, 50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 18	1Q0-1Q8 2Q0-2Q8	Data outputs
46, 21	1CP, 2CP	Clock pulse input (active rising edge)
45, 22	1CE, 2CE	Clock enable input (active-Low)
47, 20	1MR, 2MR	Master reset input (active-Low)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	VCC	Positive supply voltage

LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



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FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
nOE	nMR	nCE	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	⊕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level

h = High voltage level one set-up time prior to the Low-to-High clock transition

L = Low voltage level

l = Low voltage level one set-up time prior to the Low-to-High clock transition

NC = No change

X = Don't care

Z = High impedance "off" state

↑ = Low to High clock transition

⊕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		–0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	–18	mA
V _I	DC input voltage ³		–1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	–50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	–0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		–65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level input voltage		0.8	V
I _{OH}	High-level output current		–32	mA
I _{OL}	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	–40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = −18mA		−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³	V _{CC} = 5.5V; I _{OL} = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} , V _{OE} = Don't care		±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		−5.0	−50		−50	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	−50	−70	−180	−50	−180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		120	250		250	μA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		45	68		68	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		120	250		250	μA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$ a transition time of up to 100 μsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	1	140	190		140		MHz
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	2.0 2.5	3.8 4.2	5.1 5.6	2.0 2.5	5.7 6.1	ns
t _{PHL}	Propagation delay nMR to nQx	2	3.2	5.3	6.6	3.2	7.5	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	4 5	1.3 2.2	3.2 4.0	4.4 5.3	1.3 2.2	5.1 5.9	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	4 5	1.3 1.5	3.3 3.1	4.6 4.4	1.3 1.5	5.1 5.9	ns

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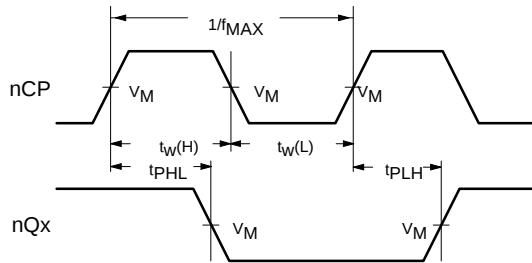
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AC SETUP REQUIREMENTS

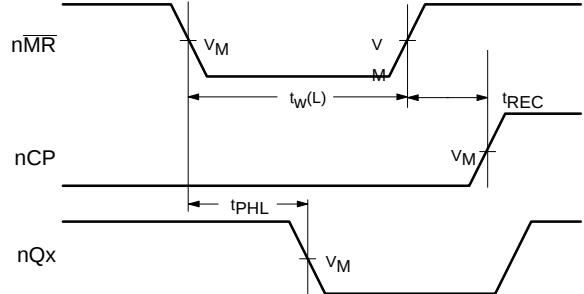
GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time, High or Low nDx to nCP	3	2.0 1.5	0.6 0.2	2.0 1.5	ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold time, High or Low nDx to nCP	3	1.5 1.5	-0.2 -0.5	1.5 1.5	
$t_{\text{W}}(\text{H})$ $t_{\text{W}}(\text{L})$	nCP pulse width High or Low	1	3.0 3.5	1.0 2.3	3.0 3.5	ns
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time, High or Low nCE to nCP	3	1.5 2.0	-0.2 1.0	1.5 2.0	ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold time, High or Low nCE to nCP	3	1.5 1.5	-1.2 0.3	1.5 1.5	ns
$t_{\text{W}}(\text{L})$	nMR pulse width, Low	2	3.0	1.6	3.0	ns
t_{rec}	Recovery time nMR to nCP	2	2.5	0.6	2.5	ns

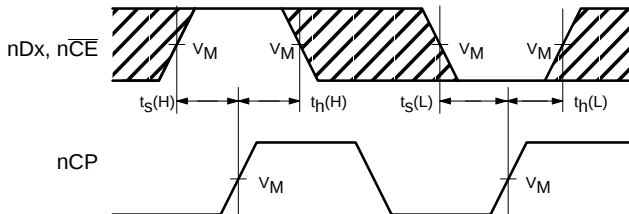
AC WAVEFORMS



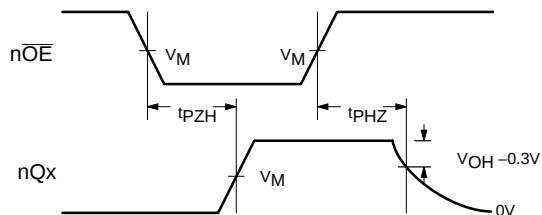
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



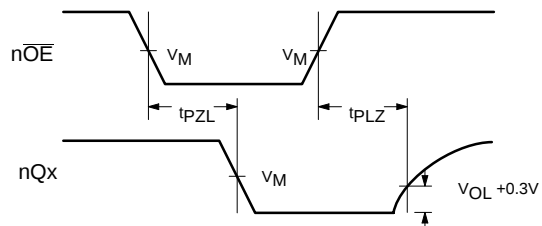
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Setup and Hold Times



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



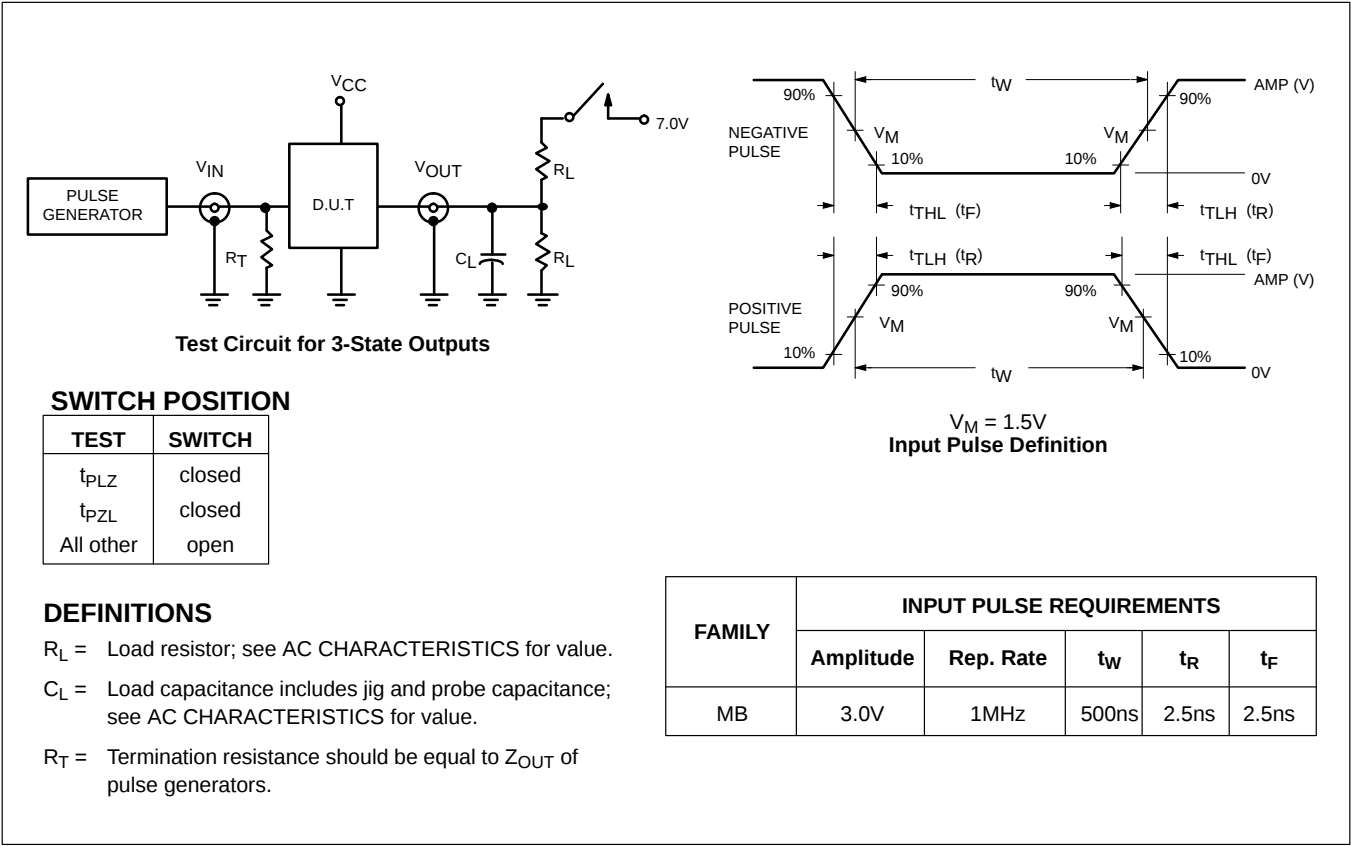
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5\text{V}$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

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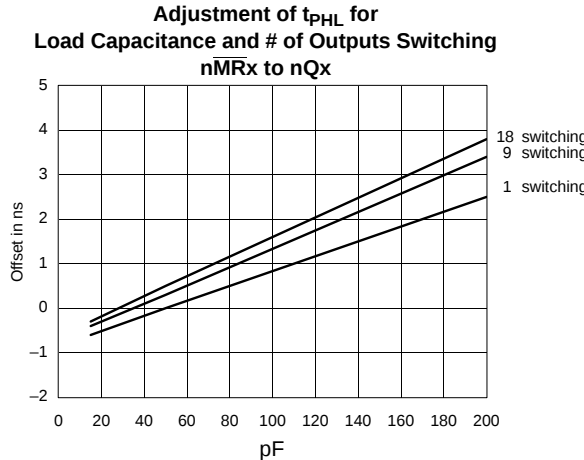
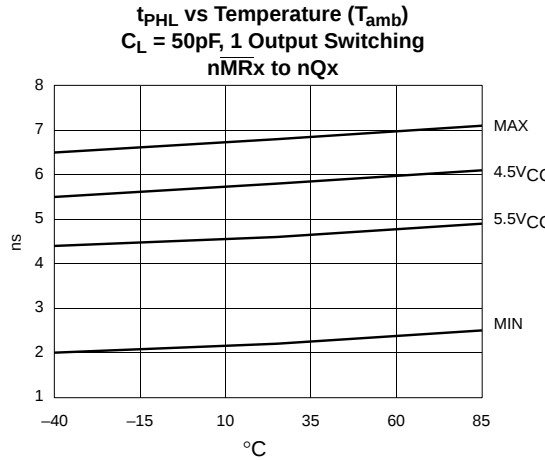
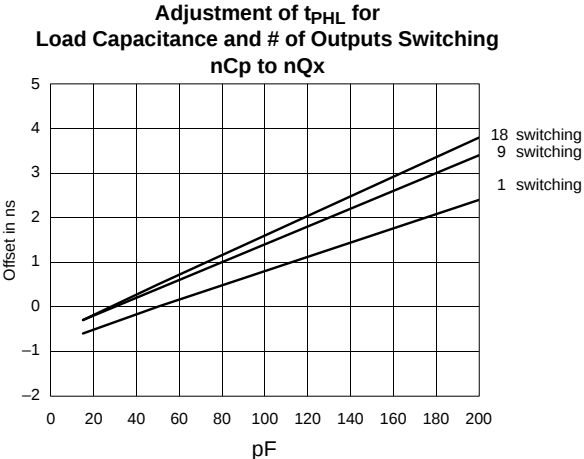
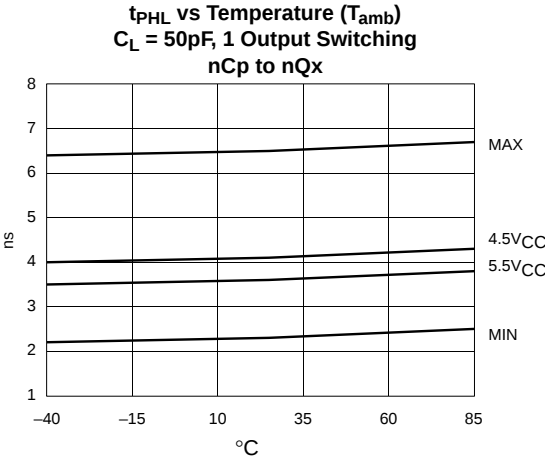
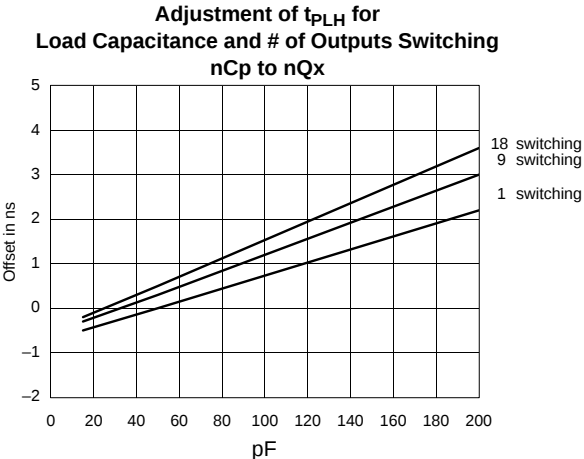
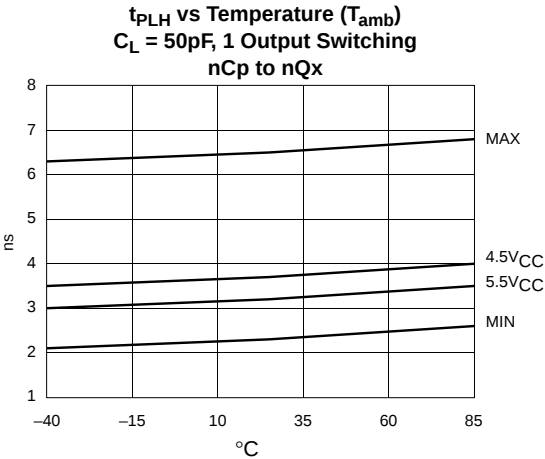
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TEST CIRCUIT AND WAVEFORM



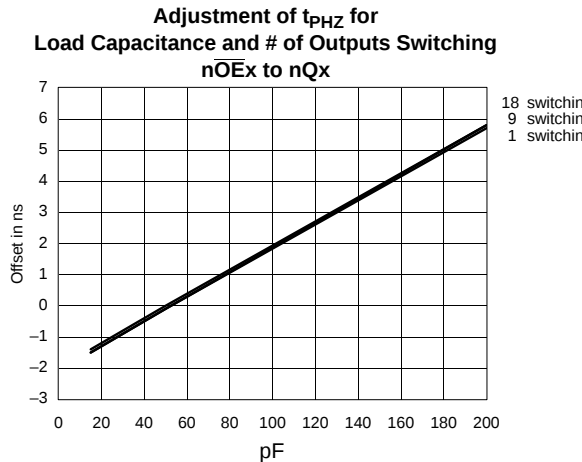
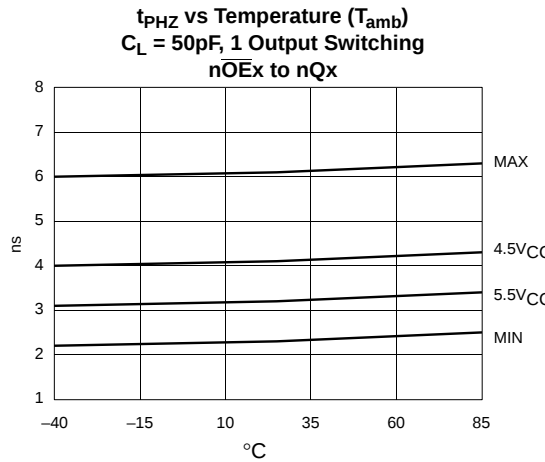
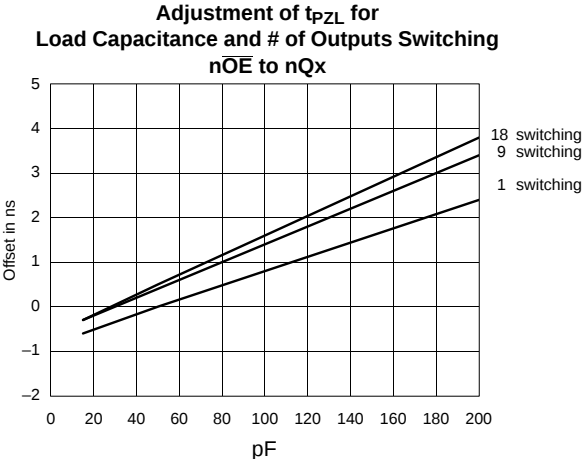
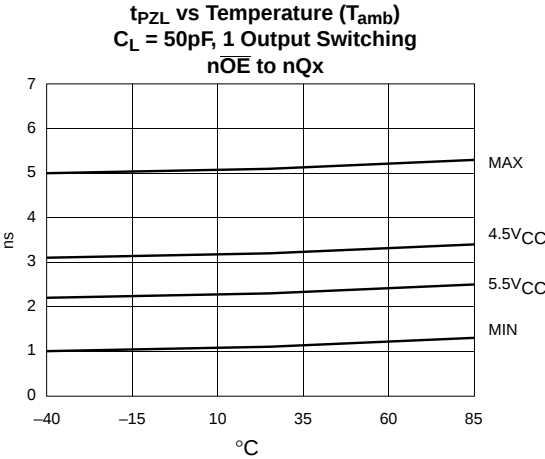
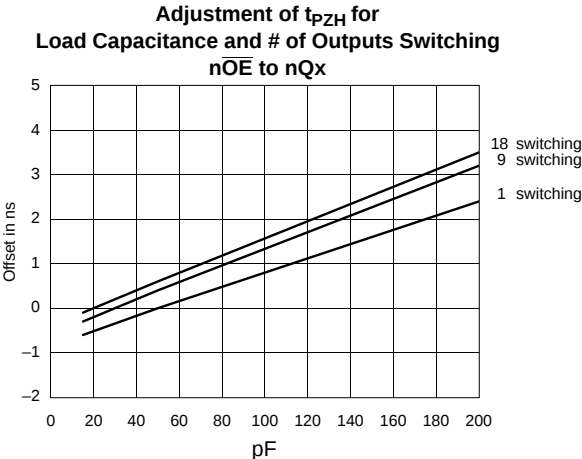
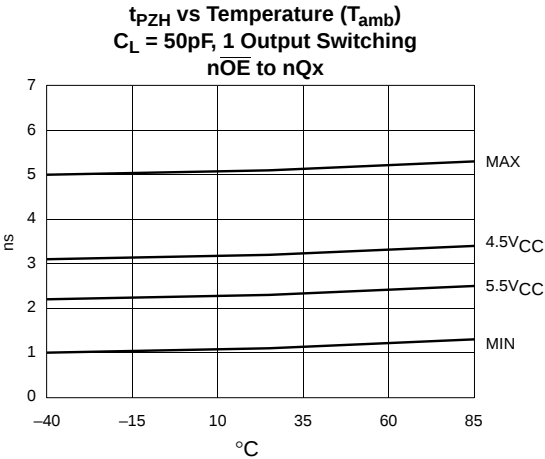
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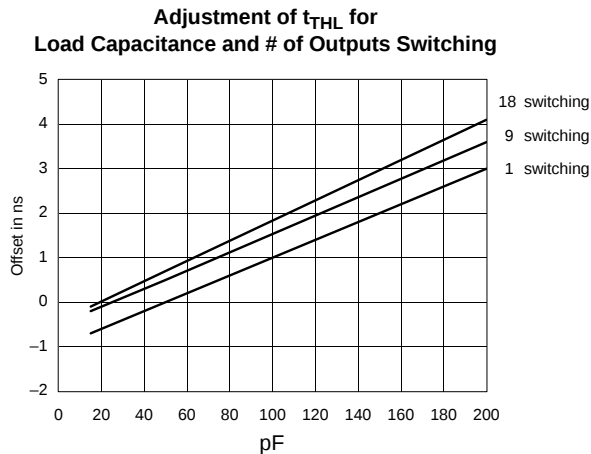
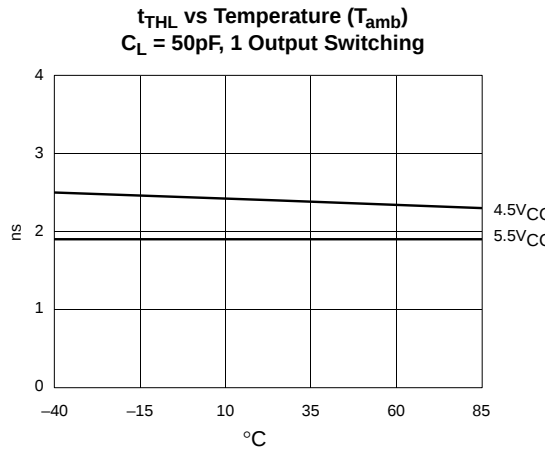
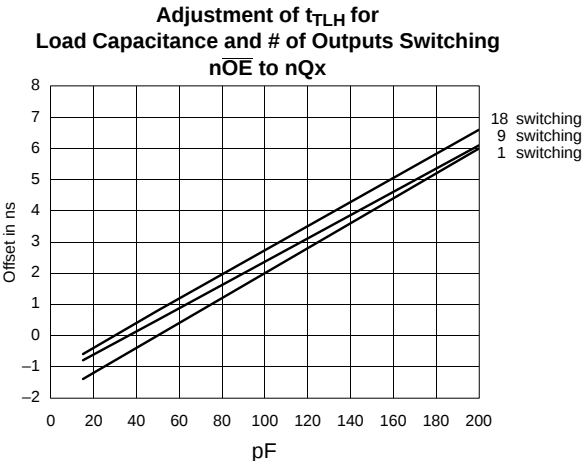
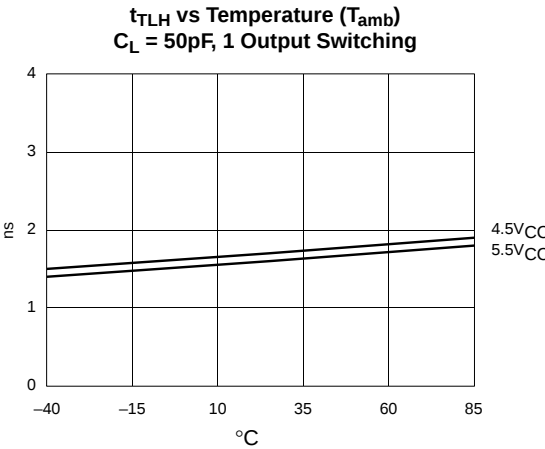
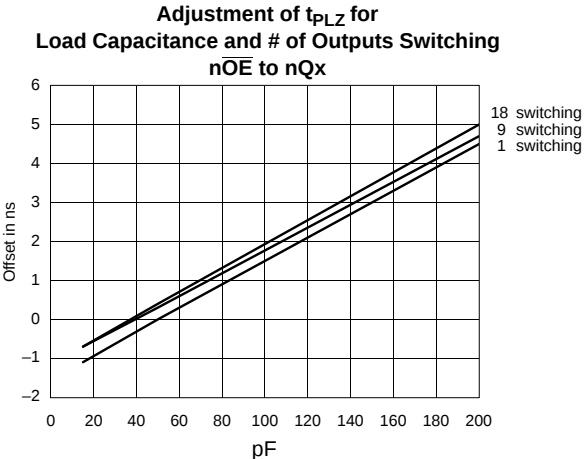
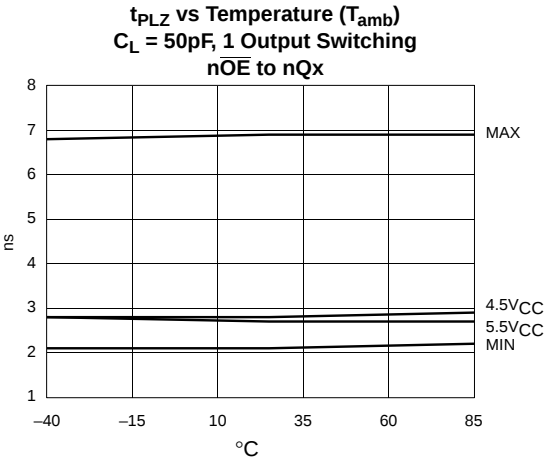
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