FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27402-2E

ASSP

POWER-VOLTAGE MONITORING IC WITH WATCHDOG TIMER

MB3793-42/30

DESCRIPTION

The MB3793 is an integrated circuit to monitor power voltage; it incorporates a watchdog timer.

A reset signal is output when the power is cut or falls abruptly. When the power recovers normally after resetting, a power-on reset signal is output to microprocessor units (MPUs). An internal watchdog timer with two inputs for system operation diagnosis can provide a fail-safe function for various application systems.

Two models with detection voltages of 4.2 and 3.0 V are available. There is also a mask option that can detect voltages of 4.9 to 3.0 V in 0.1-V steps.

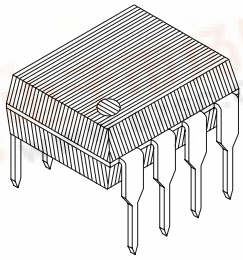
The model numbers are MB3793-42 or -30 corresponding to the detected voltage. The model number and package code are as shown below.

Model No.	Package code	Detection voltage
MB3793-42	3793-A	4.2 V
MB3793-30	3793-N	3.0 V

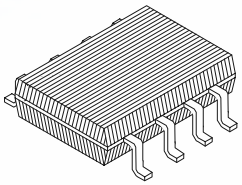
FEATURES

- Precise detection of power voltage fall: ±2.5%
- Detection voltage with hysteresis
- Low power dispersion: ICC = 27 µA (reference)
- Internal dual-input watchdog timer
- Watchdog-timer halt function (by inhibition pin)
- Independently-set watchdog and reset times
- Mask option for detection voltage (4.9 to 3.0 V, 0.1-V steps)

8-PIN PLASTIC DIP
(DIP-8P-M01)



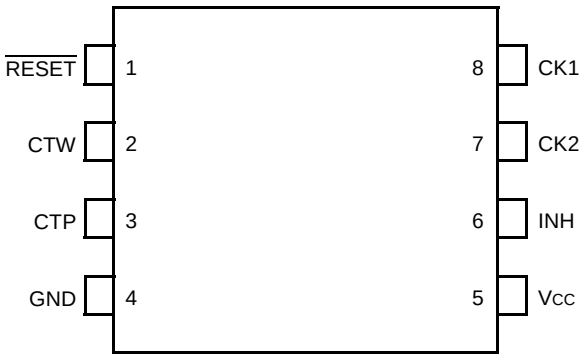
8-PIN PLASTIC SOL
(FPT-8P-M02)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ PIN ASSIGNMENT

(TOP VIEW)

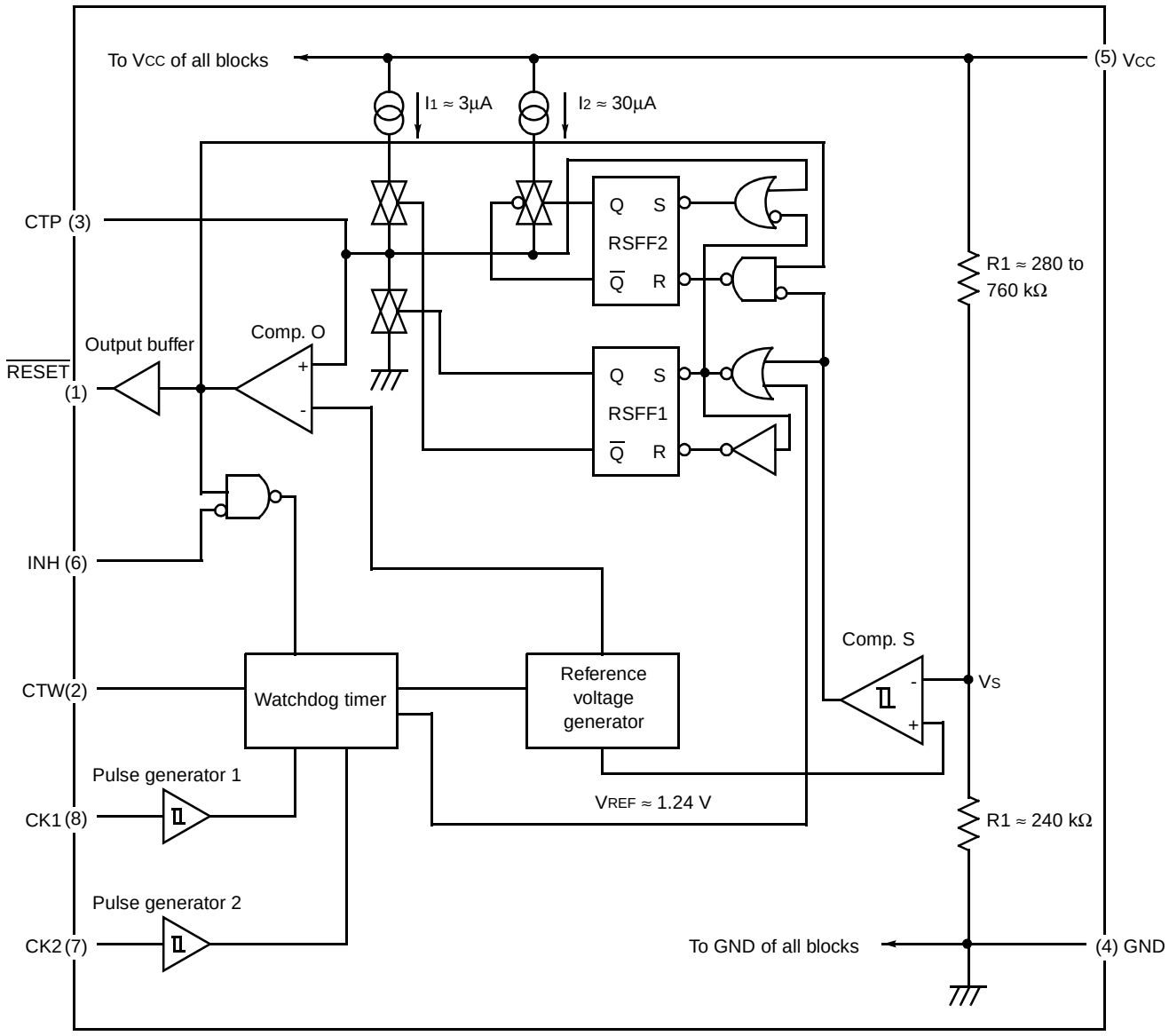


(DIP-8P-M01)
(FPT-8P-M02)

■ PIN DESCRIPTION

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$\overline{\text{RESET}}$	Outputs reset	5	V_{CC}	Power supply
2	CTW	Sets monitoring time	6	INH	Inhibits watchdog timer function
3	CTP	Sets power-on reset hold time	7	CK2	Inputs clock 2
4	GND	Ground	8	CK1	Inputs clock 1

■ BLOCK DIAGRAM



■ BLOCK FUNCTIONS

1. Comp. S

Comp. S is a comparator with hysteresis to compare the reference voltage with a voltage (V_S) that is the result of dividing the power voltage (V_{CC}) by resistors 1 and 2. When V_S falls below 1.24 V, a reset signal is output. This function enables the MB3793 to detect an abnormality within 1 µs when the power is cut or falls abruptly.

2. Comp. O

Comp. O is a comparator to control the reset signal ($\overline{RESET}$) output and compares the threshold voltage with the voltage at the CTP pin for setting the power-on reset hold time. When the voltage at the CTP pin exceeds the threshold voltage, resetting is canceled.

3. Reset output buffer

Since the reset ($\overline{RESET}$) output buffer has CMOS organization, no pull-up resistor is needed.

4. Pulse generator

The pulse generator generates pulses when the voltage at the CK1 and CK2 clock pins changes to High from Low level (positive-edge trigger) and exceeds the threshold voltage; it sends the clock signal to the watchdog timer.

5. Watchdog timer

The watchdog timer can monitor two clock pulses. Short-circuit the CK1 and CK2 clock pins to monitor a single clock pulse.

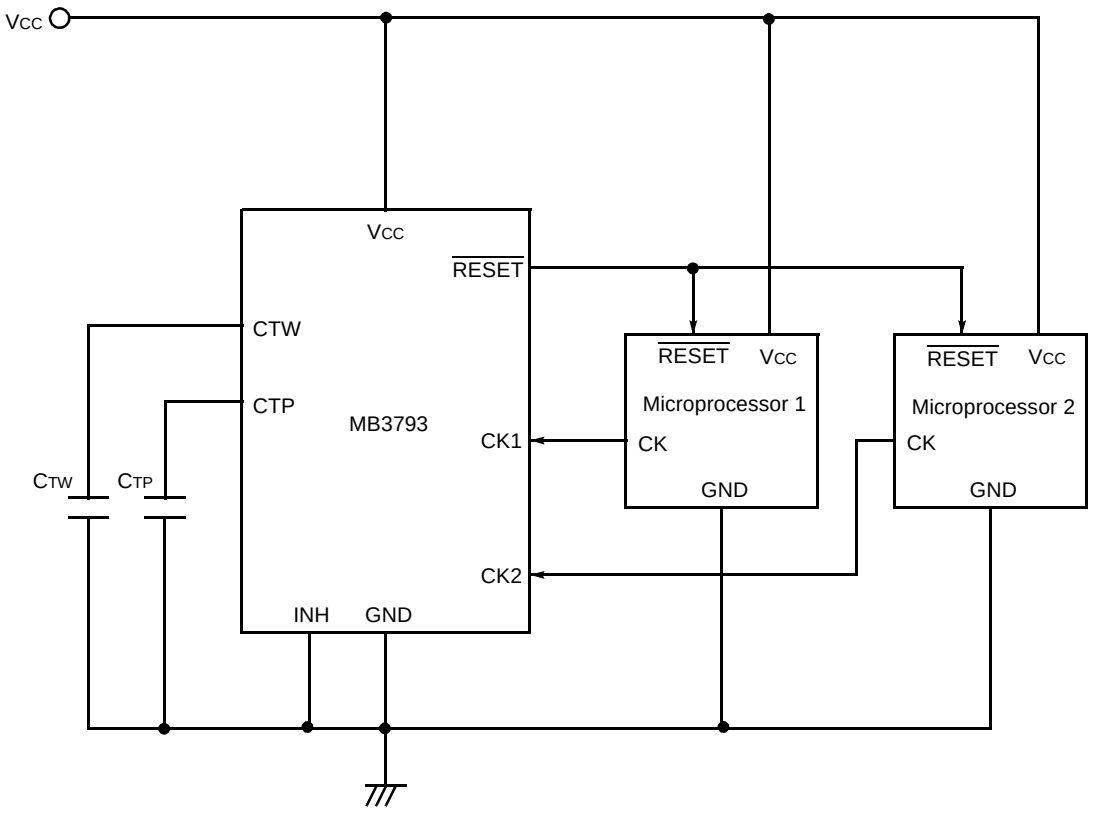
6. Inhibition pin

The inhibition (INH) pin forces the watchdog timer on/off. When this pin is High level, the watchdog timer is stopped.

7. Flip-flop circuit

The flip-flop circuit RSFF1 controls charging and discharging of the power-on reset hold time setting capacity (C_{TP}). The flip-flop circuit RSFF2 switches the charging accelerator for charging C_{TP} during resetting on/off. This circuit only functions during resetting and does not function at power-on reset.

■ STANDARD CONNECTION



Equation of time-setting capacitances (C_{TP} and C_{TW}) and set time

t_{PR} (ms) ≈ A x C_{TP} (µF)

t_{WD} (ms) ≈ B x C_{TW} (µF) + C x C_{TP} (µF)

However, when $\frac{C_{TP}}{C_{TW}}$ ≤ about 10,

t_{WD} (ms) ≈ B x C_{TW} (µF)

t_{WR} (ms) ≈ D x C_{TP} (µF)

Values of A, B, C, and D

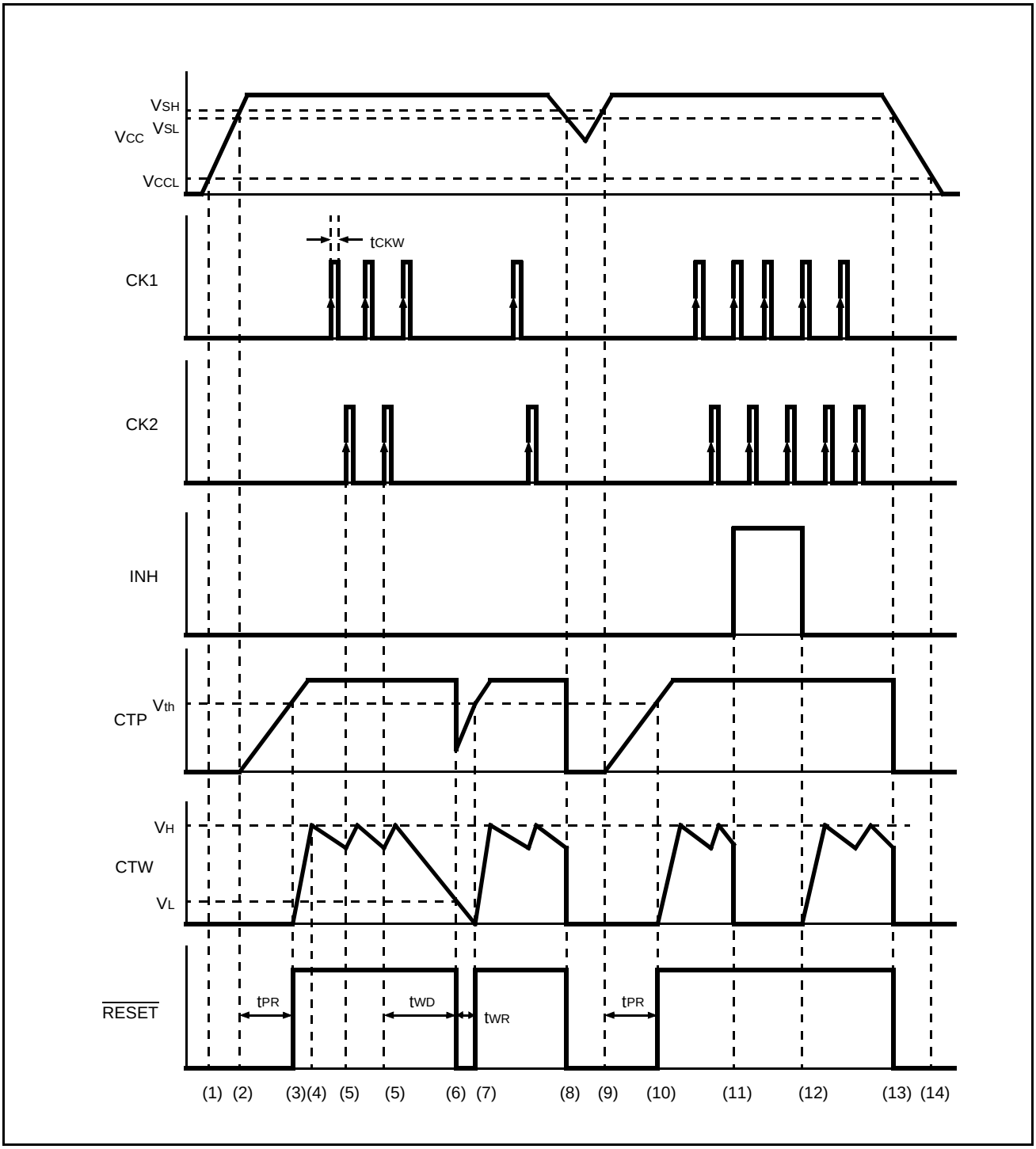
Model No.	A	B	C	D	Remark
MB3793-42	1300	1500	3	100	
MB3793-30	750	1600	4	55	

(Example) When C_{TP} = 0.1 µF and C_{TW} = 0.01 µF,

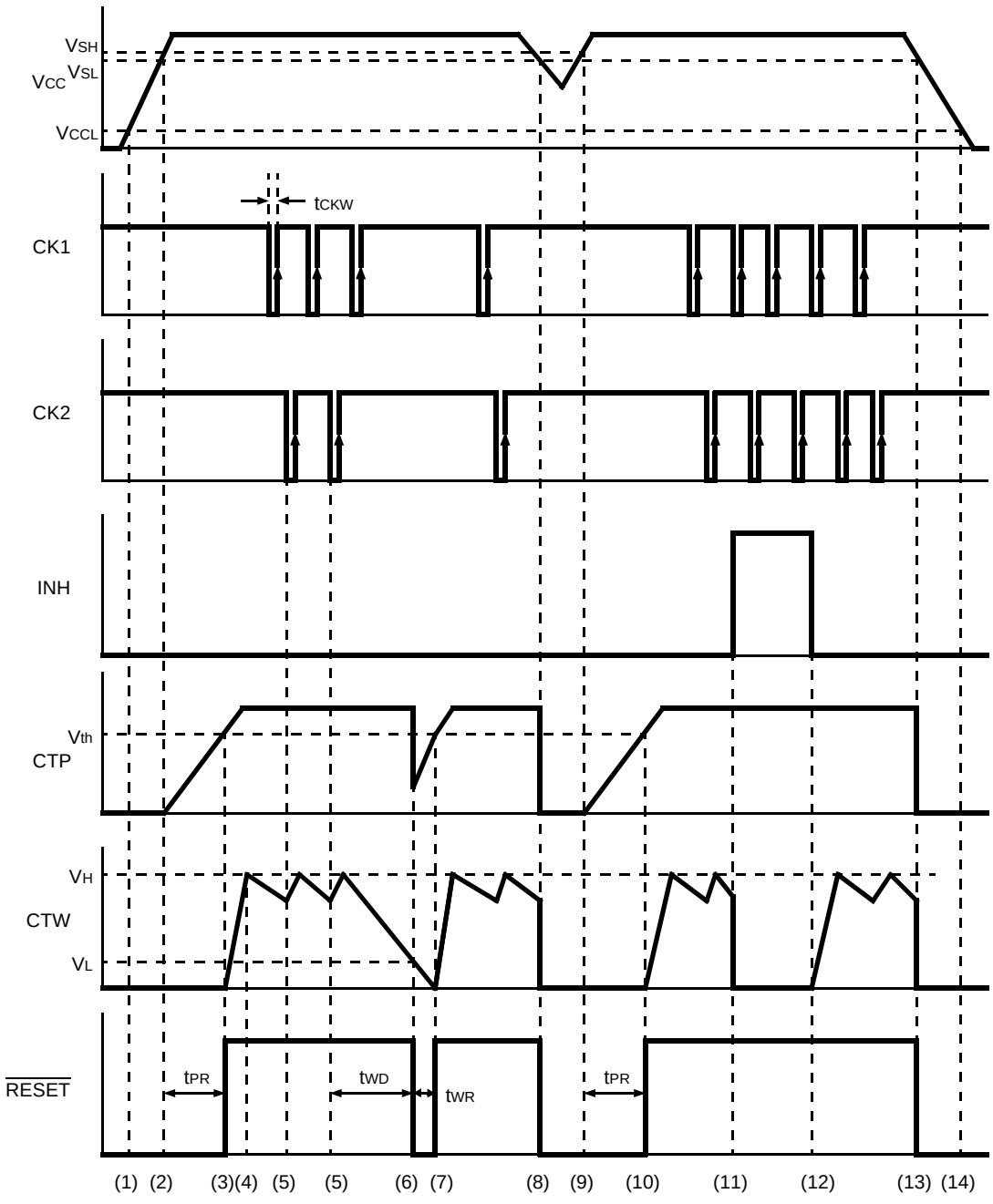
- MB3793-42
  t_{PR} ≈ 130 [ms]
  t_{WD} ≈ 15 [ms]
  t_{WR} ≈ 10 [ms]
- MB3793-30
  t_{PR} ≈ 75 [ms]
  t_{WD} ≈ 16 [ms]
  t_{WR} ≈ 5.5 [ms]

■ TIMING CHART

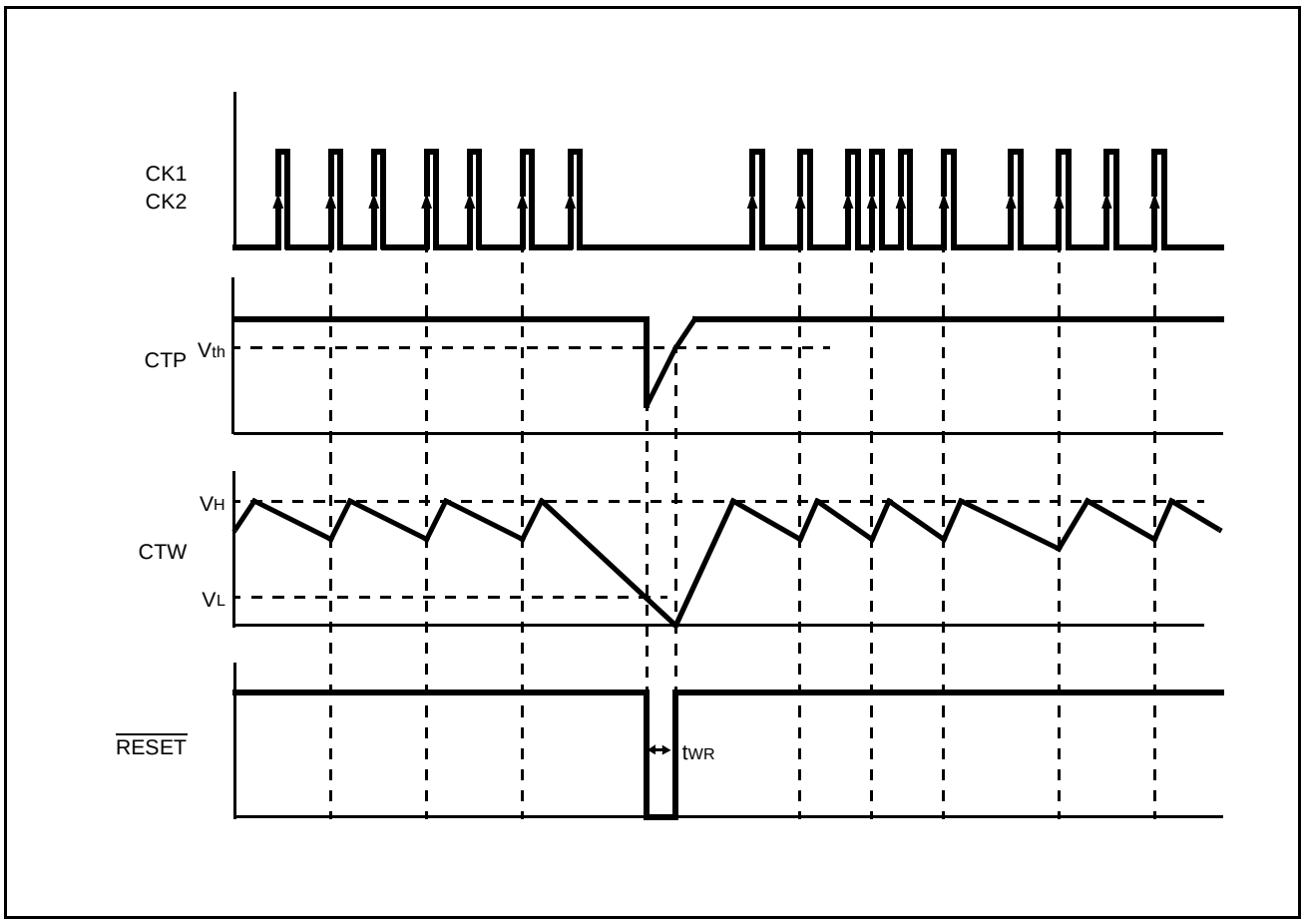
1. Basic operation (Positive clock pulse)



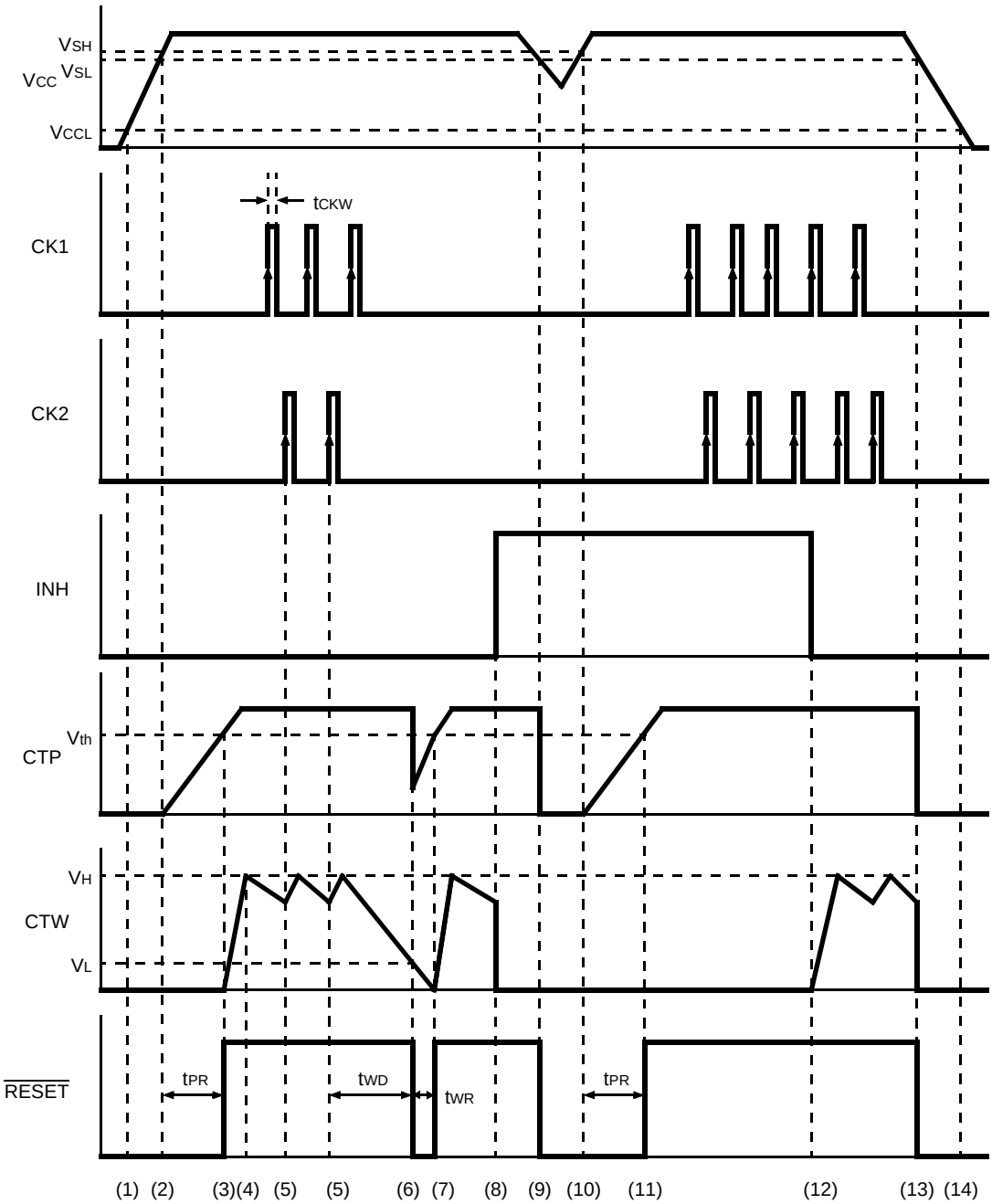
2. Basic operation (Negative clock pulse)



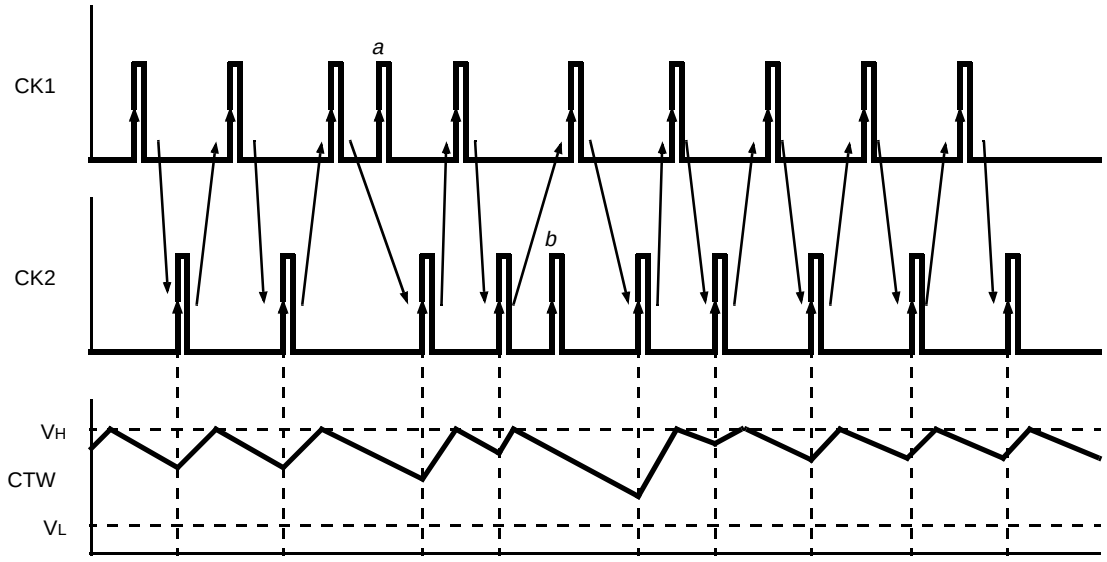
3. Single-clock input monitoring (Positive clock pulse)



4. Inhibition operation (Positive clock pulse)



5. Clock pulse input (Positive clock pulse)



The MB3793 watchdog timer monitors Clock 1 (CK1) and Clock 2 (CK2) pulses alternately. When a CK2 pulse is detected after detecting a CK1 pulse, the monitoring time setting capacity (C_{TW}) switches to charging from discharging.

When two consecutive pulses occur on one side of this alternation before switching, the second pulse is ignored. In the above figure, pulses *a* and *b* are ignored.

■ OPERATION SEQUENCE

The operation sequence is explained by using Timing Chart 1.

The following item numbers correspond to the numbers in Timing Chart 1.

(1) When the power voltage (V_{CC}) reaches about 0.8 V (V_{CCL}), a reset signal is output.

(2) When V_{CC} exceeds the rising-edge detection voltage (V_{SH}), charging of power-on reset hold time setting capacitance (C_{TP}) is started. V_{SH} is about 4.3 V in the MB3793-42 and 3. 07 V in the MB3793-30.

(3) When the voltage at the CTP pin setting the power-on reset hold time exceeds the threshold voltage (V_{th}), resetting is canceled and the voltage at the $\overline{\text{RESET}}$ pin changes to High level to start charging of the watchdog-timer monitoring time setting capacitance (C_{TW}). Vth is about 3.6 V in the MB3793-42 and 2.4 V in the MB3793-30.

The power-on reset hold time (t_{PR}) can be calculated by the following equation.

$$t_{PR}\ (\text{ms}) \approx A \times C_{TP}\ (\mu\text{F})$$

Where, A is about 1300 in the MB3793-42 and 750 in the MB3793-30.

(4) When the voltage at the CTW pin setting the monitoring time reaches High level (V_H), C_{TW} switches to discharging from charging. V_H is about 1.24 V (reference value) in both the MB3793-42 and MB3793-30.

(5) When clock pulses are input to the CK2 pin during C_{TW} discharging after clock pulses are input to the CK1 pin—positive-edge trigger, C_{TW} switches to charging.

(6) If clock pulse input does not occur at either the CK1 or CK2 clock pins during the watchdog-timer monitoring time (t_{WD}), the CTW voltage falls below Low level (V_L), a reset signal is output, and the voltage at the $\overline{\text{RESET}}$ pin changes to Low level. V_L is about 0.24 V in both the MB3793-42 and MB3793-30.

t_{WD} can be calculated from the following equation.

$$t_{WD}\ (\text{ms}) \approx B \times C_{TW}\ (\mu\text{F}) + C \times C_{TP}\ (\mu\text{F})$$

Where, B is about 1500 in the MB3793-42 and 1600 in the MB3793-30. C is about 3 in the MB3793-42 and 4 in the MB3793-30; it is much smaller than B.

Hence, when $\frac{C_{TP}}{C_{TW}} \leq 10$, the calculation can be simplified as follows:

$$t_{WD}\ (\text{ms}) \approx B \times C_{TW}\ (\mu\text{F})$$

(7) When the voltage of the CTP pin exceeds V_{th} again as a result of recharging C_{TP}, resetting is canceled and the watchdog timer restarts monitoring.

The watchdog timer reset time (t_{WR}) can be calculated by the following equation.

t_{WR} (ms) ≈ D x C_{TP} (µF)

Where, D is about 100 in the MB3793-42 and 55 in the MB3793-30.

(8) When V_{CC} falls below the rising-edge detection voltage (V_{SL}), the voltage of the CTP pin falls and a reset signal is output, and the voltage at the $\overline{\text{RESET}}$ pin changes to Low level. V_{SL} is about 4.2 V in the MB3793-42 and 3.0 V in the MB3793-30.

(9) When V_{CC} exceeds V_{SH}, C_{TP} begins charging.

(10) When the voltage of the CTP pin exceeds V_{th}, resetting is canceled and the watchdog timer restarts.

(11) When an inhibition signal is input (INH pin is High level), the watchdog timer is halted forcibly.

In this case, V_{CC} monitoring is continued ((8) - (9)) without the watchdog timer.

The watchdog timer does not function unless this inhibition input is canceled.

(12) When the inhibition input is canceled (INH pin is Low level), the watchdog timer restarts.

(13) When the V_{CC} voltage falls below V_{SL} after power-off, a reset signal is output.

Similar operation is also performed for negative clock-pulse input (Timing Chart 2).

Short-circuit the clock pins CK1 and CK2 to monitor a single clock. The basic operation is the same but the clock pulses are monitored at every other pulse (Timing Chart 3).

■ ABSOLUTE MAXIMUM RATINGS

(Ta = +25°C)

Parameter		Symbol	LImits	Symbo
Power voltage*		V_{CC}	-0.3 to +7	V
Input voltage	CK1	V_{CK1}	-0.3 to +7	V
	CK2	V_{CK2}		
	INH	V_{INH}		
Reset output voltage (direct current)	$\overline{\text{RESET}}$	I_{OL} I_{OH}	-10 to +10	mA
Allowable loss (Ta ≤ +85°C)		P_D	200	mW
Storage temperature		Tstg	-55 to +125	°C

*The power voltage is based on the ground voltage (0 V).

Note: Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Limits			Unit
		Min.	Typical	Max.	
Reset ($\overline{\text{RESET}}$) output current	I_{OL} I_{OH}	-5	-	+5	mA
Power-on reset hold time setting capacity	C_{TP}	0.001	-	10	µF
Watchdog-timer monitoring time setting capacity	C_{TW}	0.001	-	1	µF
Watchdog timer monitoring time	t_{WD}	0.1	-	1500	ms
Operating ambient temperature	Ta	-40	-	+85	°C

Note: These recommended operation conditions guarantee normal logic operation of an LSI circuit. The limits of the AC and DC electrical characteristics are guaranteed within these recommended conditions.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{CC} = +5 V (MB3793-42), V_{CC} = +3.3 V (MB3793-30), Ta = +25°C)

Parameter		Symbol	Test Conditions		Limits			Unit
					Min.	Typical	Max.	
Power current	MB3793-42	I_{CC1}	Watchdog timer operation*		-	27	50	µA
		I_{CC2}	Watchdog timer halt**		-	25	45	
	MB3793-30	I_{CC1}	Watchdog timer operation*		-	25	45	µA
		I_{CC2}	Watchdog timer halt**		-	24	45	
Detection voltage	MB3793-42	V_{SL}	V_{CC} falling	Ta = +25°C	4.10	4.20	4.30	V
				Ta = -40 to +85°C	4.05	4.20	4.35	
		V_{SH}	V_{CC} rising	Ta = +25°C	4.20	4.30	4.40	V
				Ta = -40 to +85°C	4.15	4.30	4.45	
	MB3793-30	V_{SL}	V_{CC} falling	Ta = +25°C	2.90	3.00	3.10	V
				Ta = -40 to +85°C	2.85	3.00	3.15	
		V_{SH}	V_{CC} rising	Ta = +25°C	2.97	3.07	3.17	V
				Ta = -40 to +85°C	2.92	3.07	3.22	
Detection voltage hysteresis difference	MB3793-42	V_{SHYS}	V_{SH} - V_{SL}		50	100	150	mV
	MB3793-30				30	70	110	mV
Clock-input threshold voltage		V_{thCH}	-		(1.4)	1.9	(2.5)	V
		V_{thCL}	-		(0.8)	1.3	(1.8)	V
Clock-input hysteresis		V_{CHYS}	-		(0.4)	0.6	(0.8)	V
Inhibition-input threshold voltage		V_{thIN}	-		0.8	1.5	2.0	V
Input current	CK1 CK2 INH	I_{IH}	V_{CK} = V_{CC}		-	0	1.0	µA
		I_{IL}	V_{CK} = 0 V		-1.0	0	-	µA
Reset output voltage	MB3793-42	V_{OH}	$I_{\overline{RESET}}$ = -5 mA		4.5	4.75	-	V
		V_{OL}	$I_{\overline{RESET}}$ = +5 mA		-	0.12	0.4	V
	MB3793-30	V_{OH}	$I_{\overline{RESET}}$ = -3 mA		2.8	3.10	-	V
		V_{OL}	$I_{\overline{RESET}}$ = +3 mA		-	0.12	0.4	V
Reset-output minimum power voltage		V_{CCL}	$I_{\overline{RESET}}$ = +50 µA		-	0.8	1.2	V

*At clock input pins CK1 and CK2, the pulse input frequency is 1 kHz and the pulse amplitude is 0 V to V_{CC}.
**Inhibition input is at High level.

2. AC Characteristics

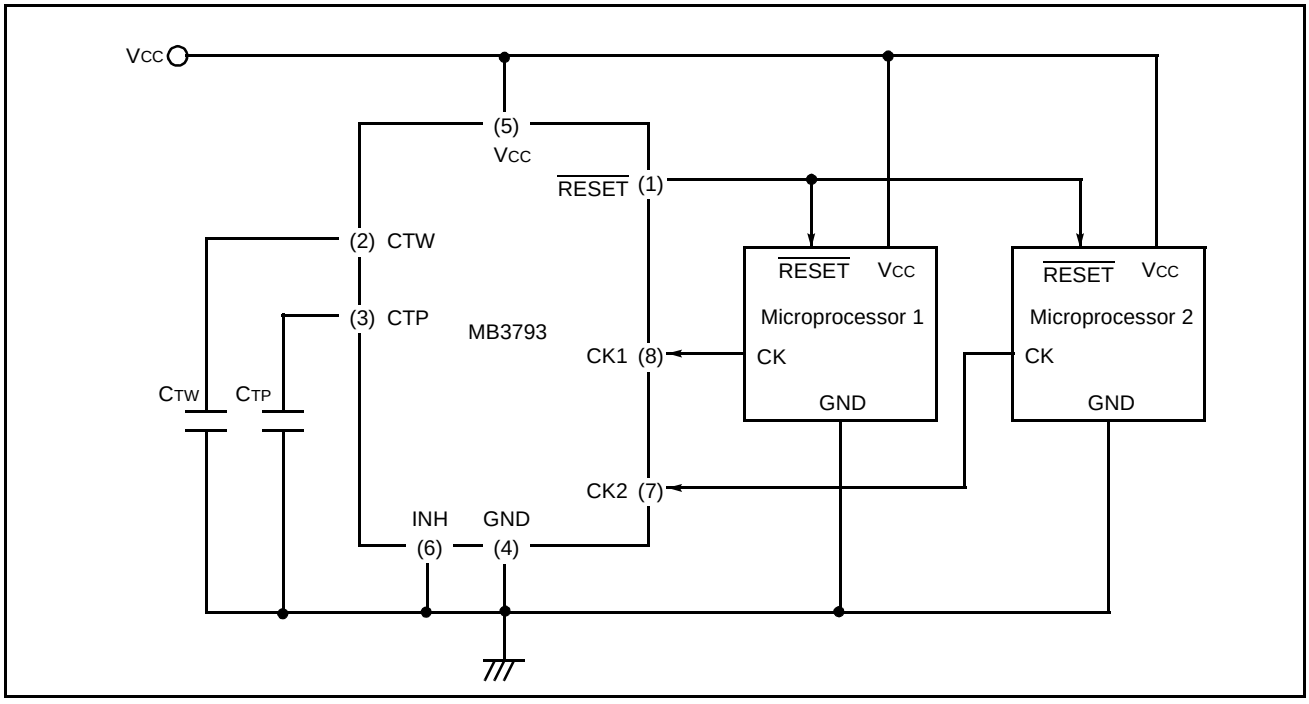
(V_{CC} = +5 V (MB3793-42), V_{CC} = +3.3 V (MB3793-30), Ta = +25°C)

Parameter		Symbol	Test Conditions	Limits			Unit
				Min.	Typical	Max.	
Power-on reset hold time	MB3793-42	t_{PR}	C_{TP} = 0.1 µF	80	130	180	ms
	MB3793-30			30	75	120	ms
Watchdog timer monitoring time	MB3793-42	t_{WD}	C_{TW} = 0.01 µF	7.5	15	22.5	ms
	MB3793-30		C_{TP} = 0.1 µF	8	16	24	ms
Watchdog timer reset time	MB3793-42	t_{WR}	C_{TP} = 0.1 µF	5	10	15	ms
	MB3793-42			2.0	5.5	9	ms
Clock (CK1, CK2) input pulse duration		t_{CKW}	-	500	-	-	ns
Reset ($\overline{RESET}$) output transition time*	Rising	t_{TLH}	C_L = 50pF	-	-	500	ns
	Falling	t_{THL}	C_L = 50pF	-	-	500	ns

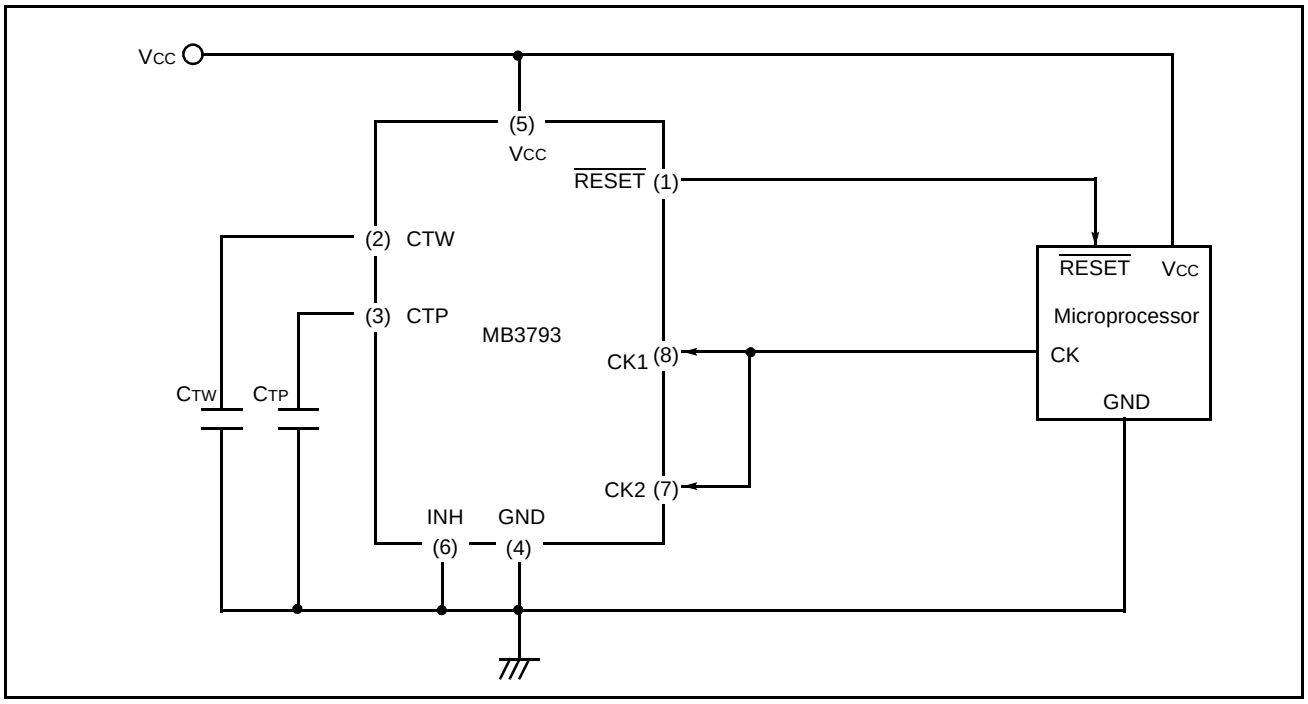
*The voltage range is 10% to 90% at testing the reset output transition time.

■ WATCHDOG TIMER USE EXAMPLE

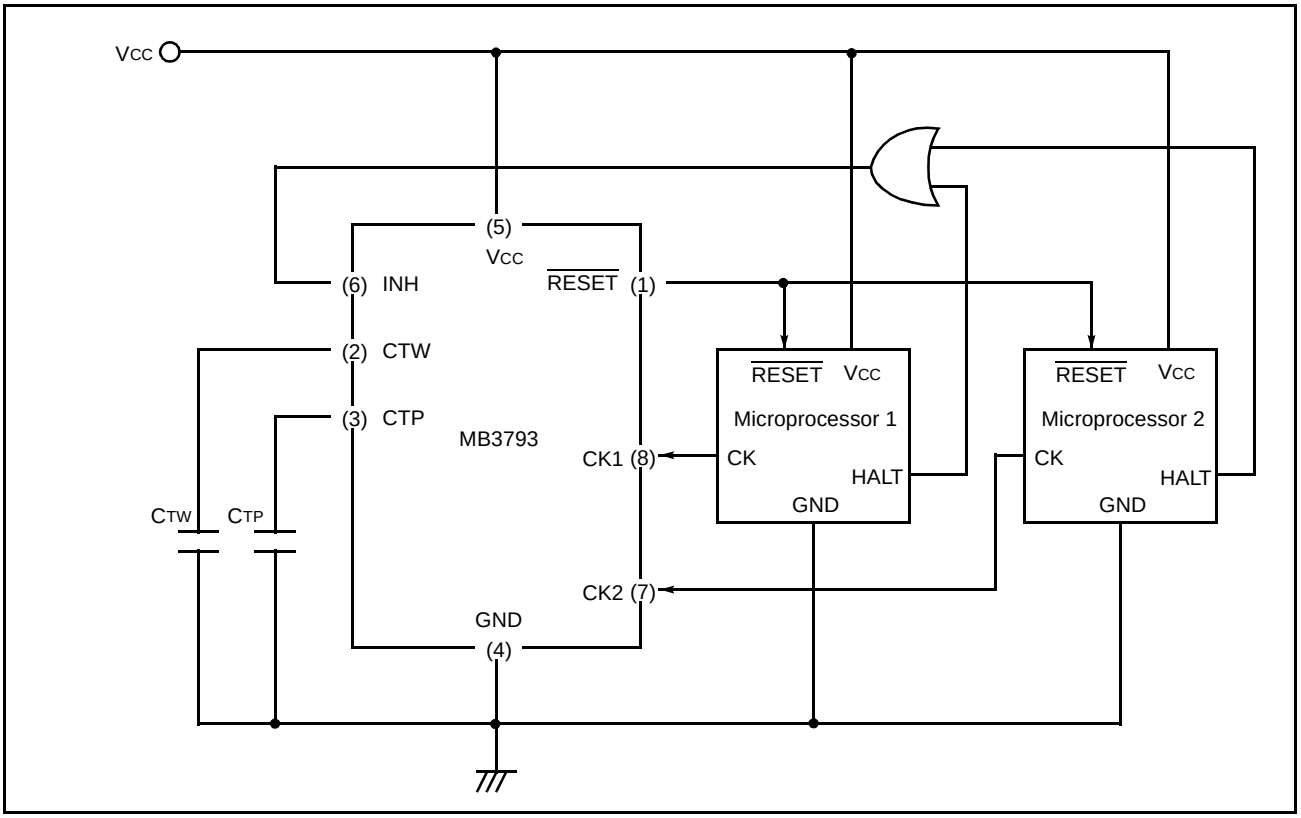
1. Monitoring Two Clocks



2. Monitoring Single Clock

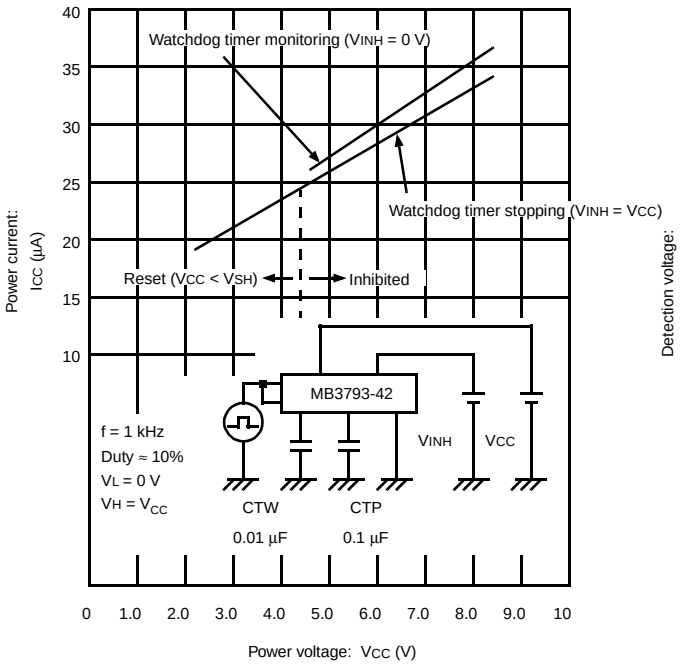


3. Watchdog Timer Stopping

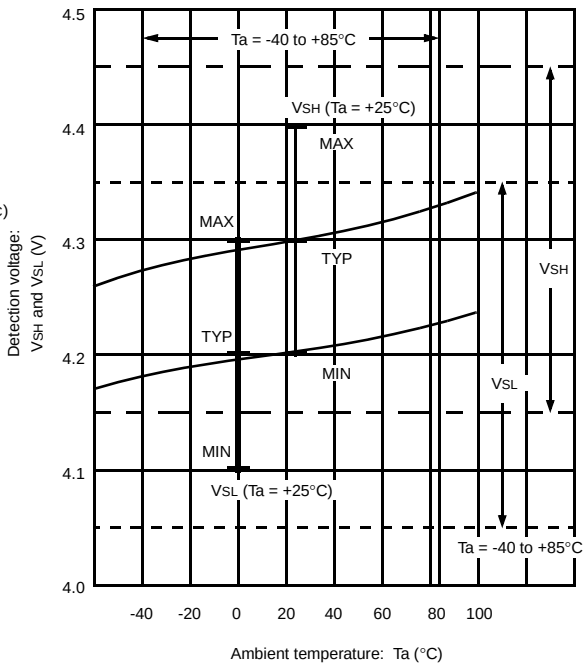


■ REFERENCE CHARACTERISTIC CURVES (FOR MB3793-42)

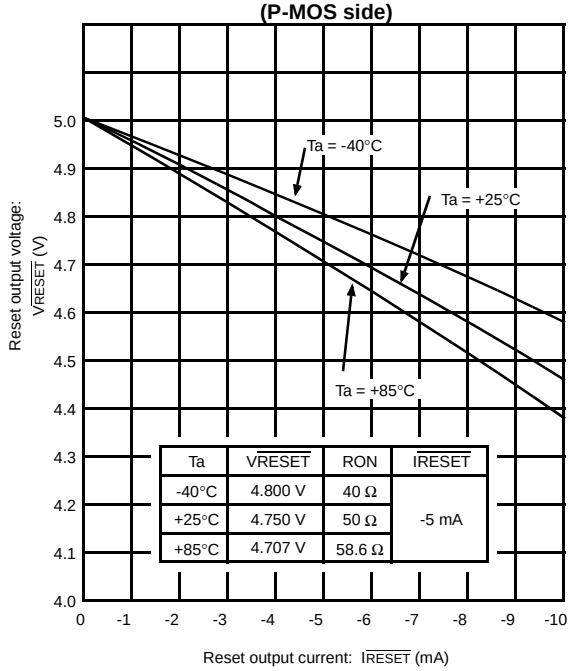
Power Current - Power Voltage



Detection Voltage - Ambient Temperature

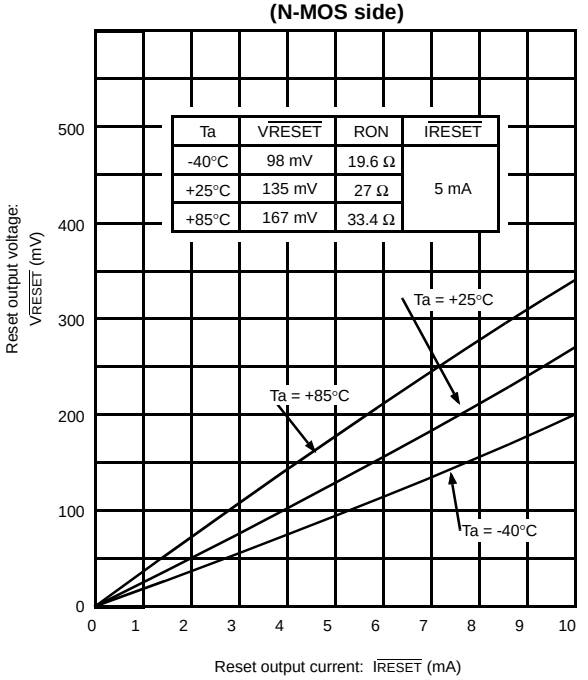


Reset Output Voltage - Reset Output Current (P-MOS side)



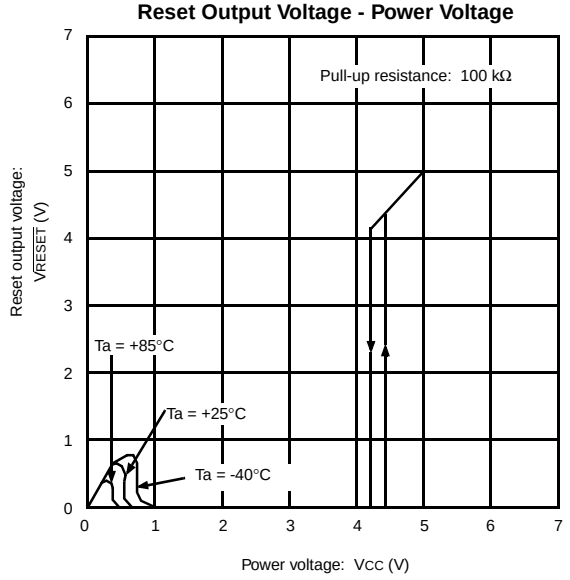
Ta	VRESET	RON	IRESET
-40°C	4.800 V	40 Ω	-5 mA
+25°C	4.750 V	50 Ω	
+85°C	4.707 V	58.6 Ω	

Reset Output Voltage - Reset Output Current (N-MOS side)

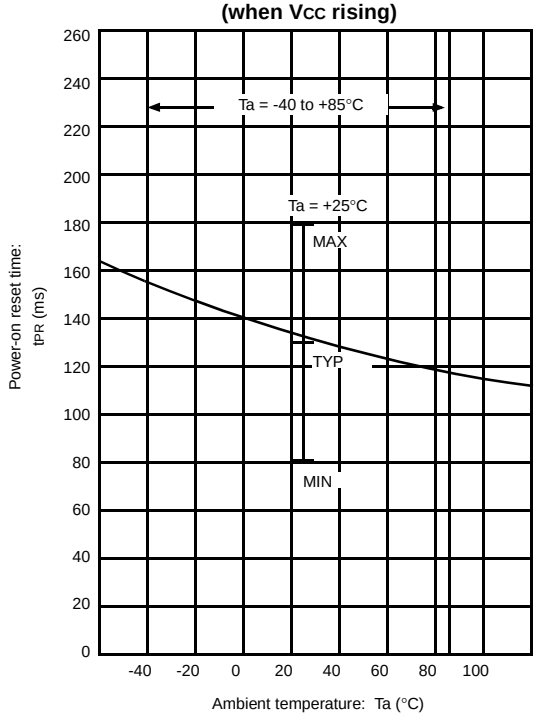


Ta	VRESET	RON	IRESET
-40°C	98 mV	19.6 Ω	5 mA
+25°C	135 mV	27 Ω	
+85°C	167 mV	33.4 Ω	

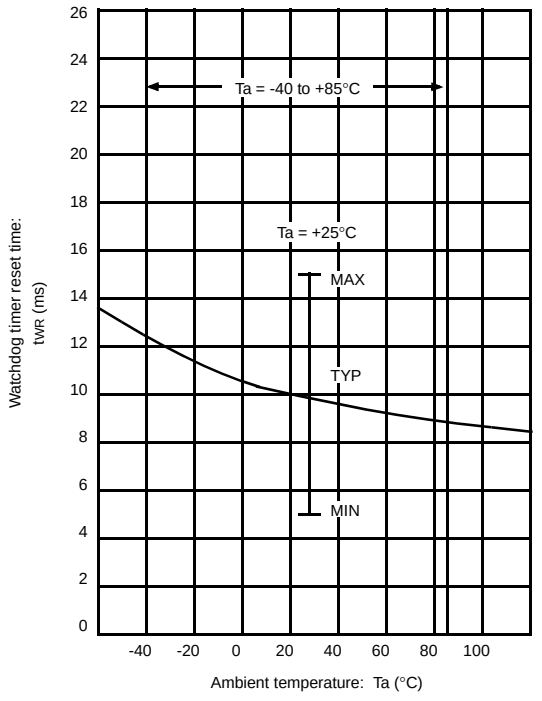
Reset Output Voltage - Power Voltage



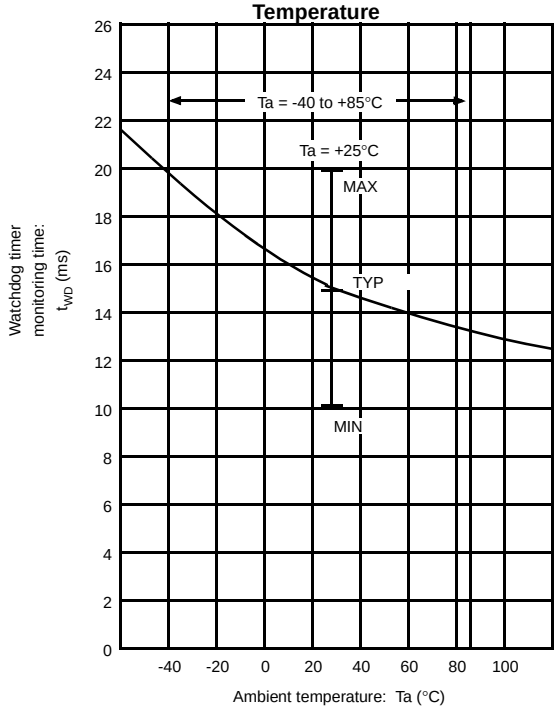
Reset-on Reset Time - Ambient Temperature (when VCC rising)



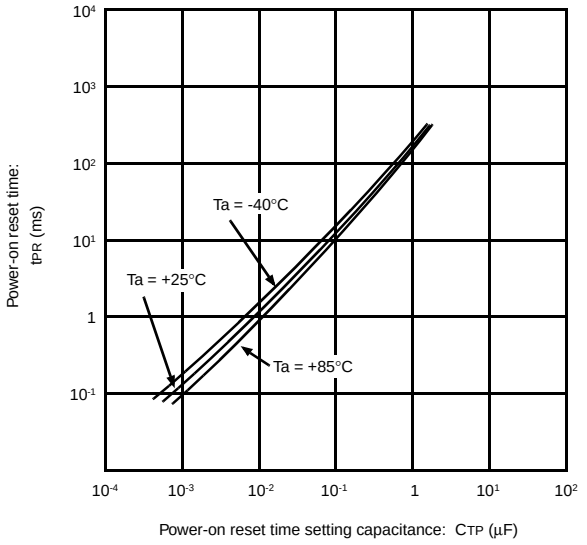
Watchdog Timer Reset Time - Ambient Temperature (when monitoring)



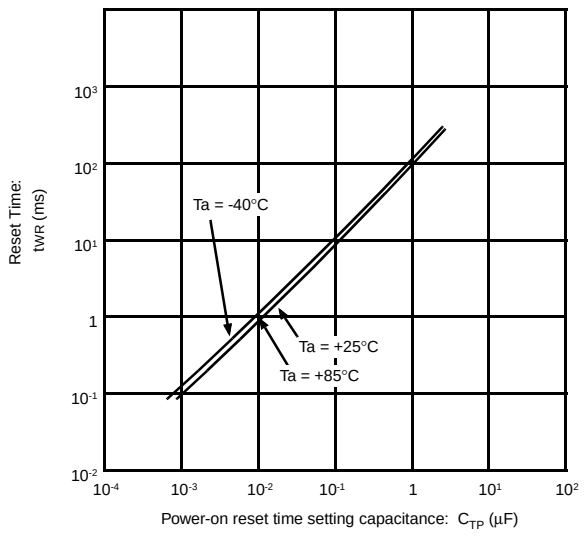
Watchdog Timer Monitoring Time - Ambient Temperature



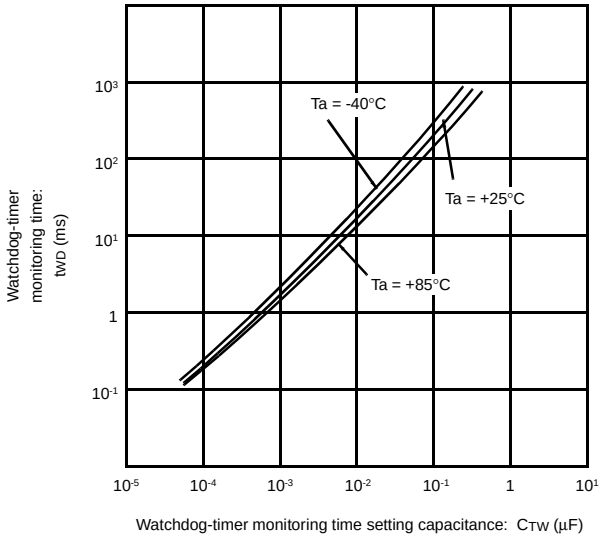
Power-on Reset Time - C_{TP} Capacitance



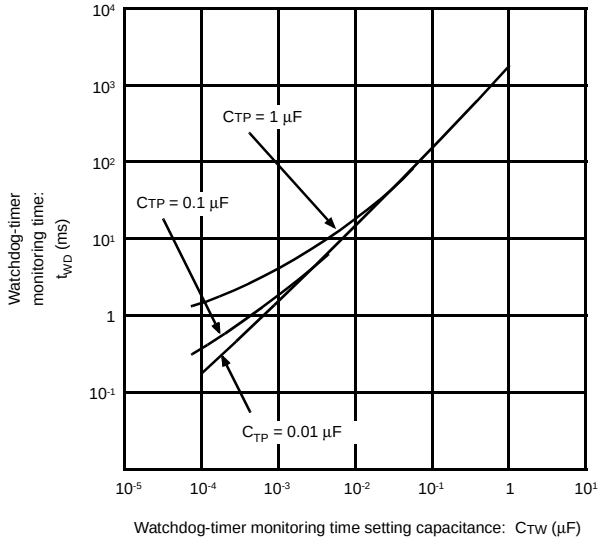
Reset Time - C_{TP} Capacitance



Watchdog-Timer Monitoring Time - C_{TW} Capacitance (under Ta condition)

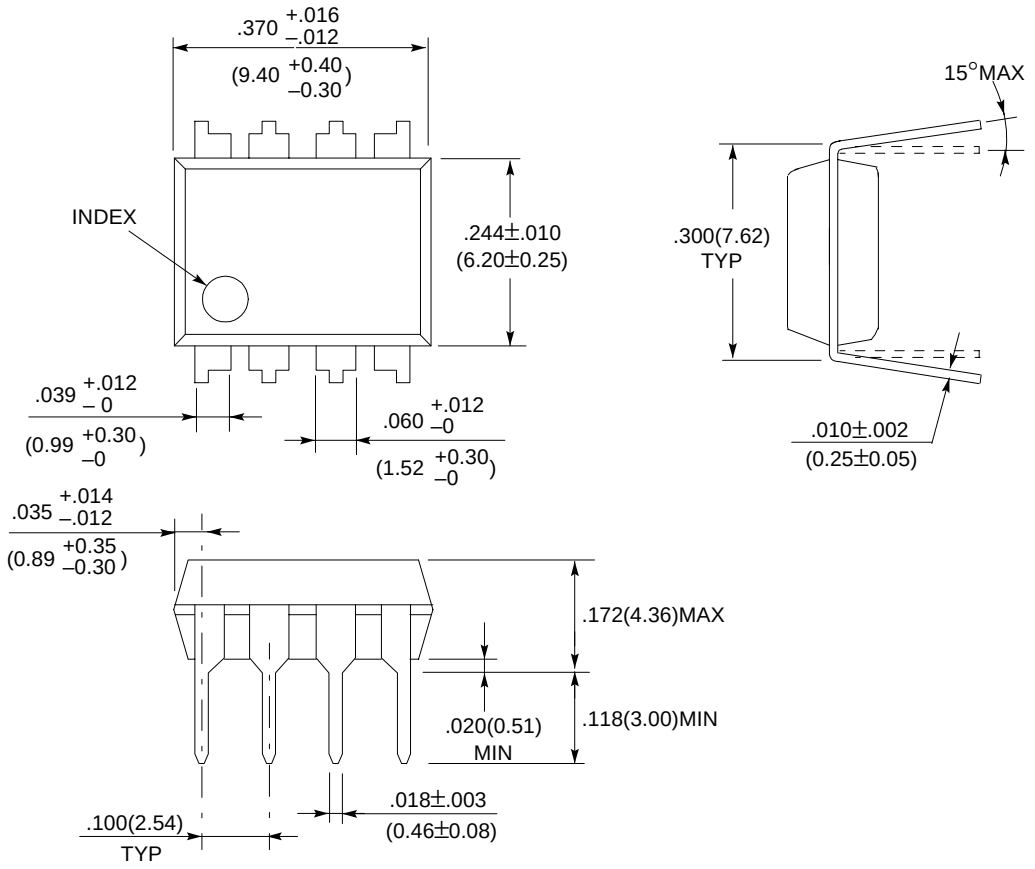


Watchdog-Timer Monitoring Time - C_{TW} Capacitance



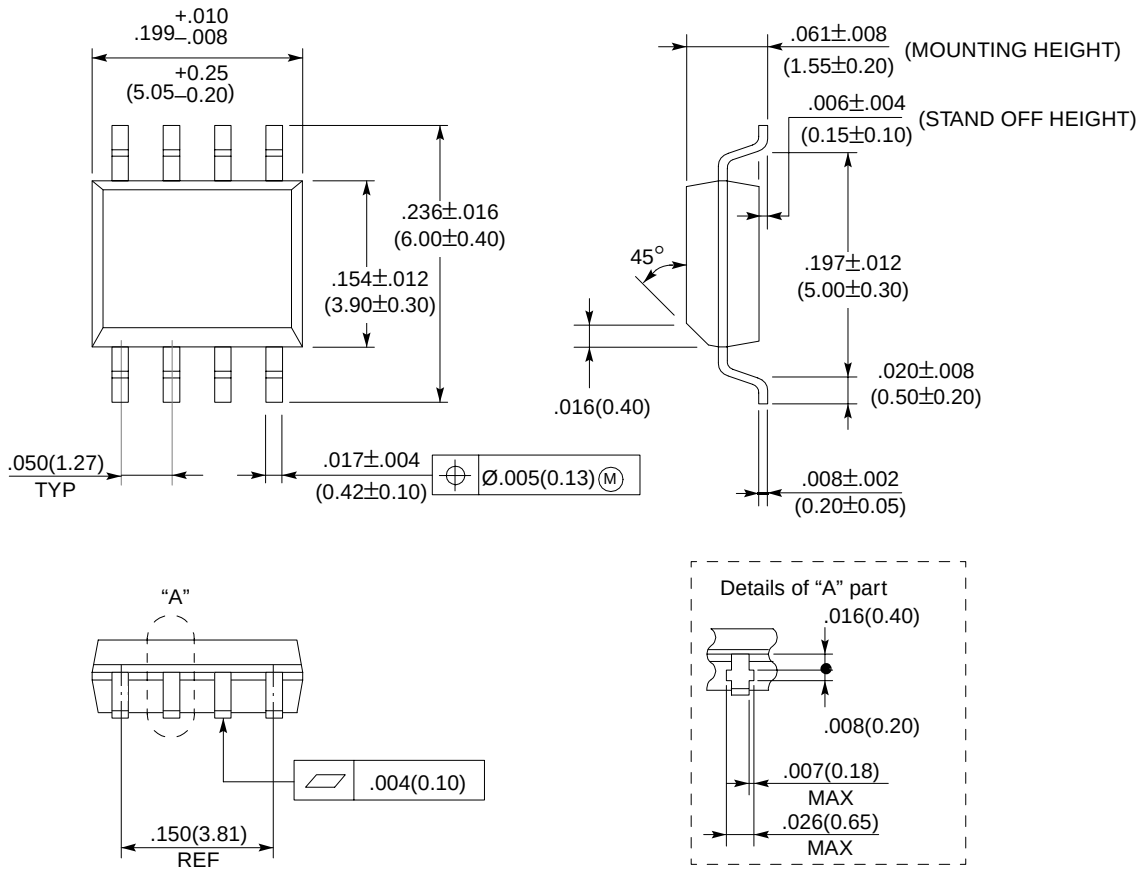
■ PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE



Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-8P-M02)



Dimensions in
inches (millimeters)

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