FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27216-2E

*ASSP For Power Supply Applications*

**BIPOLAR**

# Switching Regulator Controller

# MB3817

## ■ DESCRIPTION

The MB3817 is a pulse width modulator (PWM) type switching regulator controller IC designed for low-voltage and high-speed operation. This can be used in applications as down-conversion or down/up-conversion (Zeta method).

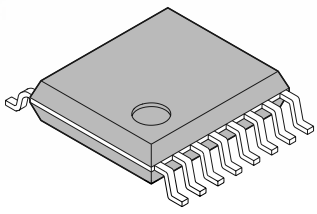
With fewer external components and faster operating speed, the MB3817 enables reduction in power supply unit size, making it ideal for use with internal power supplies in compact, high-performance portable devices.

## ■ FEATURES

- Wide range of operating power supply voltages: 2.5 V to 18 V
- Built-in high-precision reference voltage generator: 1.5 V ± 2%
- High speed operation is possible: Max. 500 kHz
- Wide input voltage range of error amplifier: 0 to $V_{CC}$ – 0.9 V
- Built-in soft start function
- Built-in timer/latch-actuated short-circuiting protection circuit
- Totem-pole type output with adjustable on/off current (for PNP transistors)
- Built-in standby function
- Small package: SSOP-16P (FPT-16P-M05)

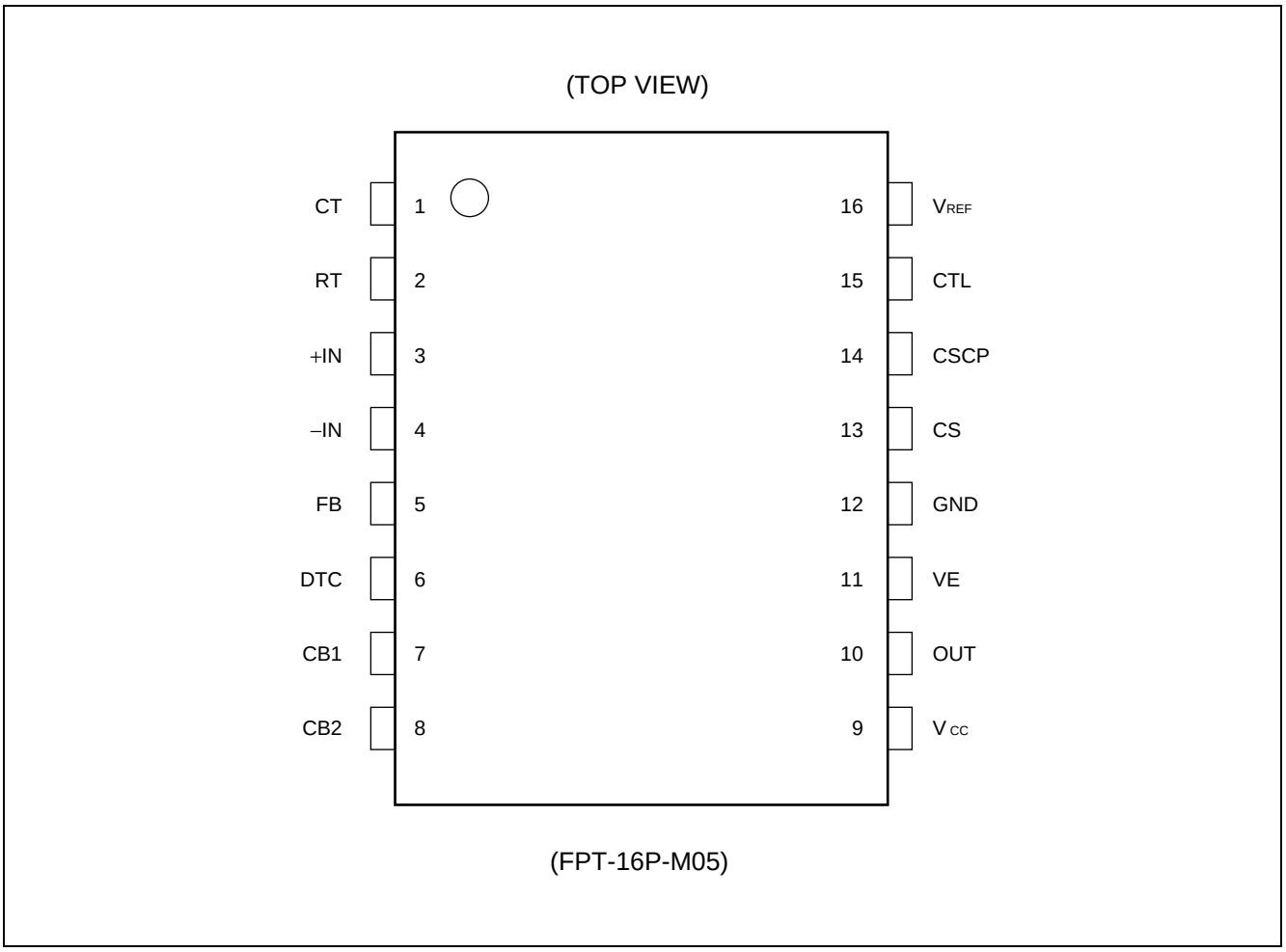
## ■ PACKAGE

16-pin Plastic SSOP



(FPT-16P-M05)

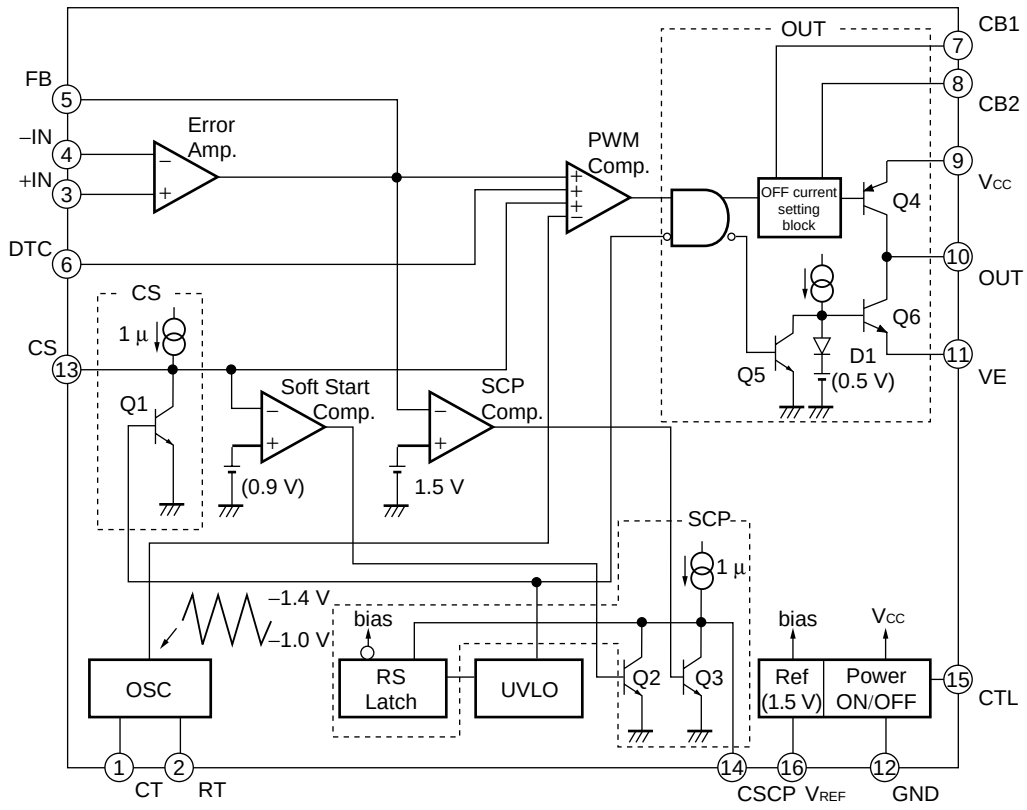
## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTION

| Pin no. | Pin name | I/O | Descriptions |
|---|---|---|---|
| 1 | CT | — | This pin connects to a capacitor for setting the triangular-wave frequency. |
| 2 | RT | — | This pin connects to a resistor for setting the triangular-wave frequency. |
| 3 | +IN | I | Error amplifier non-inverted input pin |
| 4 | –IN | I | Error amplifier inverted input pin |
| 5 | FB | O | Error amplifier output pin |
| 6 | DTC | I | Dead time control pin |
| 7 | CB1 | — | Boot capacitor connection pin |
| 8 | CB2 | — | Boot capacitor connection pin |
| 9 | $V_{CC}$ | — | Power supply pin |
| 10 | OUT | O | Totem-pole type output pin |
| 11 | VE | — | Output current setting pin |
| 12 | GND | — | Ground pin |
| 13 | CS | — | Soft start setting capacitor connection pin |
| 14 | CSCP | — | Short detection setting capacitor connection pin |
| 15 | CTL | I | Power supply control pin<br>When this pin is High, IC is inactive state<br>When this pin is Low, IC is standby state |
| 16 | $V_{REF}$ | O | Reference voltage output pin |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Power supply voltage | $V_{CC}$ | — | — | 20 | V |
| Power dissipation | $P_D$ | Ta ≦ +25°C | — | 440* | mW |
| Storage temperature | Tstg | — | –55 | +125 | °C |

* : The package is mounted on the epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Power supply voltage | $V_{CC}$ | — | 2.5 | 6.0 | 18 | V |
| Reference voltage output current | $I_{OR}$ | — | –1 | — | 0 | mA |
| Error amp. input voltage | $V_{IN}$ | — | 0 | — | $V_{CC}$ – 0.9 | V |
| Control input voltage | $V_{CTL}$ | — | 0 | — | 18 | V |
| Output current | $I_O$ | — | 3 | — | 30 | mA |
| Timing capacitance | $C_T$ | — | 150 | — | 1500 | pF |
| Timing resistance | $R_T$ | — | 5.1 | — | 100 | kΩ |
| Oscillation frequency | $f_{OSC}$ | — | 10 | 200 | 500 | kHz |
| Soft start capacitance | $C_S$ | — | — | 0.1 | 1.0 | µF |
| Short detection capacitance | $C_{SCP}$ | — | — | 0.1 | 1.0 | µF |
| Boot capacitance | $C_B$ | — | — | — | 0.1 | µF |
| Operating temperature | Ta | — | –40 | +25 | +85 | °C |

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 6 V, Ta = +25°C)

| Parameter | | Symbol | Pin no. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| Reference section (Ref) | Output voltage | $V_{REF}$ | 16 | — | 1.47 | 1.50 | 1.53 | V |
| | Output temperature stability | $\Delta V_{REF}/V_{REF}$ | 16 | Ta = –40°C to +85°C | — | 0.5* | — | % |
| | Input stability | Line | 16 | $V_{CC}$ = 2.5 V to 18 V | — | 2 | 10 | mV |
| | Load stability | Load | 16 | $I_{OR}$ = 0 mA to –1 mA | — | 2 | 10 | mV |
| | Short circuit output current | $I_{OS}$ | 16 | $V_{REF}$ = 1 V | –10 | –5 | –2 | mA |
| Under voltage lockout protection section (UVLO) | Threshold voltage | $V_{TH}$ | 13 | $V_{CC}$ = ↑ | — | 2.0 | 2.3 | V |
| | | $V_{TL}$ | 13 | $V_{CC}$ = ↓ | 1.5 | 1.8 | — | V |
| | Hysteresis width | $V_H$ | 13 | — | 0.1 | 0.2 | — | V |
| | Reset voltage | $V_R$ | 13 | — | 0.6 | 1.0 | — | V |
| Soft start section (CS) | Threshold voltage | $V_{T0}$ | 10 | Duty cycle = 0 % | 0.9 | 1.0 | — | V |
| | | $V_{T100}$ | 10 | Duty cycle = 100 % | — | 1.4 | 1.5 | V |
| | Input standby voltage | $V_{STB}$ | 13 | — | — | 50 | 100 | mV |
| | Charge current | $I_{CHG}$ | 13 | — | –1.4 | –1.0 | –0.6 | µA |
| Short circuit detection section (SCP) | Threshold voltage | $V_{TH}$ | 14 | — | 0.60 | 0.65 | 0.70 | V |
| | Input standby voltage | $V_{STB}$ | 14 | — | — | 50 | 100 | mV |
| | Input latch voltage | $V_I$ | 14 | — | — | 50 | 100 | mV |
| | Input source current | $I_I$ | 14 | — | –1.4 | –1.0 | –0.6 | µA |
| Triangular waveform oscillator section (OSC) | Oscillator frequency | $f_{OSC}$ | 10 | $C_T$ = 330 pF<br>$R_T$ = 6.2 kΩ | 450 | 500 | 550 | kHz |
| | Frequency voltage stability | $\Delta f/f_{dv}$ | 10 | $V_{CC}$ = 3.6 V to 16 V | — | 1 | 10 | % |
| | Frequency temperature stability | $\Delta f/f_{dt}$ | 10 | Ta = –40°C to +85°C | — | 1* | — | % |

* : Standard design value.

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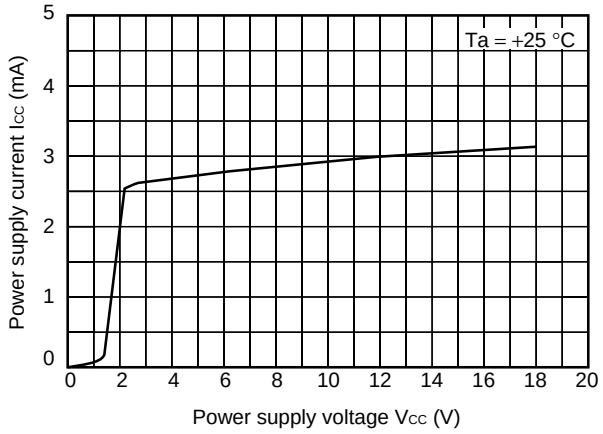
($V_{CC}$ = 6 V, Ta = +25°C)

| Parameter | | Symbol | Pin no. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| Error amp. section (Error Amp.) | Input offset voltage | $V_{IO}$ | 3, 4 | $V_{FB}$ = 1.2 V | — | — | 10 | mV |
| | Input offset current | $I_{IO}$ | 3, 4 | $V_{FB}$ = 1.2 V | — | — | 100 | nA |
| | Input bias current | $I_I$ | 3, 4 | $V_{FB}$ = 1.2 V | –200 | –100 | — | nA |
| | Common mode input voltage range | $V_{CM}$ | 3, 4 | — | 0 | — | $V_{CC}$ – 0.9 | V |
| | Common mode rejection ratio | CMRR | 5 | DC | 60 | 100 | — | dB |
| | Voltage gain | $A_V$ | 5 | DC | 60 | 100 | — | dB |
| | Frequency bandwidth | BW | 5 | $A_V$ = 0 dB | — | 800* | — | kHz |
| | Maximum output voltage width | $V_{OM}^+$ | 5 | — | 1.8 | 2.0 | — | V |
| | | $V_{OM}^-$ | 5 | — | — | 50 | 500 | mV |
| | Output sink current | $I_O^+$ | 5 | $V_{FB}$ = 1.2 V | 60 | 120 | — | µA |
| | Output source current | $I_O^-$ | 5 | $V_{FB}$ = 1.2 V | — | –2.0 | –0.6 | mA |
| Dead time control section (DTC) | Threshold voltage | $V_{T0}$ | 10 | Duty cycle = 0 % | 0.9 | 1.0 | — | V |
| | | $V_{T100}$ | 10 | Duty cycle = 100 % | — | 1.4 | 1.5 | V |
| | ON duty cycle | Dtr | 10 | $V_{DTC} = V_{REF} \times 0.88$<br>$C_T$ = 330 pF,<br>$R_T$ = 6.2 kΩ | 70 | 80 | 90 | % |
| | Input current | $I_{DTC}$ | 6 | $V_{DTC}$ = 0 V | –500 | –250 | — | nA |
| PWM comparator section (PWM Comp.) | Threshold voltage | $V_{T0}$ | 10 | Duty cycle = 0 % | 0.9 | 1.0 | — | V |
| | | $V_{T100}$ | 10 | Duty cycle = 100 % | — | 1.4 | 1.5 | V |
| | Input sink current | $I_I^+$ | 5 | — | 60 | 120 | — | µA |
| | Input source current | $I_I^-$ | 5 | — | — | –2.0 | –0.6 | mA |
| Output section (OUT) | Output sink current | $I_O^+$ | 10 | $R_E$ = 15 kΩ | 18 | 30 | 42 | mA |
| | Output source current | $I_O^-$ | 10 | Duty ≦ 5 % | — | –100 | –50 | mA |
| | Standby leakage current | $I_{LO}$ | 10 | $V_{CC}$ = 18 V,<br>$V_O$ = 18 V | — | — | 10 | µA |
| Control section (CTL) | Input on condition | $V_{ON}$ | 11 | — | 2.1 | — | 18 | V |
| | Input off condition | $V_{OFF}$ | 11 | — | 0 | — | 0.7 | V |
| Input current | | $I_I$ | 15 | $V_{CTL}$ = 5 V | — | 100 | 200 | µA |
| Standby current | | $I_{CCS}$ | 9 | $V_{CTL}$ = 0 V | — | — | 10 | µA |
| Power supply current | | $I_{CC}$ | 9 | Output “H” | — | 2.7 | 4.0 | mA |

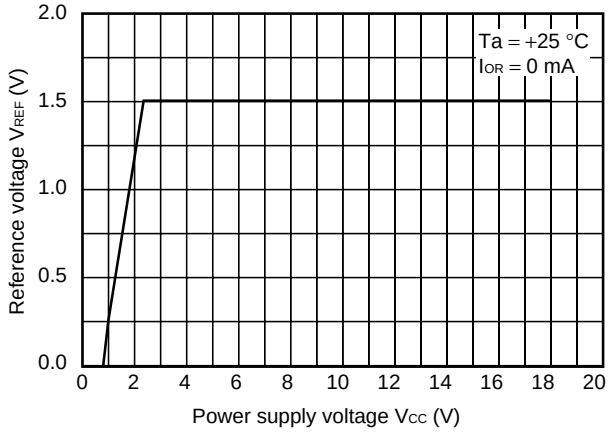
* : Standard design value.

## ■ TYPICAL CHARACTERISTICS

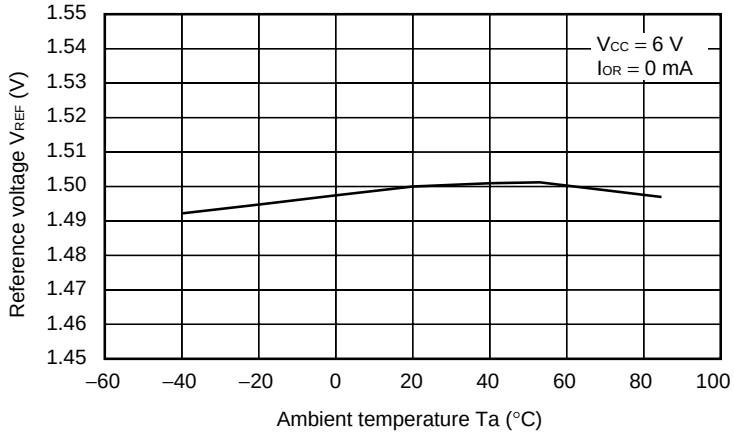
Power supply current vs. power supply voltage



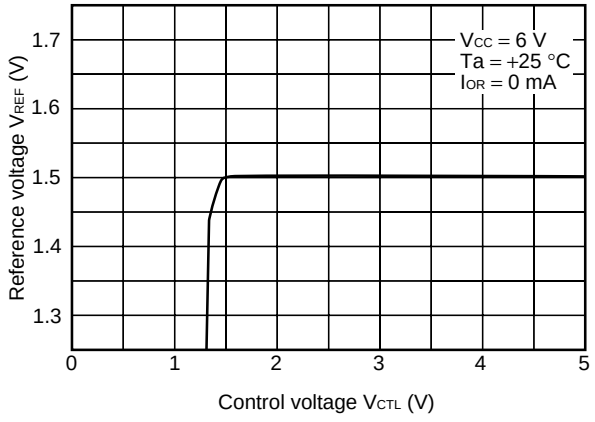

Reference voltage vs. power supply voltage



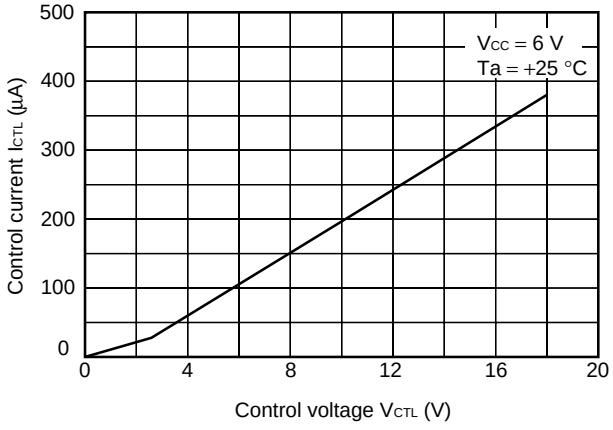

Reference voltage vs. ambient temperature




Reference voltage vs. control voltage




Control current vs. control voltage

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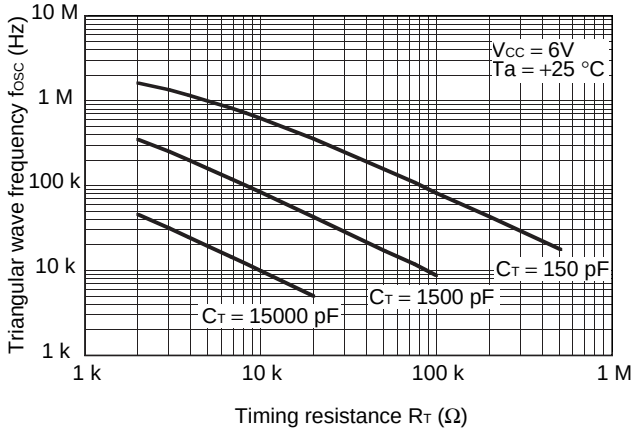
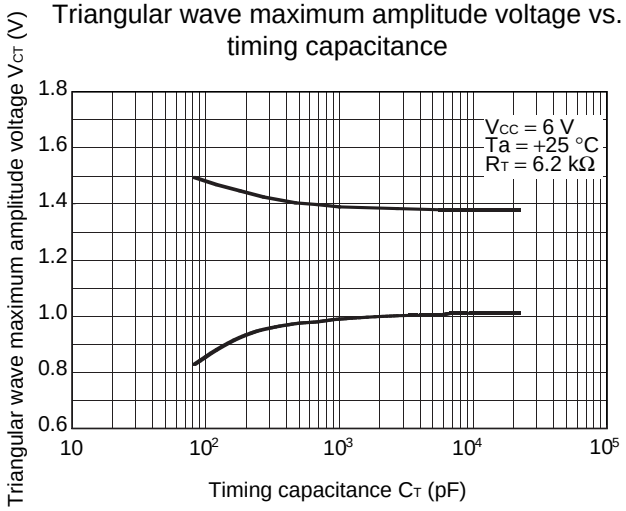
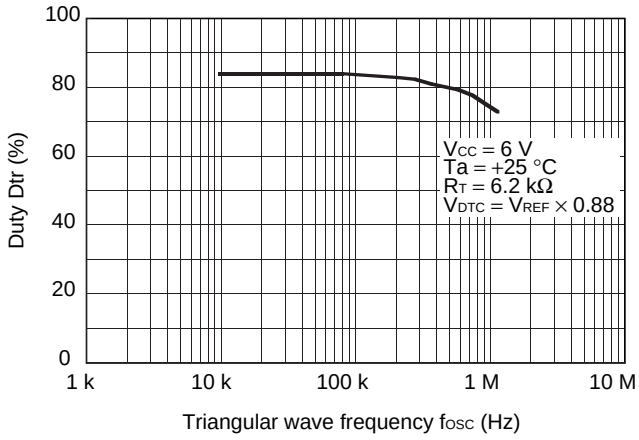
Triangular wave frequency vs. timing resistance



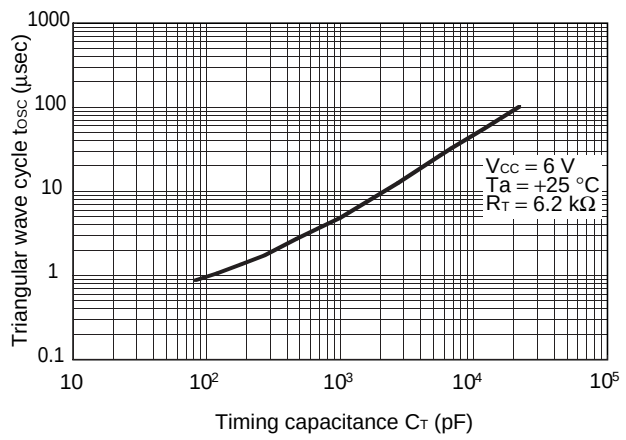

Triangular wave maximum amplitude voltage vs. timing capacitance



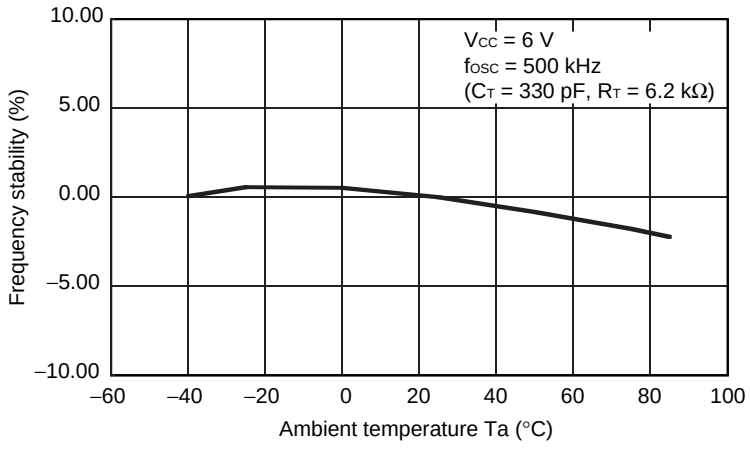

Duty vs. triangular wave frequency




Triangular wave cycle vs. timing capacitance




Frequency stability vs. ambient temperature

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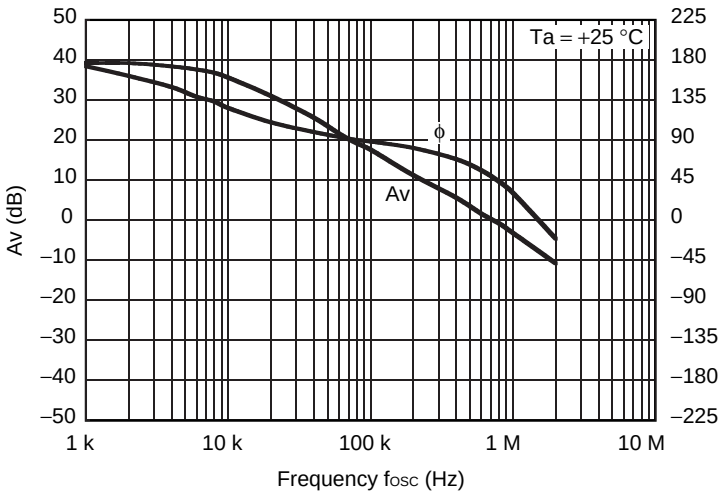
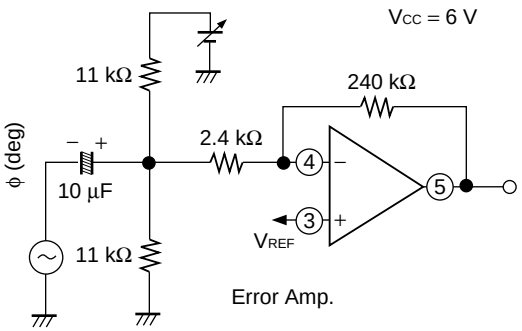
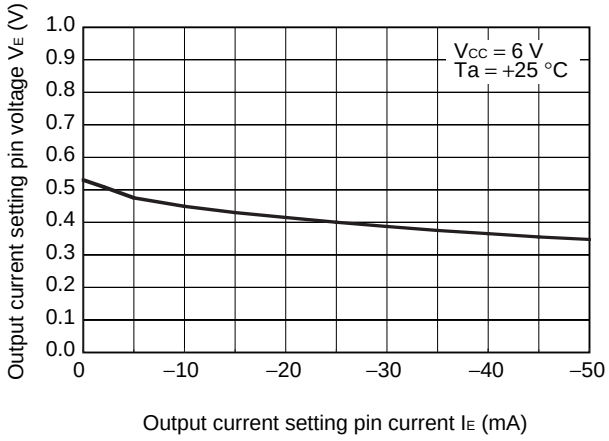
Error amp. frequency



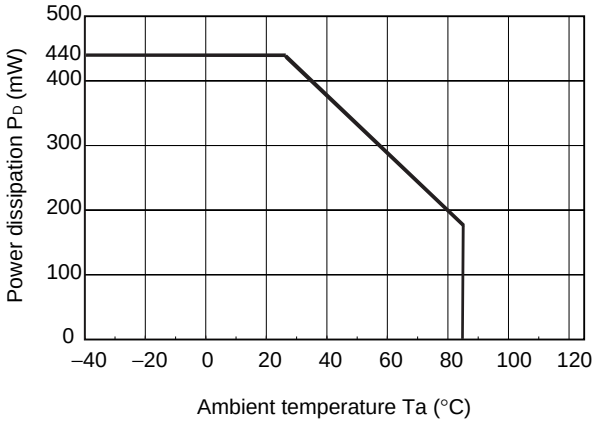

• Measurement circuit




Output current setting pin voltage vs. output current setting pin current




Power dissipation vs. ambient temperature



## ■ FUNCTIONAL DESCRIPTION

### 1. Switching Regulator Functions

#### (1) Reference voltage circuit (Ref)

The reference voltage circuit generates a temperature-compensated stable voltage (≒1.50 V). This reference voltage is used as the reference voltage and bias level for the power control unit.

#### (2) Triangular-wave oscillator circuit

By connecting a timing capacitor and a resistor to the $C_T$ (pin1) and the $R_T$ (pin2) terminals, it is possible to generate any desired triangular oscillation waveform.

#### (3) Error amplifier

The error amp. is an amplifier circuit that detects the output voltage from the switching regulator and produces the PWM control signal. The broad in-phase input voltage range of 0 V to Vcc – 0.9 V provides easy setting from external power supplies and enables use with applications such as DC motor speed control systems.

Also, it is possible to provide stable phase compensation for a system by setting up any desired level of loop gain, by connecting feedback resistance and a capacitor between the error amp. output pin (FB pin (pin 5)) and the inverse input pin (–IN pin (pin 4)).

#### (4) PWM comparator (PWM Comp.)

This is a voltage comparator with one inverted input and three non-inverted inputs, and operates as a voltage-pulse width modulator controlling output duty in relation to input voltage.

The output transistor is turned on during the interval in which the triangular waveform is lower than any of three voltages: the error amp. output voltage (FB pin (pin 5)), soft start set voltage (CS pin (pin 13)), or dwell time setting voltage (DTC pin (pin 6)).

#### (5) Output circuits (OUT)

The output circuit has totem pole type configuration, and can drive an external PNP transistor.

The on current value can be set up to a maximum of 30 mA using the resistance (RE) connected to the VE pin (pin 11).

The off current is set by connecting a bootstrap capacitor $C_B$ between the CP1 pin (pin 7) and CP2 pin (pin 8).

### 2. Power Supply Control Functions

The output is switched on and off according to the voltage level at the CTL pin (pin 15).

| CTL pin voltage level | Channel on/off status |
|---|---|
| L (≦0.7 V) | Standby mode* |
| H (≧2.1 V) | Operating mode |

* : Supply current in standby mode is 10 μA or less.

### 3. Protective Circuit Functions

#### (1) Soft start and short protection circuits (CS, SCP)

Soft starting, by preventing a rush current at power-on, can be provided by connecting a capacitor $C_S$ to the CS pin (pin 13).

After the soft start operation is completed, the CSCP pin (pin 14) is held at “L” level (standby voltage $V_{STB}$), which functions as short detection standby mode. If an output short causes the error amp. output to rise above 1.5 V, capacitor $C_{SCP}$ begins charging, and after reaching threshold voltage $V_{TH}$ of 0.65 V causes the OUT pin (pin 10) to be fixed at “H” level and the dwell time to be set to 100%, and the CSCP pin (pin 14) is held at “L” level.

Once the protection circuit has been activated, the power supply must be reset to restore operation.

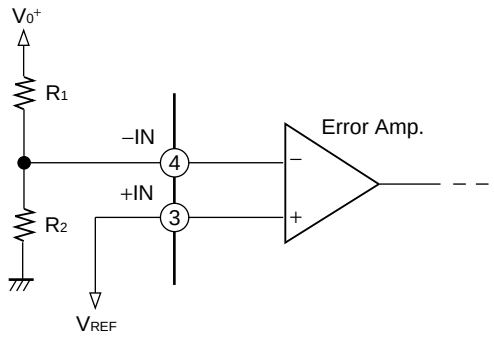
**(2) Low input voltage error prevention circuit (UVLO)**

Power-on surges and momentary drops in power supply voltage can cause errors in control IC operation, which can destroy or damage systems. The low input voltage error protection circuit compares the supply voltage to the internal reference voltage, and sets the OUT pin (pin 10) to “H” level in the event of a drop in supply voltage.

Operation is restored when the power supply voltage returns above the threshold voltage of the low input voltage error prevention circuit.

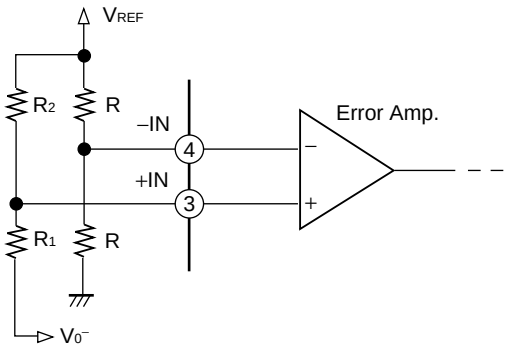
## ■ SETTING OUTPUT VOLTAGE

- **Output voltage $V_O$ is plus**




$$V_0^+ = \frac{V_{REF}}{R_2}(R_1 + R_2)$$

- **Output voltage $V_O$ is minus**




$$V_0^- = -\frac{V_{REF}}{2 \times R_2}(R_1 + R_2) + V_{REF}$$

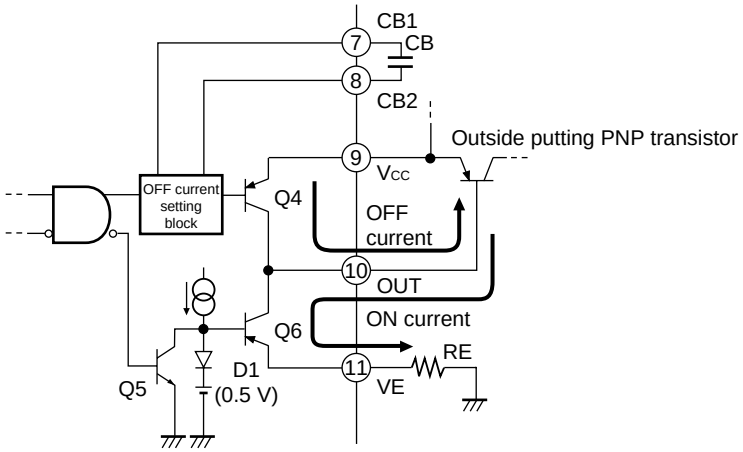
## ■ METHOD OF SETTING THE OUTPUT CURRENT

The output circuit is comprised of a totem-pole configuration. Its output current waveform is such that the ON-current value is set by constant current and the OFF-current value is set by a time constant. These output currents are set using the equations below.

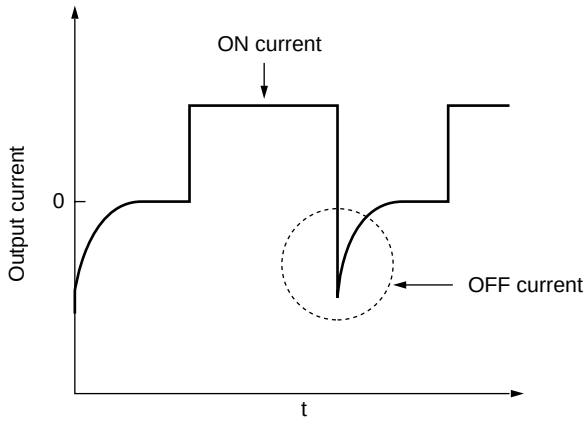
ON current: $I_{O^+}$ [mA] $\fallingdotseq \frac{500}{R_E\ [\Omega]}$ (Voltage on output current-setting pin $V_E$ = 0.5 V)

OFF current: OFF-current time constant = proportional to the value of $C_B$

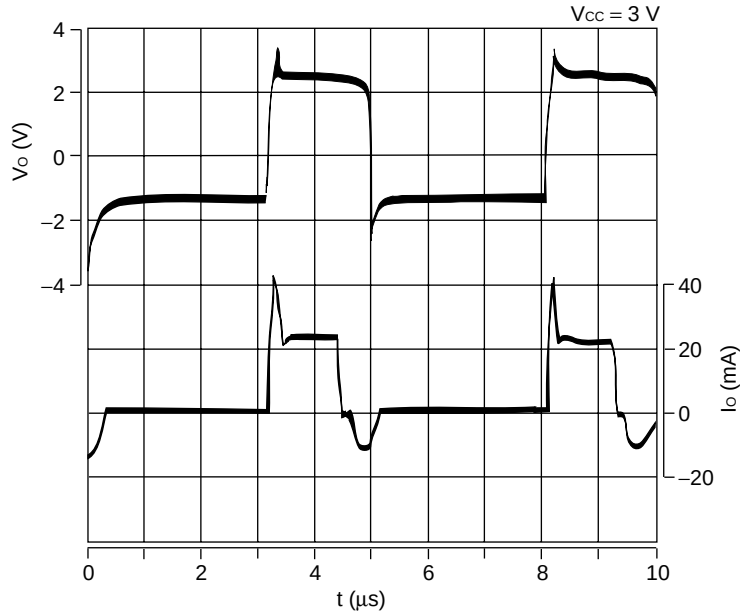
- **Output circuit**



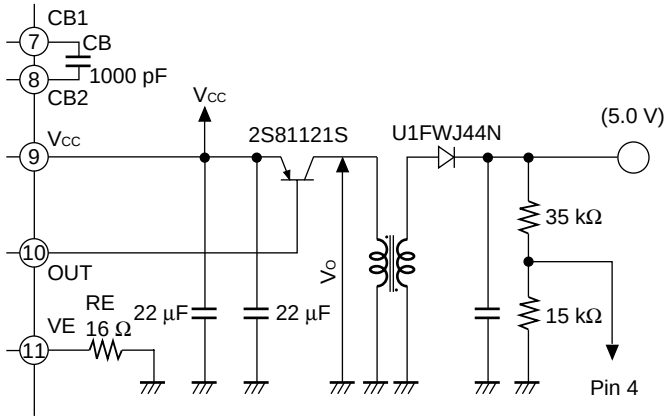

- **Output current waveform**



- **Voltage and current waveforms on output pin**




- **Measuring circuit diagram**



## ■ METHOD OF SETTING THE SHORT DETECTION TIME

The error amp. output is connected to the inverted input of the short detector comparator circuit (SCP Comp.), where it is constantly compared to the reference voltage of approximately 1.5 V that is connected to the non-inverted input.

If the switching regulator load conditions are stabilized, the short detector comparator output is at “H” level, transistor Q3 is on, and the CSCP pin (pin14) holds the input standby voltage $V_{STB}$ which is 50 mV.

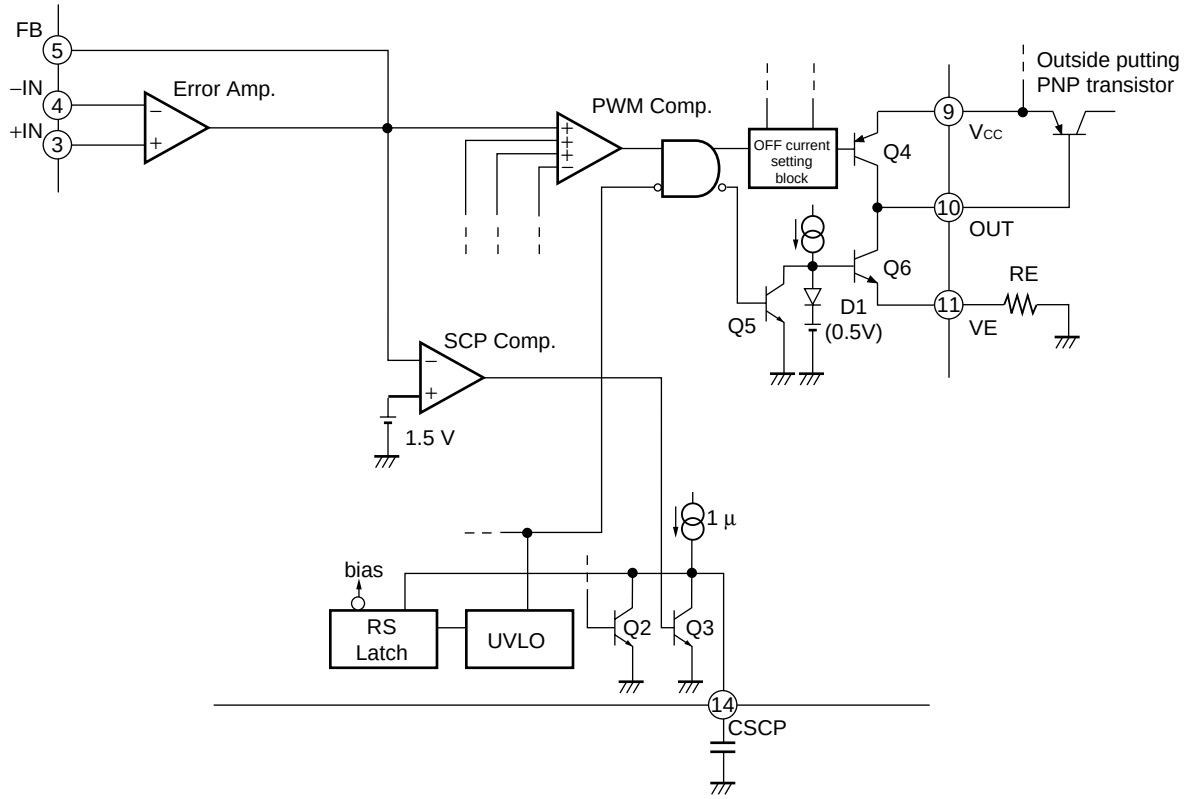
If load conditions change rapidly due to a cause such as a load short, so that output voltage falls, the short detector comparator circuit output changes to “L” level. When this happens, transistor Q3 turns off and the short detector capacitor $C_{SCP}$ connected externally to the CSCP pin starts charging from the input source current $I_I$, which is –1.0 μA.

Short detection time ($t_{PE}$)

$$t_{PE}\,[s] \fallingdotseq 0.65 \times C_{SCP}\,[\mu F]$$

When the short detector capacitor $C_{SCP}$ has been charged to the threshold voltage $V_{TH}$, which is 0.65 V, the SR latch is set, and the external PNP transistor is turned off (setting dwell time to 100%). At this time, the SR latch input is closed, and the CSCP pin is set to input latch voltage $V_I$ which is 50 mV.

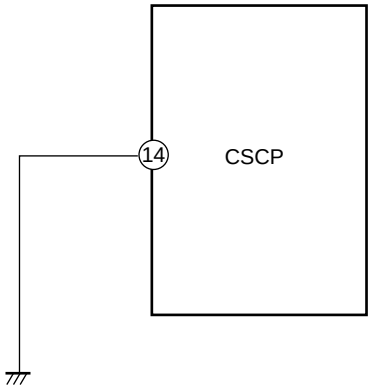
- **Short protection circuit**



## ■ TREATMENT WHEN NOT USING CSCP

When you do not use the timer/latch-actuated short-circuiting protection circuit, connect the CSCP terminal (pin 14) to GND.

- **Treatment when not using CSCP**



## ■ METHOD OF SETTING SOFT START TIME

To protect against surge currents when the IC is turned on, a soft start setting can be made by connecting a soft start capacitor ($C_S$) to the CS pin (pin 13).

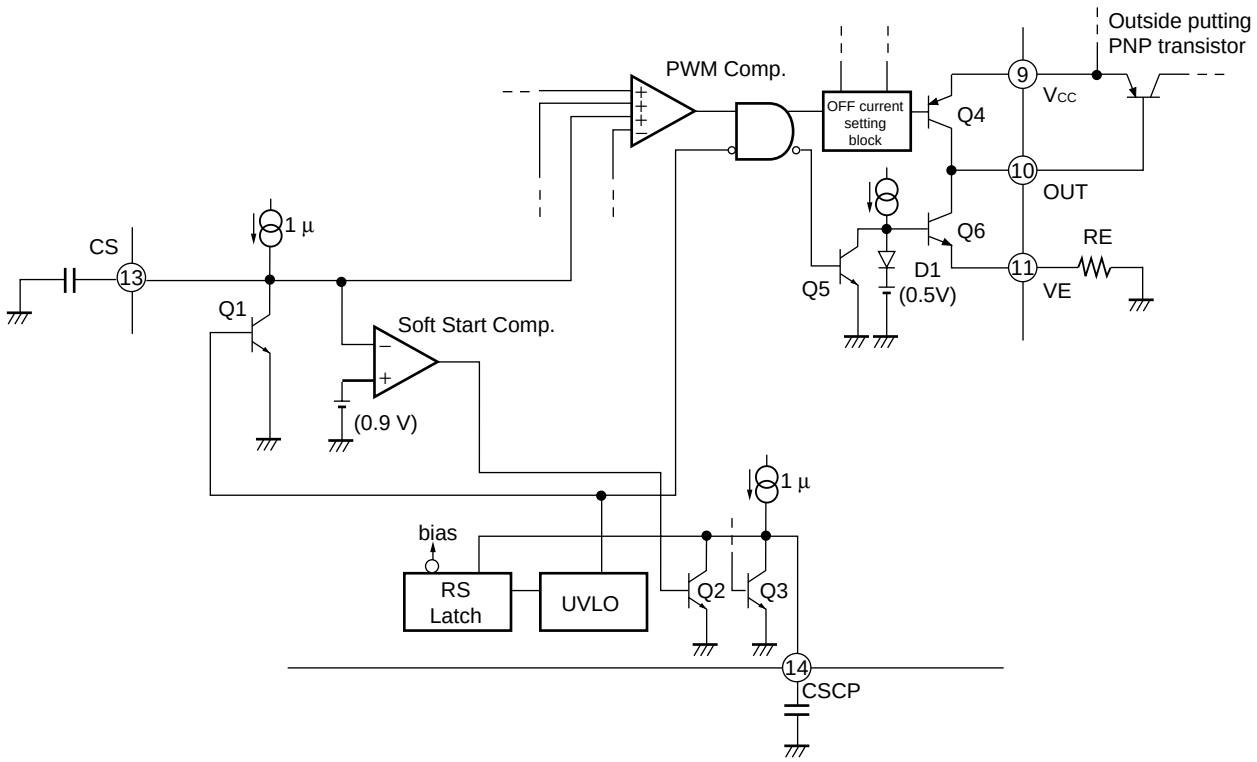
When the IC starts up (CTL pin (pin 15) to "H" level, Vcc ≧ UVLO threshold voltage $V_{TH}$) the transistor Q1 turns off and the soft start capacitor ($C_S$) connected to the CS pin begins charging from the charge current $I_{CHG}$ which is –1.0 μA.

At this time, if the CS pin voltage is less than 0.9 V, the soft start comparator circuit output goes to "H" level, transistor Q2 turns on and the CSCP pin (pin 14) holds input standby voltage $V_{STB}$ which is 50 mV so that the short protection circuit is not activated. When the CS pin voltage is greater than or equal to 0.9 V, transistor Q2 turns off, the PWM comparator circuit compares the CS pin voltage with the triangular wave and changes the ON duty of the OUTPUT pin, thus achieving a soft start. Note that the soft start time is determined by the following formula.

Soft start time (time before output ON duty reaches 50%)

$$t_S\ [ms] \fallingdotseq 1.2 \times C_S\ [\mu F]$$

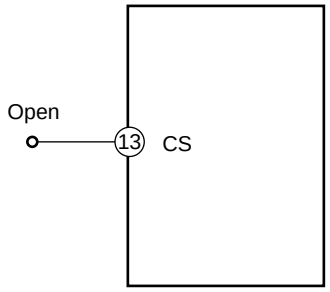
- **Soft start circuit**



## ■ TREATMENT WHEN NOT USING CS

When not using the soft start function, the CS pin (pin 13) should be left open.

- **When no soft start time is set**



## ■ METHOD OF SETTING THE DEAD TIME

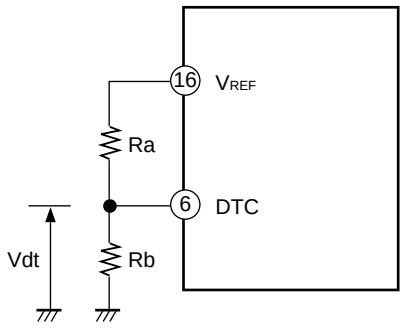
When the device is set for step-up inverted output based on the flyback method, the output transistor is fixed to a full-on state (ON-duty = 100 %) at power switch-on. To prevent this problem, you may determine the voltages on the DTC terminals (pin 6) from the $V_{REF}$ voltage so you can easily set the output transistor's dead time (maximum ON-duty) independently for each channel as shown below.

When the voltage on the DTC terminals (pin 6) is lower than the triangular-wave output voltage from the oscillator, the output transistor turns off. The dead time calculation formula assuming that triangular-wave amplitude ≅ 0.4 V and triangular-wave minimum voltage ≅ 1.4 V is given below.

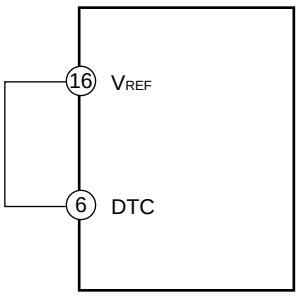
$$\text{Duty (ON)}_{MAX} \fallingdotseq \frac{Vdt - 1.0\ V}{0.4} \times 100\ [\%]$$

When you do not use these DTC terminals, connect them to $V_{REF}$ terminal.

- **When using DTC to set dead time**




- **When not using DTC to set dead time**

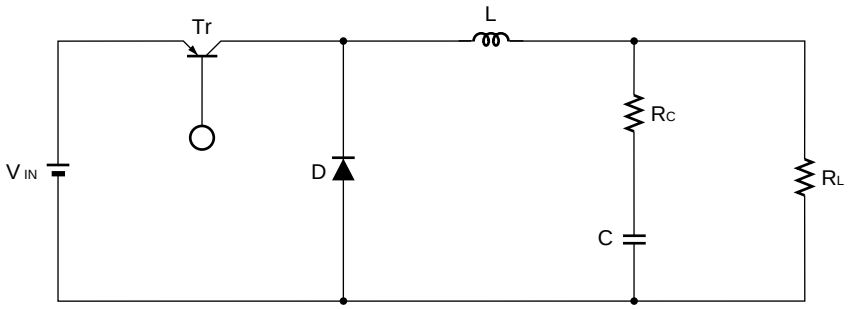


## ■ EQUIVALENT SERIES RESISTOR AND STABILITY OF SMOOTHING CAPACITOR

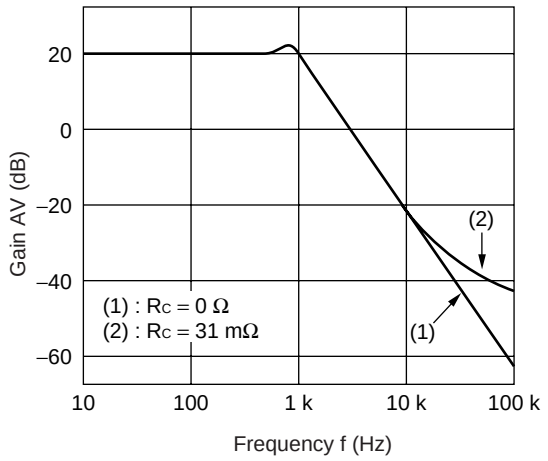
The equivalent series resistance (ESR) of a smoothing capacitor in a DC/DC converter greatly affects the phase characteristics of the loop depending on its value.

System stability is improved by ESR because it causes the phase to lead that of the ideal capacitor in high-frequency regions. (See Figures 2 and 3) Conversely, if a low-ESR smoothing capacitor is used, system stability deteriorates. Therefore, use of a low-ESR semiconductor electrolytic capacitors (ex. OS–CON) or tantalum capacitors calls for careful attention.

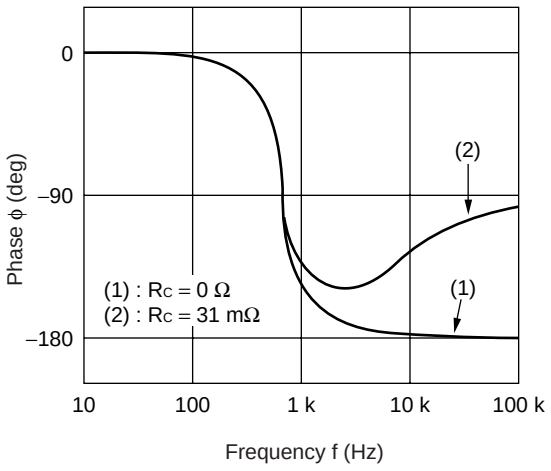
• **Figure 1 Basic circuit of stepdown DC/DC converter**




• **Figure 2 Gain-Frequency characteristic**



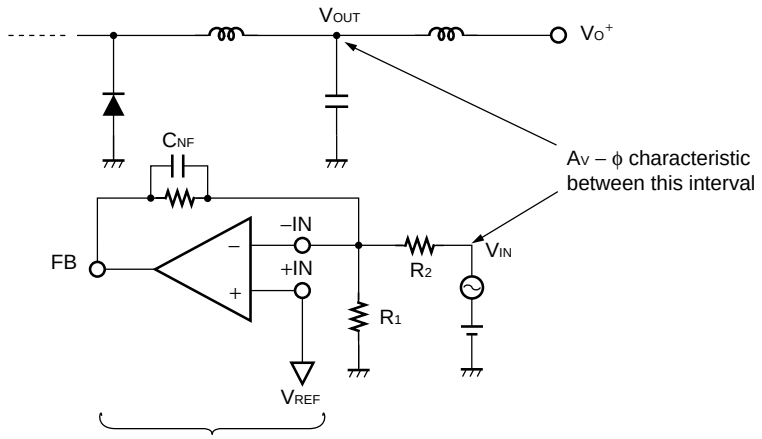

• **Figure 3 Phase-Frequency characteristic**



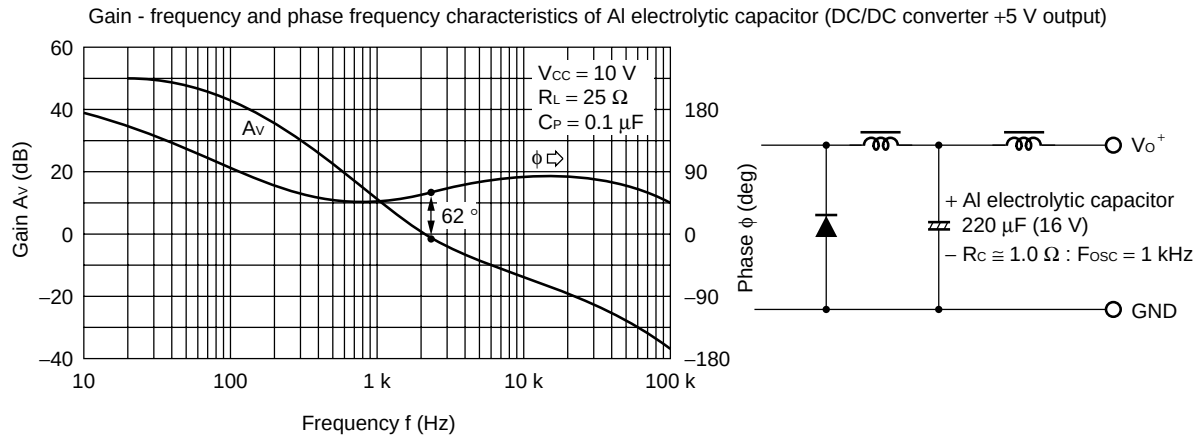
**(Reference Data)**

The phase margin is halved by changing the smoothing capacitor from an aluminium electrolytic capacitor ($R_C \simeq 1.0\ \Omega$) to a small-ESR semiconductor electrolytic capacitor (OS – CON; $R_C \simeq 0.2\ \Omega$). (See Figure 5 and 6.)

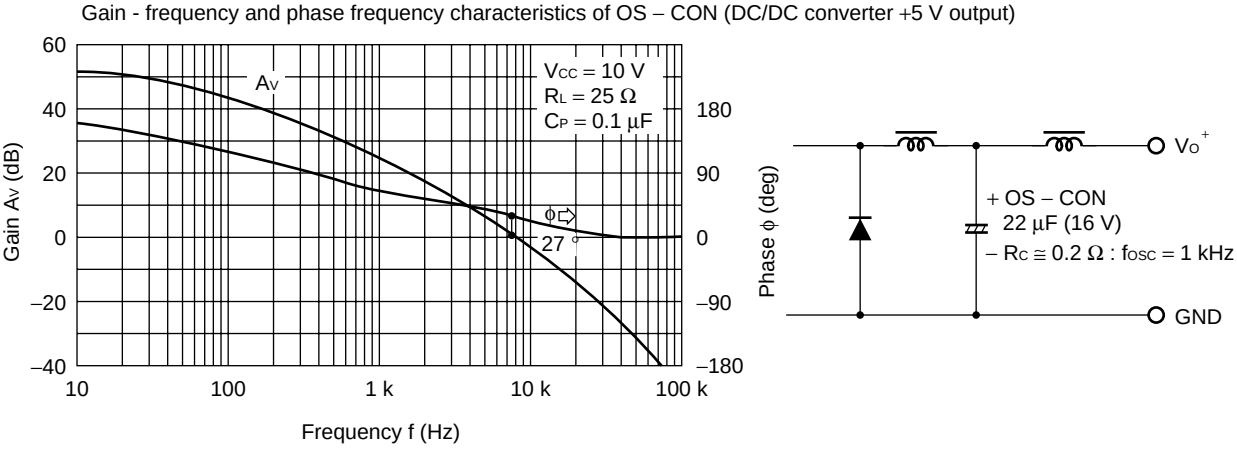
- **Figure 4 DC/DC converter $A_V$ – $\phi$ characteristic measuring circuit**




- **Figure 5 Gain-Frequency characteristic**

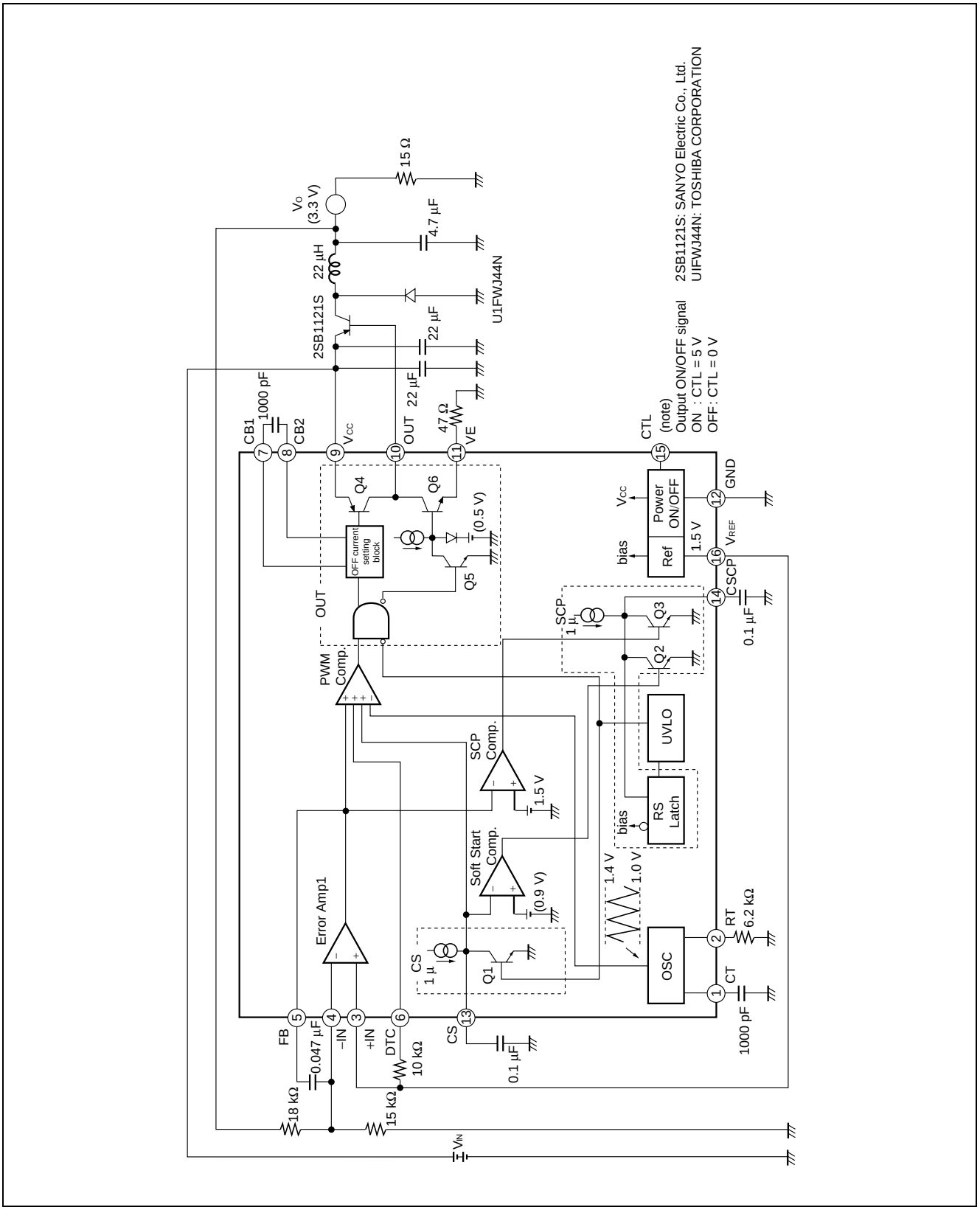



- **Figure 6 Phase-Frequency characteristic**

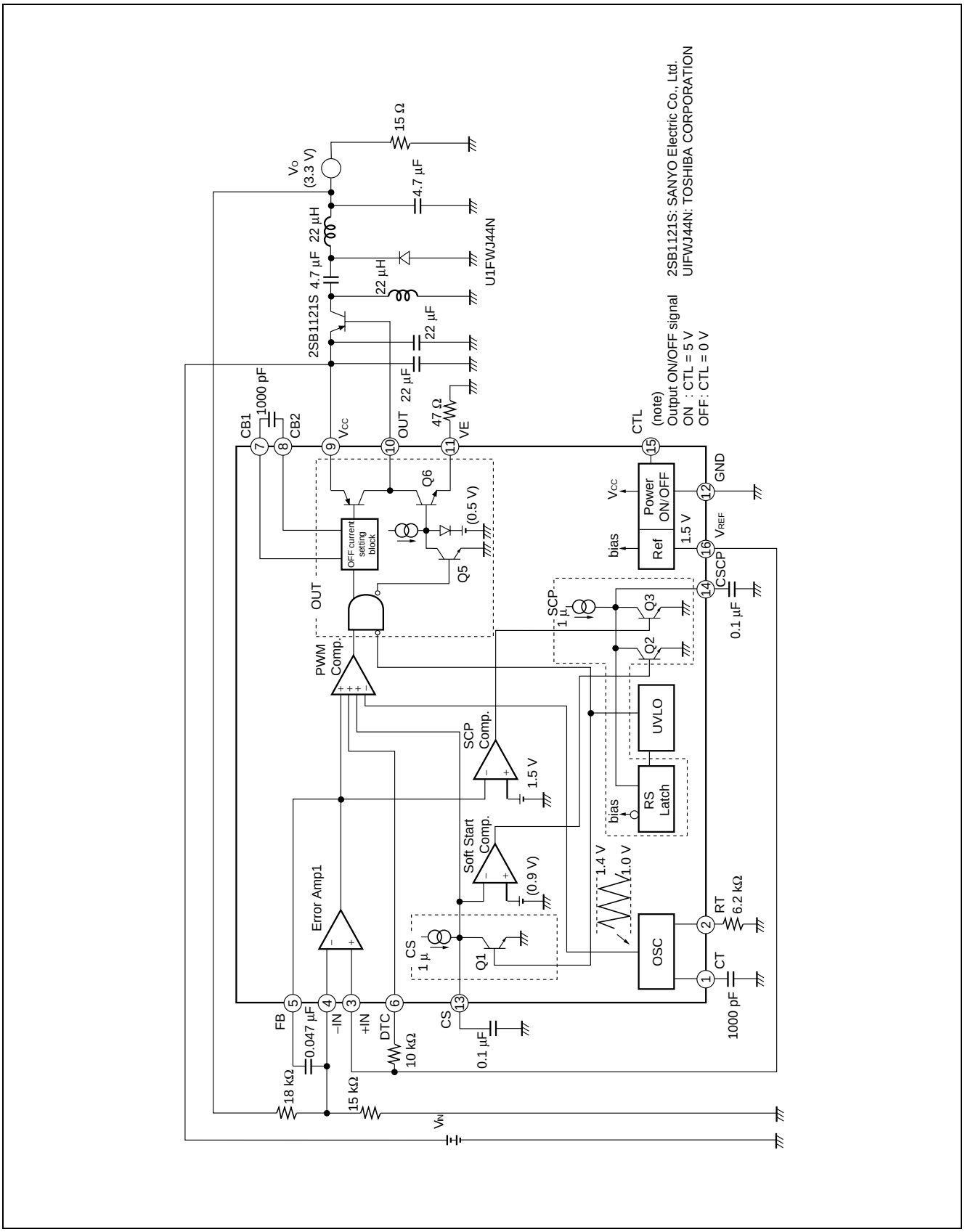


## ■ APPLICATION EXAMPLE

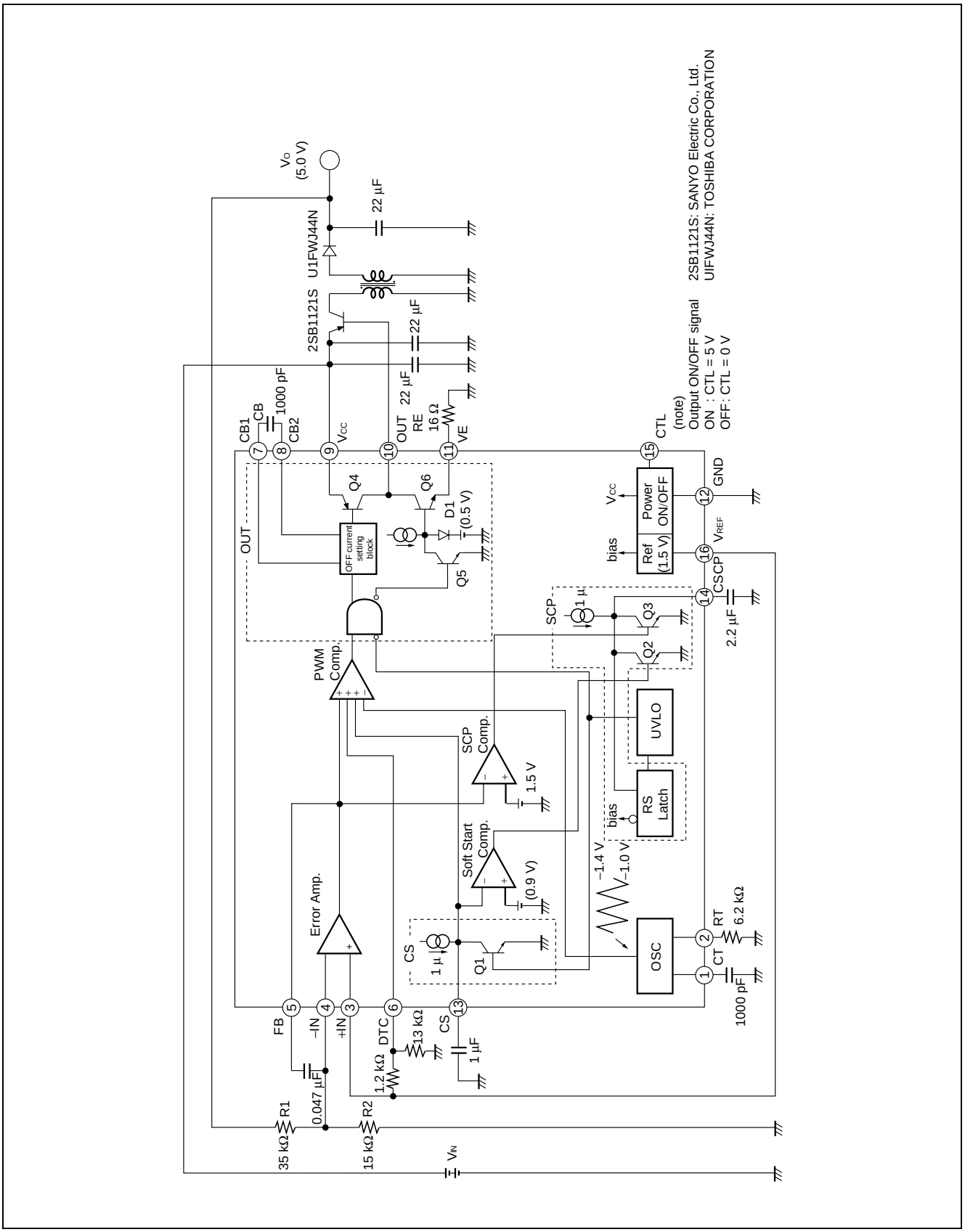
### 1. Step-down scheme



## 2. Zeta scheme



## 3. Flyback scheme



## ■ USAGE PRECAUTIONS

### 1. Never use setting exceeding maximum rated conditions.

Exceeding maximum rated conditions may cause permanent damage to the LSI.

Also, it is recommended that recommended operating conditions be observed in normal use. Exceeding recommended operating conditions may adversely affect LSI reliability.

### 2. Use this device within recommended operating conditions.

Recommended operating conditions are values within which normal LSI operation is warranted.

Standard electrical characteristics are warranted within the range of recommended operating conditions and within the listed conditions for each parameter.

### 3. Printed circuit board ground lines should be set up with consideration for common impedance.

### 4. Take appropriate static electricity measures.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

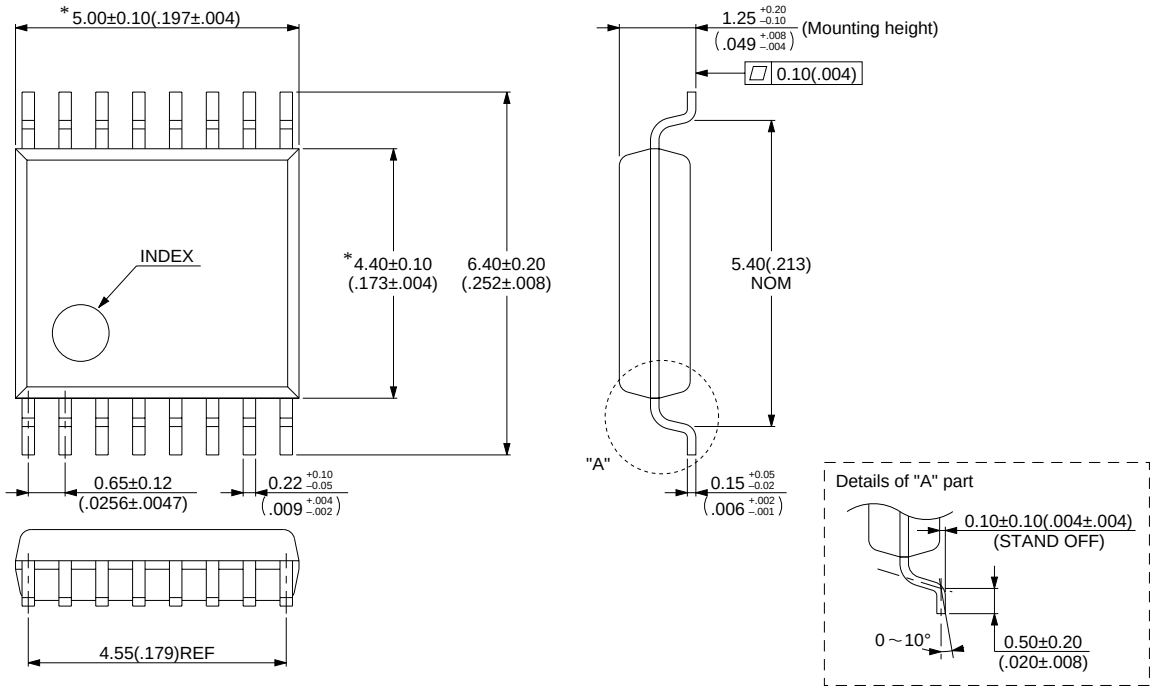
## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB3817PFV | 16-pin Plastic SSOP<br>(FPT-16P-M05) | |

## ■ PACKAGE DIMENSION

16-pin Plastic SSOP
(FPT-16P-M05)

*: These dimensions do not include resin protrusion.






Dimensions in mm (inches)

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