

# MB84256A-70/-70L/-70LL/-10/-10L/-10LL CMOS 256K-BIT LOW POWER SRAM

## 32,768 WORD x 8-BIT CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION

The Fujitsu MB84256A is a 32,768-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The MB84256A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

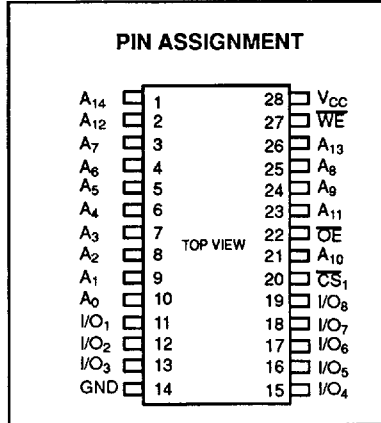
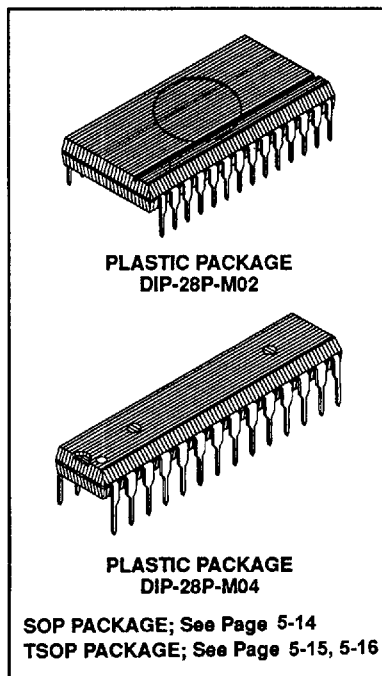
- Organization: 32,768 x 8 bits
- Fast access time: 70 ns max. (MB84256A-70/-70L/-70LL)  
100 ns max. (MB84256A-10/-10L/-10LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three state outputs
- Single +5V power supply,  $\pm 10\%$  tolerance
- Low power standby:
  - CMOS level: 5.5 mW max. (MB84256A-70/-10)  
0.55 mW max. (MB84256A-70L/-70LL/-10L/-10LL)
  - TTL level: 16.5 mW max. (MB84256A-70/-70L/-70LL/-10/-10L/-10LL)
- Data retention: 2.0V min.
- Standard 28-pin Plastic Packages:
 

DIP (600mil)	MB84256A-xx(L/LL)P
Skinny DIP (300 mil)	MB84256A-xx(L/LL)P-SK
SOP	MB84256A-xx(L/LL)PF
TSOP (normal bend)	MB84256A-xx(L/LL)PFTN
TSOP (reverse bend)	MB84256A-xx(L/LL)PFTR

### ABSOLUTE MAXIMUM RATINGS (see NOTE)

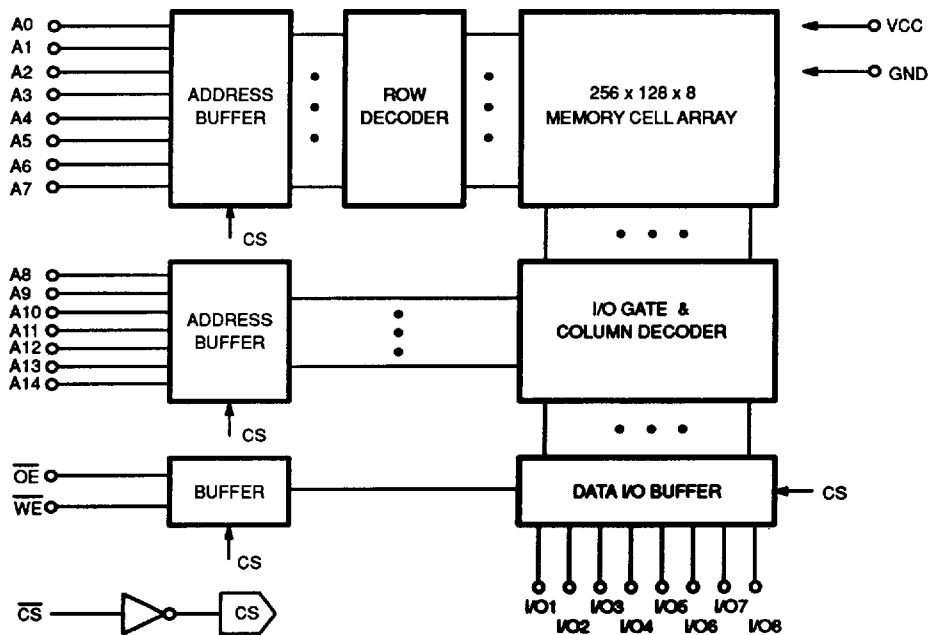
Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	-0.5 to +7.0	V
Input Voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
Output Voltage	$V_{VO}$	-0.5 to $V_{CC} + 0.5$	V
Temperature Under Bias	$T_{BIAS}$	-10 to +85	$^{\circ}C$
Storage Temperature	$T_{STG}$	-40 to +125	$^{\circ}C$

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 - MB84256A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	ISB	High-Z
L	H	H	DOUT Disable	ICC	High-Z
L	L	H	Read	ICC	DOUT
L	X	L	Write	ICC	DIN

**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ( $V_{I/O} = 0V$ )	C <sub>I/O</sub>			8	pF
Input Capacitance ( $V_{IN} = 0V$ )	C <sub>IN</sub>			7	pF

## RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ambient Temperature	T <sub>A</sub>	0		70	°C

## DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

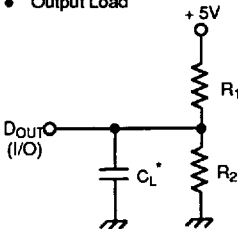
Parameter	Symbol	Test Condition	MB84256A-70/-10		MB84256A-70L/-70LL /-10L/-10LL		Unit
			Min	Max	Min	Max	
Standby Supply Current	I <sub>SB1</sub>	$\overline{CS} \geq V_{CC} - 0.2V$		1		0.1	mA
	I <sub>SB2</sub>	$\overline{CS} = V_{IH}$		3		3	mA
Active Supply Current	I <sub>CC1</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , CS = V <sub>IL</sub> I <sub>OUT</sub> = 0mA		50		50	mA
Operating Supply Current	I <sub>CC2</sub>	Cycle = Min. Duty = 100% I <sub>OUT</sub> = 0mA		80		80	mA
			-70		70		
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0V to V <sub>CC</sub>	-1	1	-1	1	µA
Output Leakage Current	I <sub>LVO</sub>	V <sub>VO</sub> = 0V to V <sub>CC</sub> CS = V <sub>IH</sub> or OE = V <sub>IH</sub> or WE = V <sub>IL</sub>	-1	1	-1	1	µA
Input High Voltage	V <sub>IH</sub>		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>		-3.0*	0.8	-3.0*	0.8	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4		2.4		V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA		0.4		0.4	V

Note: All voltages are referenced to GND.

\*: -3.0V min. for pulse width less than 20 ns. (V<sub>IL</sub> min. = -0.3V at DC level.)

Fig. 2 – AC TEST CONDITIONS

• Output Load



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V<sub>IL</sub>=0.8V, V<sub>IH</sub>=2.2V  
Output: V<sub>OL</sub>=0.8V, V<sub>OH</sub>=2.0V

\* Including Jig and stray capacitance

	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t <sub>CLZ</sub> , t <sub>CHZ</sub> , t <sub>WLZ</sub> , and t <sub>WHZ</sub>
Load II	1.8KΩ	990Ω	5pF	t <sub>CLZ</sub> , t <sub>CHZ</sub> , t <sub>WLZ</sub> , and t <sub>WHZ</sub>

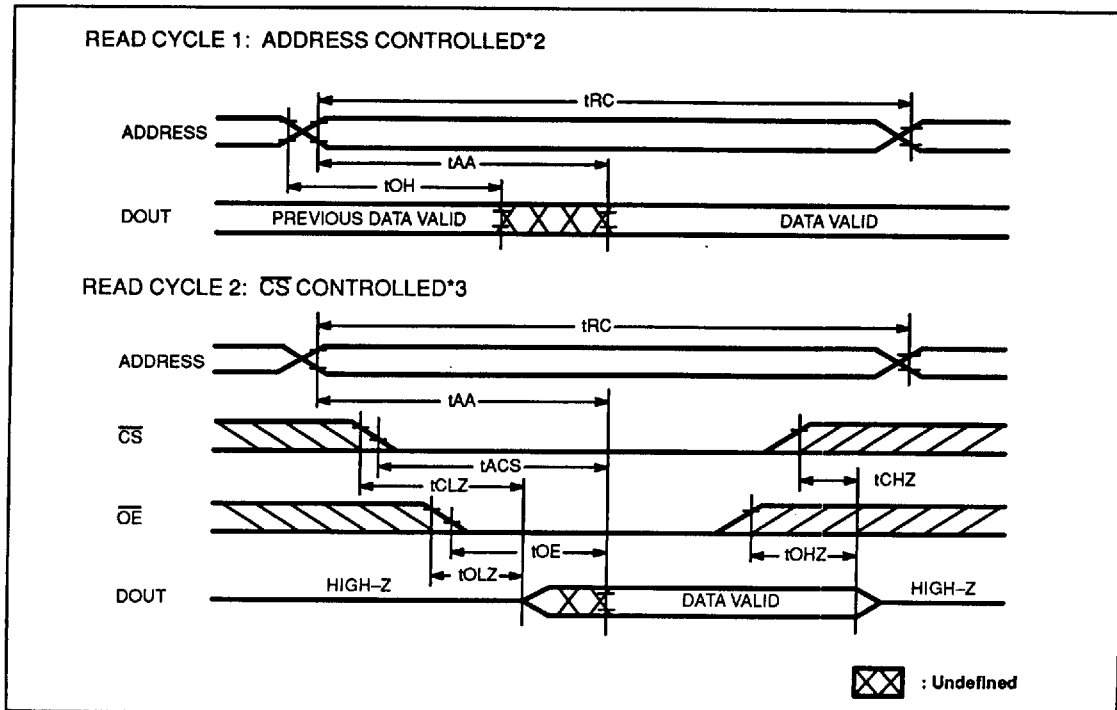
## AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

### READ CYCLE \*1

Parameter	Symbol	MB84256A-70/-70L/-70LL		MB84256A-10/-10L/-10LL		Unit
		Min	Max	Min	Max	
Read Cycle Time	$t_{RC}$	70		100		ns
Address Access Time *2	$t_{AA}$		70		100	ns
$\overline{CS}$ 1 Access Time *3	$t_{ACS}$		70		100	ns
Output Enable to Output Valid	$t_{OE}$		35		40	ns
Output Hold from Address Change	$t_{OH}$	20		20		ns
Chip Select to Output Low-Z *4	$t_{CLZ}$	10		10		ns
Output Enable to Output Low-Z *4	$t_{OLZ}$	5		5		
Chip Select to Output High-Z *4	$t_{CHZ}$		25		40	ns
Output Enable to Output High-Z *4	$t_{OHZ}$		25		40	

### READ CYCLE TIMING DIAGRAM \*1



Note: \*1  $\overline{WE}$  is high for Read cycle.

\*2 Device is continuously selected,  $\overline{CS} = \overline{OE} = \text{VIL}$ .

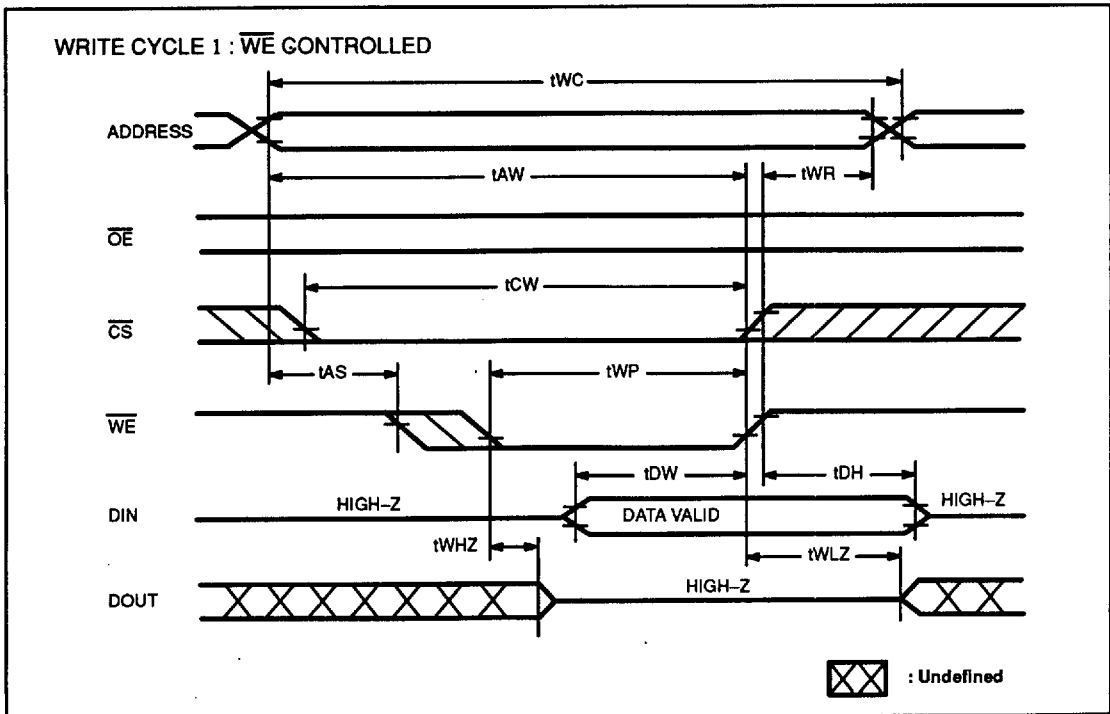
\*3 Address valid prior to or coincident with  $\overline{CS}$  transition low.

\*4 Transition is measured at the point of  $\pm 500\text{mV}$  from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE \*1\*2

Parameter	Symbol	MB84256A-70/-70L/-70LL		MB84256A-10/-10L/-10LL		Unit
		Min	Max	Min	Max	
Write Cycle Time *3	$t_{WC}$	70		100		ns
Address Valid to End of Write	$t_{AW}$	50		80		ns
Chip Select to End of Write	$t_{CW}$	50		80		ns
Data Valid to End of Write	$t_{DW}$	25		40		ns
Data Hold Time	$t_{DH}$	0		0		ns
Write Pulse Width	$t_{WP}$	50		60		ns
Address Setup Time	$t_{AS}$	0		0		ns
Write Recovery Time *4	$t_{WR}$	5		5		ns
$\overline{WE}$ to Output Low-Z *5	$t_{WLZ}$	5		5		ns
$\overline{WE}$ to Output High-Z *5	$t_{WHZ}$		25		40	ns

WRITE CYCLE TIMING DIAGRAM \*1 \*2

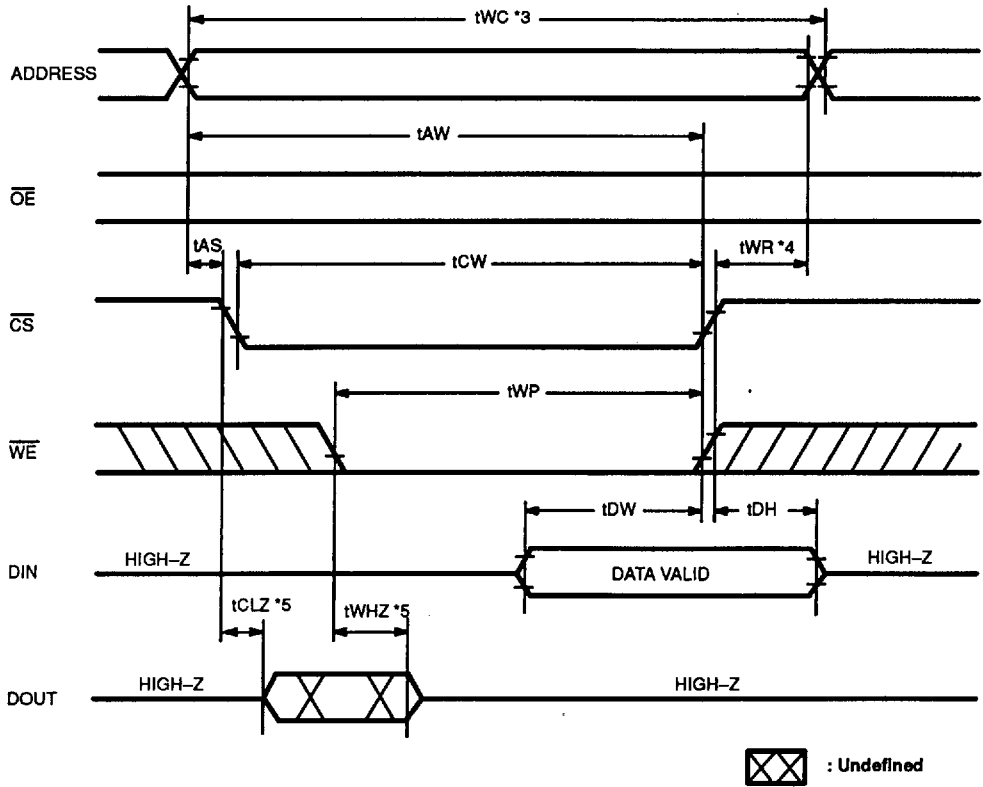


- Note: \*1 If  $\overline{OE}$ ,  $\overline{CS}$  are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.  
 \*2 If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in high impedance state.  
 \*3 All write cycle are determined from last address transition to the first address transition of the next address.  
 \*4  $t_{WR}$  is defined from the end point of WRITE Mode..  
 \*5 Transition is measured at the point of  $\pm 500mV$  from steady state voltage with specified Load I in Fig. 2.

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WRITE CYCLE TIMING DIAGRAM \*1 \*2

WRITE CYCLE 2 :  $\overline{CS}$  CONTROLLED



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- Note: \*1 If  $\overline{OE}$ ,  $\overline{CS}$  are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.  
 \*2 If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in high impedance state.  
 \*3 All write cycle are determined from last address transition to the first address transition of the next address.  
 \*4  $t_{WR}$  is defined from the end point of WRITE Mode..  
 \*5 Transition is measured at the point of  $\pm 500mV$  from steady state voltage with specified Load II in Fig. 2.

# DATA RETENTION CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

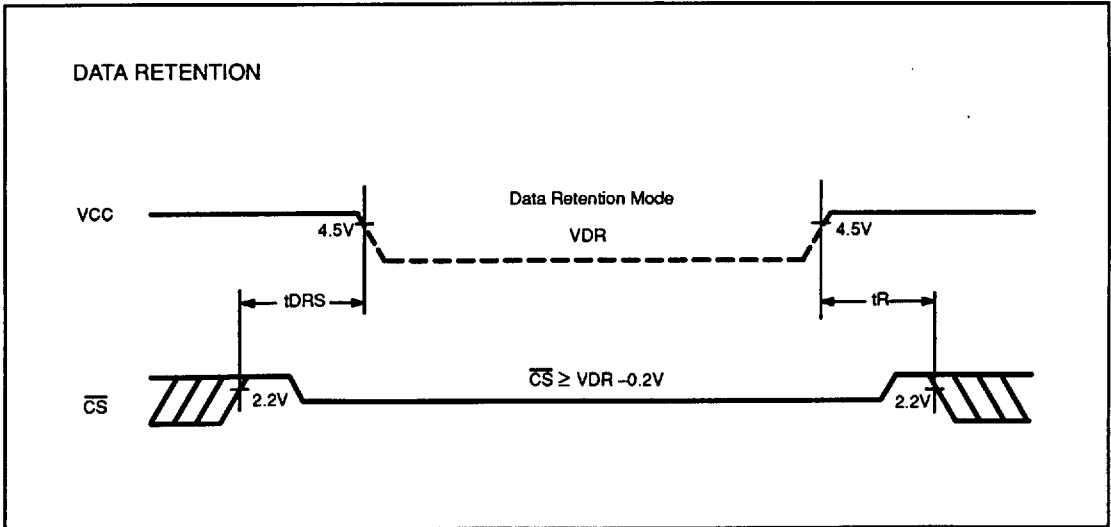
Parameter	Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage *1	VDR	2.0		5.5	V
Data Retention Supply Current *2	Standard			1.0	mA
	L-Version		1.0	50	μA
	LL-Version		1.0	50 *3	
Data Retention Setup Time	tDRS	0			ns
Operation Recovery Time	tR	tRC			ns

Note: \*1  $\overline{CS} \geq VDR - 0.2V$

\*2 VDR = 3.0V,  $\overline{CS} \geq VDR - 0.2V$

\*3 IDR = 5 μA max. at VDR = 3.0V, TA = 40°C

## DATA RETENTION TIMING



## TYPICAL CHARACTERISTICS CURVES

Fig. 3 - NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

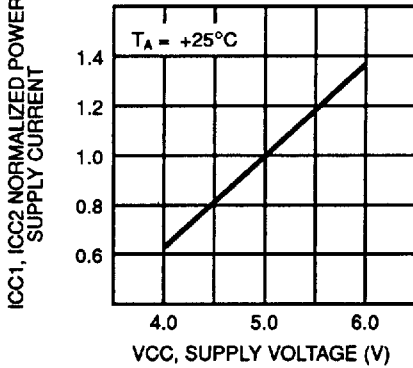


Fig. 4 - NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

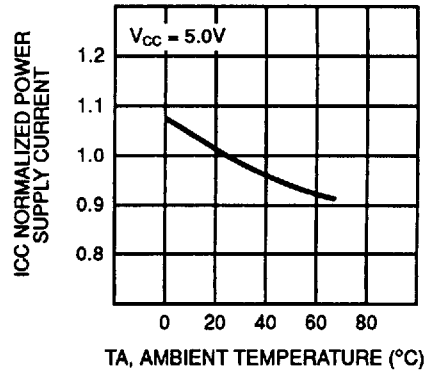


Fig. 5 - NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

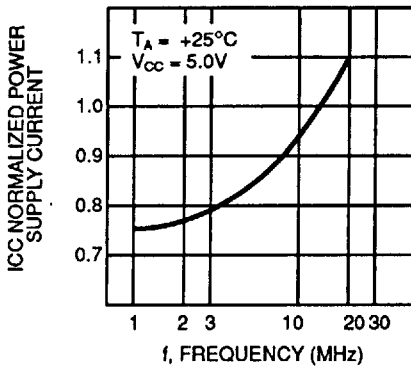


Fig. 6 - NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

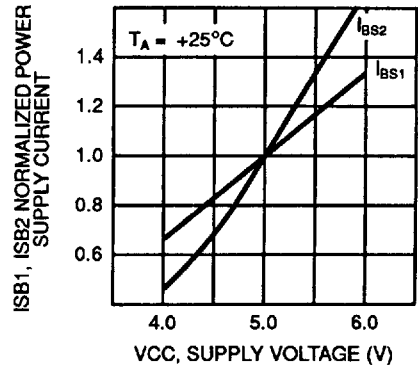


Fig. 7 - NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

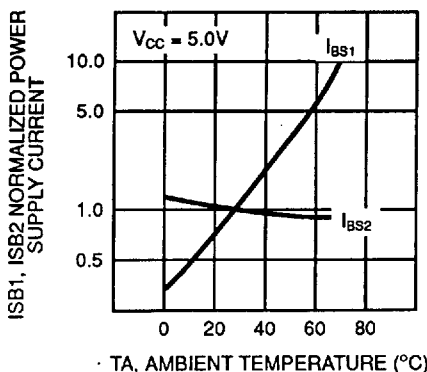
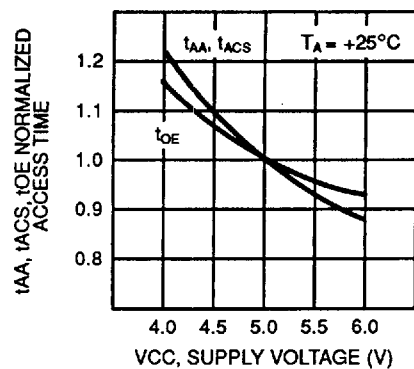


Fig. 8 - NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE





## TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 9 - NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

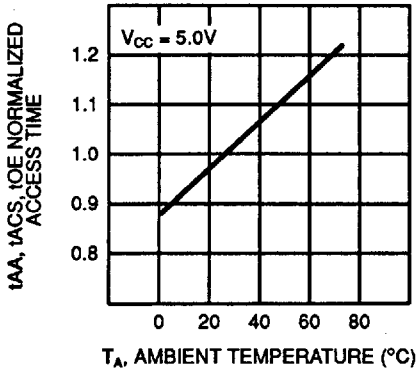
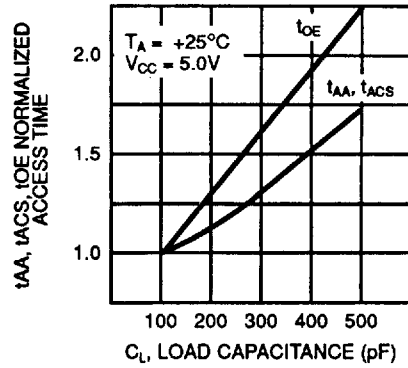


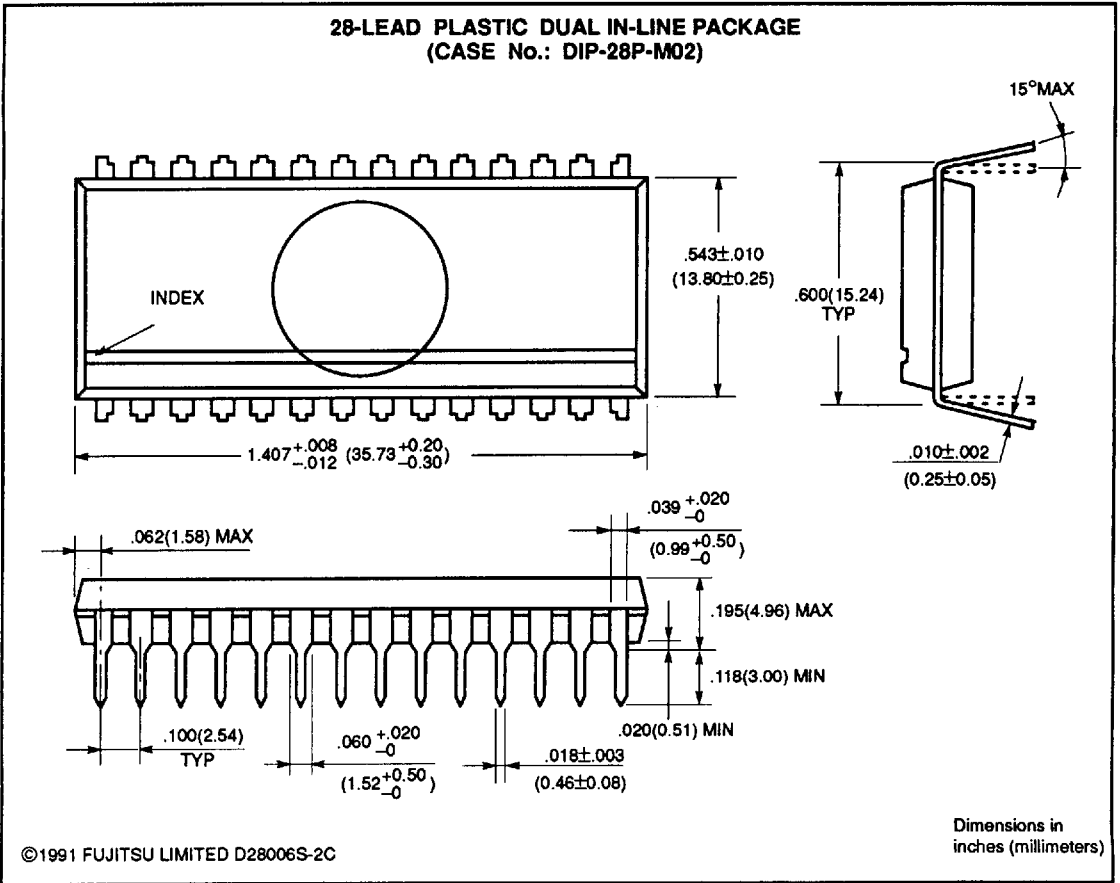
Fig. 10 - NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE



MB84256A-70/-70L/-70LL  
MB84256A-10/-10L/-10LL

# PACKAGE DIMENSIONS

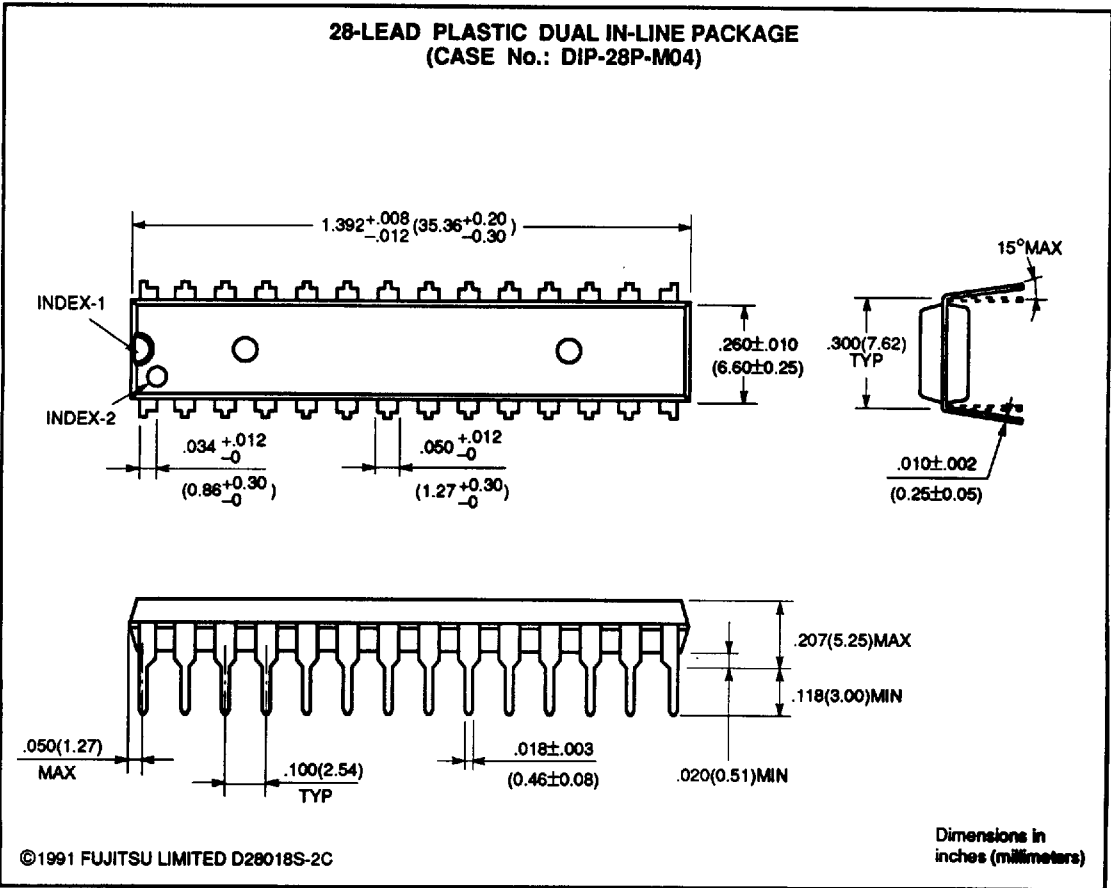
(Suffix: P)



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**PACKAGE DIMENSIONS (Continued)**  
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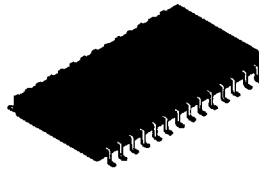
**28-LEAD PLASTIC DUAL IN-LINE PACKAGE**  
 (CASE No.: DIP-28P-M04)



MB84256A-70/-70L/-70LL  
 MB84256A-10/-10L/-10LL

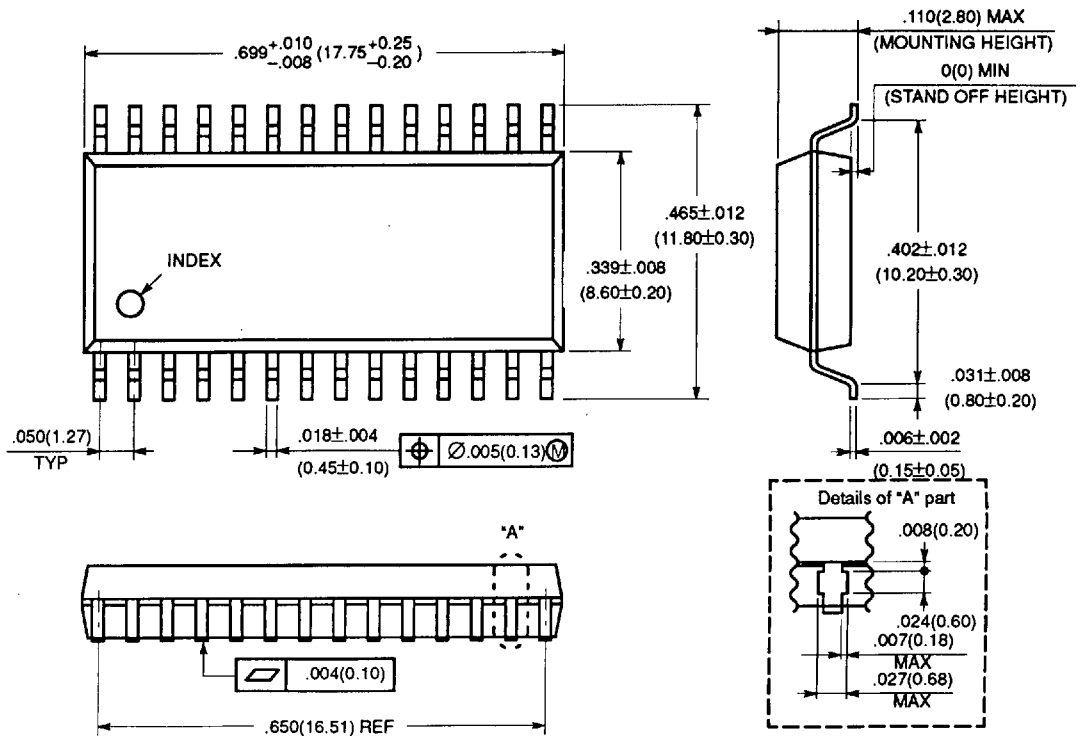
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(Suffix: PF)



FPT-28P-M02

## 28-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-28P-M02)



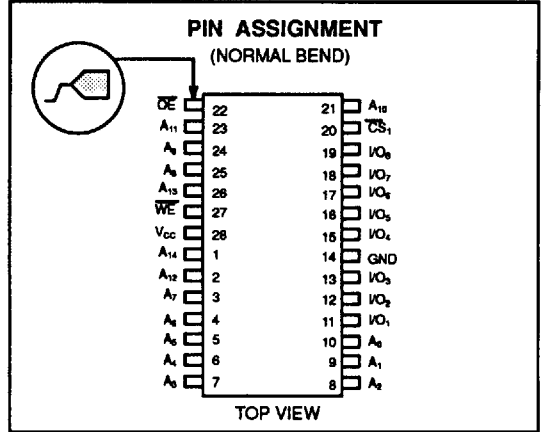
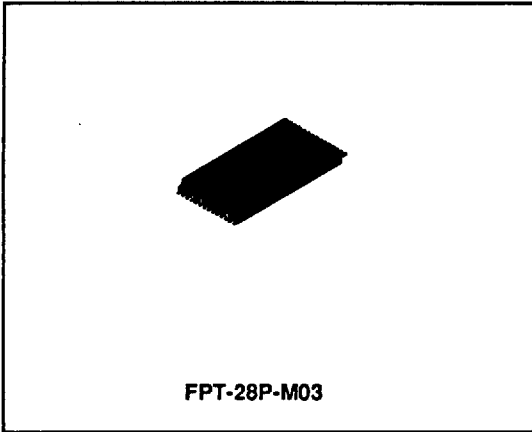
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Dimensions in inches (millimeters)

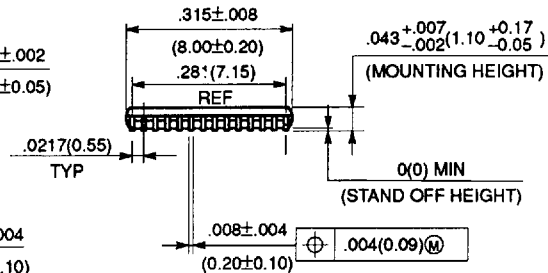
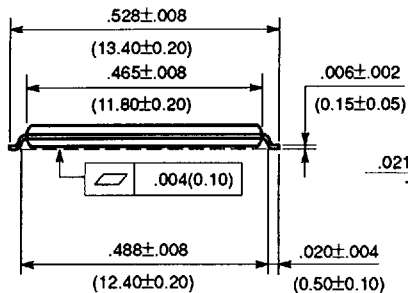
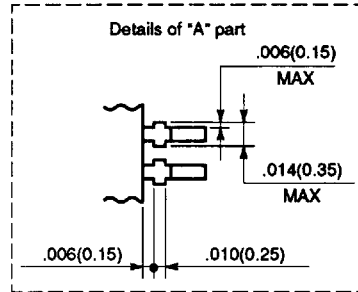
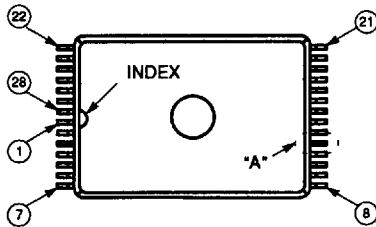
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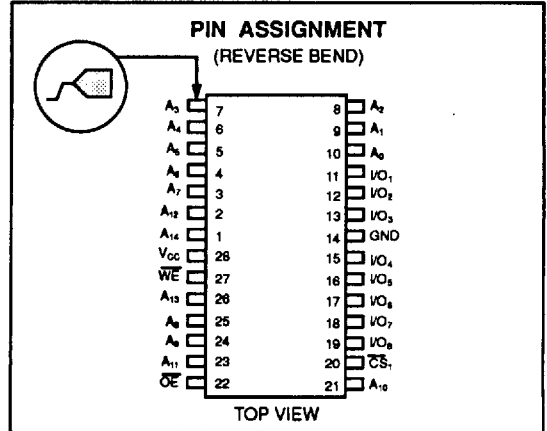
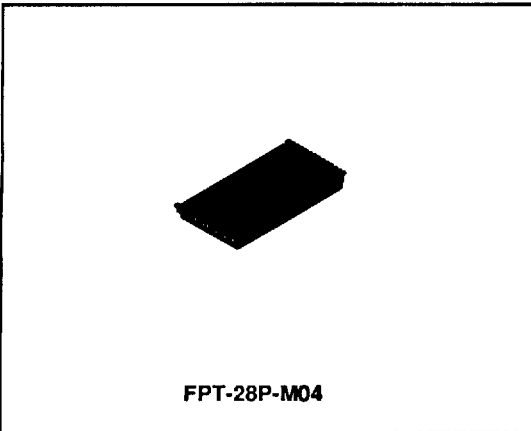


## 28-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-28P-M03)

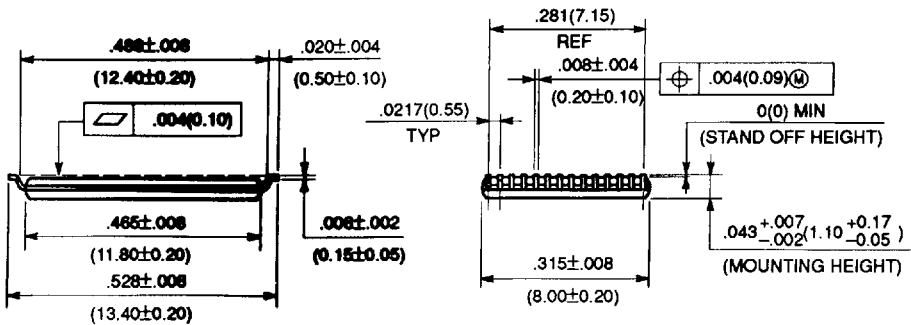
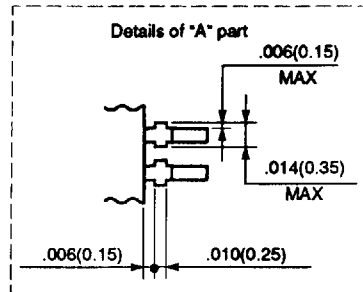
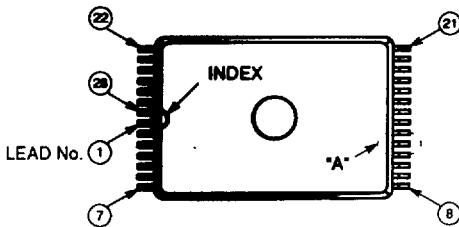


# PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)



## 28-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-28P-M04)



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