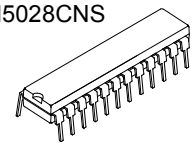
# 16-bit Constant Current LED Sink Driver with Gain Control

## Features

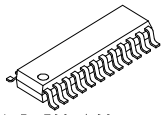
- 16 constant-current output channels
- Output current adjustable through an external resistor
- Output current gain programmable for White Balance
- Constant output current range: 5-90 mA
- Excellent output current accuracy:
  between channels: ±3% (max.), and
  between ICs: ±6% (max.)
- Constant output current invariant to load voltage change
- Fast response of output current, $\overline{OE}$ (min.): 200 ns
- 25MHz clock frequency
- Schmitt trigger input
- 5V supply voltage

MBI5028CNS



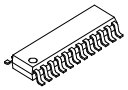
SDIP24-P-300-1.78
Weight: 1.11g(typ)

MBI5028CF



SOP24-P-300-1.00
Weight: 0.28g(typ)

MBI5028CP



SSOP24-P-150-0.64
Weight: 0.11g(typ)

| Current Accuracy | | Conditions |
|---|---|---|
| Between Channels | Between ICs | |
| < ±3% | < ±6% | $I_{OUT}$ = 10 mA ~ 60 mA |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## Product Description

MBI5028 succeeds MBI5026 and is designed for LED displays with Gain Control extension. MBI5028 exploits PrecisionDrive™ technology to enhance its output characteristics. MBI5028 contains a serial buffer and data latches, which convert serial input data into parallel output format. At MBI5028 output stage, sixteen regulated current ports are designed to provide constant current sinks for driving LEDs within a wide range of Vf variations.

MBI5028 provides users with great flexibility and device performance while using MBI5028 in their LED panel system design. Users may adjust the output current from 5 mA to 90 mA through an external resistor $R_{ext}$, which gives users flexibility in controlling the light intensity of LEDs. MBI5028 guarantees to endure maximum 17V at the output port. The high clock frequency, 25 MHz, also satisfies the system requirements of high volume data transmission.

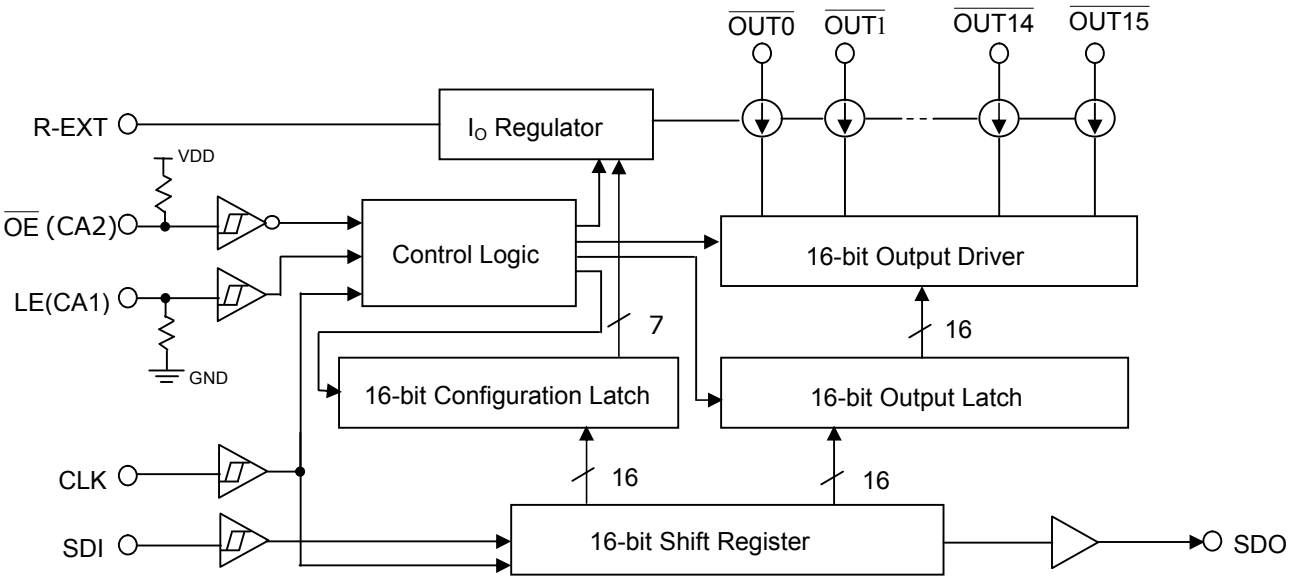
MBI5028 also exploits Share-I-O™ technology and is backward compatible with MBI5026 in both electrical characteristics and package aspect. To utilize the Current Adjust feature with Share-I-O™ technology, users may not need to change the printed circuit board originally for MBI5026. To enter a special function mode- Current Adjust mode, users just need to set a sequence of signals on LE(CA1), $\overline{OE}$ (CA2) and CLK input pins. Normally, the output current can be regulated only through an external resistor. In addition, in the Current Adjust mode, the output current can be software-programmable by a system controller. The system controller adjusts the output current by sending a 7-bit Current Adjust code to 16-bit Configuration Latch through MBI5028 SDI pin. The code will be latched and effective to control the output current regulator. A fine adjustment of the output current could be achieved by a gain ranging from 0.5 to 2 with 128 fine steps. By setting another sequence of signals on LE(CA1), $\overline{OE}$ (CA2) and CLK input pins, MBI5028 may resume to a Normal mode and perform as MBI5026. The Shift Register, with SDI, SDO, and CLK, carries the image data as usual.

**A Share-I-O™ technique** is specifically applied to MBI5028. By means of the Share-I-O™ technique, an additionally effective function, Current Gain, can be added to LED drivers, however, without any extra pins. Thus, MBI5028 could be a drop-in replacement of MBI5026. The printed circuit board originally designed for MBI5026 may be also applicable for MBI5028.

For MBI5028, the pin 4, LE(CA1), and the pin 21, $\overline{OE}$ (CA2), can be acted as different functions as follows:

| Pin / Device Name | MBI5028 |
|---|---|
| Function Description of Pin 4 | LE + Current Adjust (CA1) |
| Function Description of Pin 21 | $\overline{OE}$ + Current Adjust (CA2) |

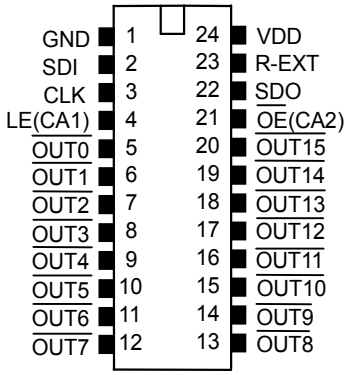
## Block Diagram




## Terminal Description

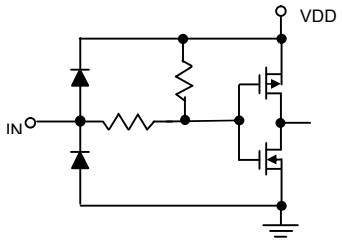
| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | GND | Ground terminal for control logic and current sink |
| 2 | SDI | Serial-data input to the Shift Register |
| 3 | CLK | Clock input terminal for data shift on rising edge |
| 4 | LE(CA1) | Data strobe input terminal<br>Serial data is transferred to the respective latch when LE(CA1) is high. The data is latched when LE(CA1) goes low.<br>Also, a control signal input for Current Adjust mode (See **Timing Diagram**) |
| 5~20 | $\overline{OUT0}$ ~ $\overline{OUT15}$ | Constant current output terminals |
| 21 | $\overline{OE}$ (CA2) | Output enable terminal<br>When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).<br>Also, a second control signal input for Current Adjust mode (See **Timing Diagram**) |
| 22 | SDO | Serial-data output to the following SDI of next driver IC |
| 23 | R-EXT | Input terminal used to connect an external resister for setting up all output current |
| 24 | VDD | 5V supply voltage terminal |

## Pin Configuration

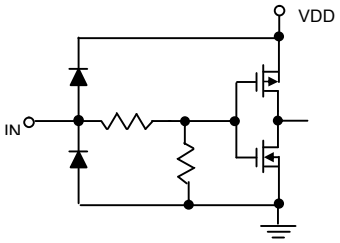


## Equivalent Circuits of Inputs and Outputs

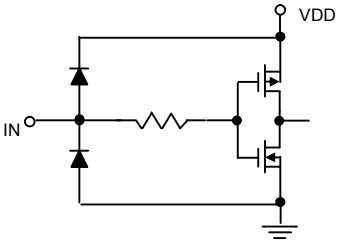
**$\overline{OE}$ (CA2) terminal**



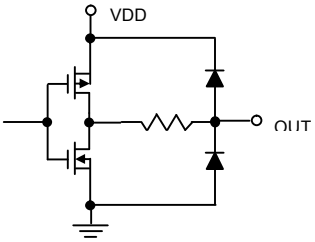

**LE(CA1) terminal**




**CLK, SDI terminal**

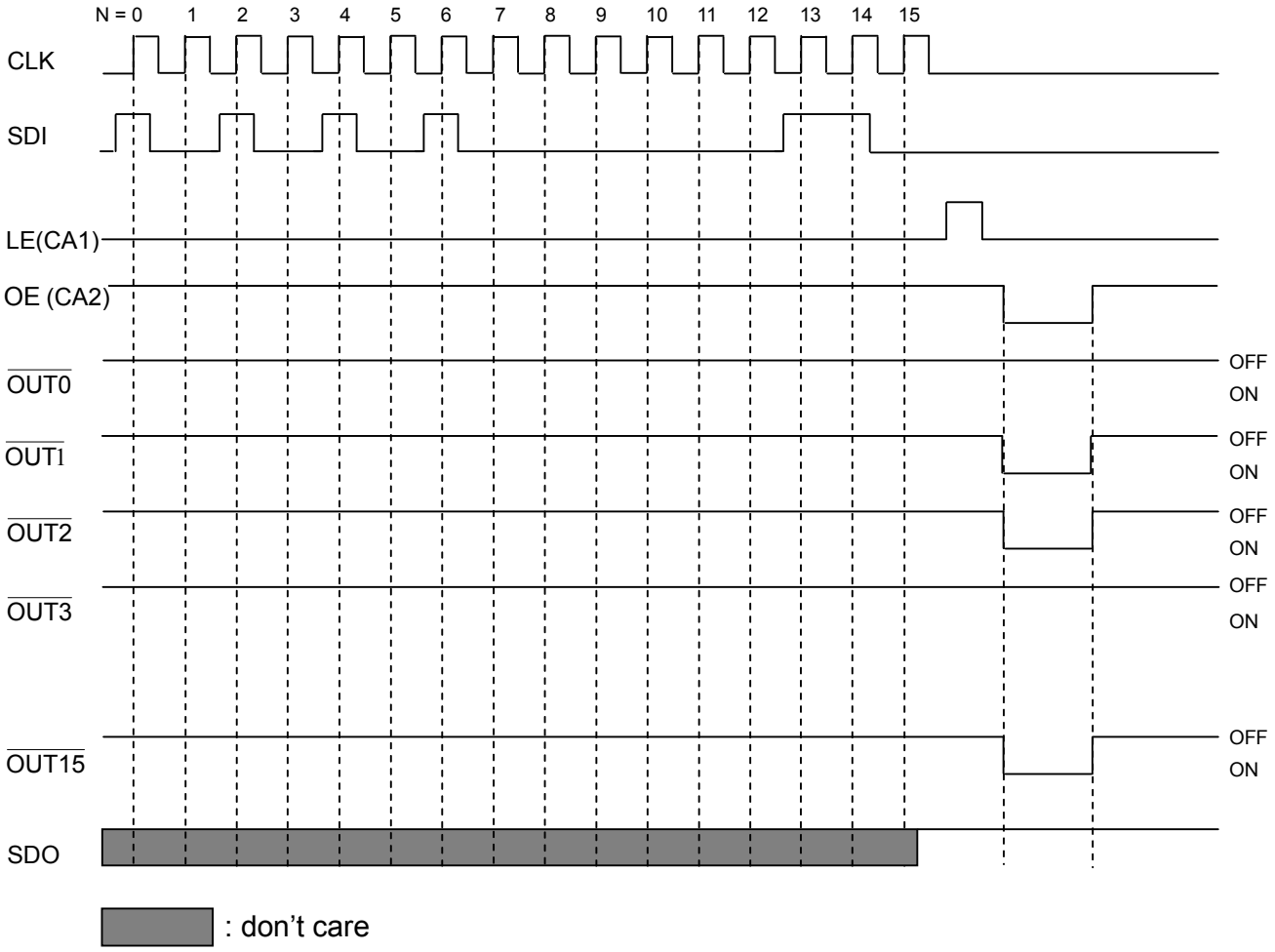



**SDO terminal**



## Timing Diagram

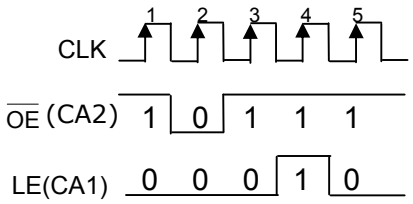
### Normal Mode




## Truth Table (In Normal Mode)

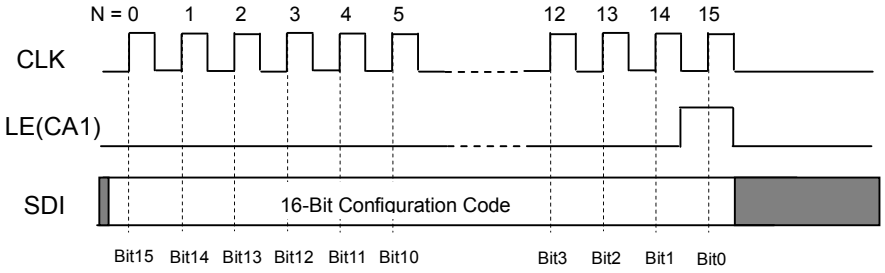
| CLK | LE | $\overline{OE}$ | SDI | $\overline{OUT0}$ ... $\overline{OUT7}$ ... $\overline{OUT15}$ | SDO |
|---|---|---|---|---|---|
| ↑ | H | L | $D_n$ | $\overline{D_n}$ ..... $\overline{D_{n-7}}$ .... $\overline{D_{n-15}}$ | $D_{n-15}$ |
| ↑ | L | L | $D_{n+1}$ | No Change | $D_{n-14}$ |
| ↑ | H | L | $D_{n+2}$ | $\overline{D_{n+2}}$ .... $\overline{D_{n-5}}$ .... $\overline{D_{n-13}}$ | $D_{n-13}$ |
| ↓ | X | L | $D_{n+3}$ | $\overline{D_{n+2}}$ .... $\overline{D_{n-5}}$ .... $\overline{D_{n-13}}$ | $D_{n-13}$ |
| ↓ | X | H | $D_{n+3}$ | Off | $D_{n-13}$ |

## Entering Current Adjust Mode




The signal sequence makes MBI5028 enter a **Current Adjust** mode.

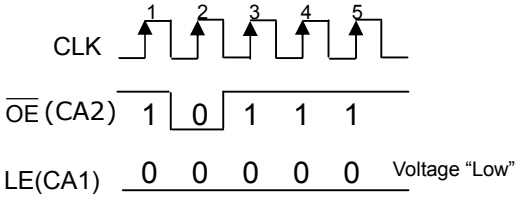
## Writing Configuration Code




**Note:**

Pin OE (CA2) always enables the output port no matter MBI5028 enters a Current Adjust mode or not. When entering the Current Adjust mode, by sending the positive pulse of LE(CA1), the content of the Shift Register, a Current Adjust code, will be written to the 16-Bit Configuration Latch.

## Resuming to Normal Mode




The signal sequence makes MBI5028 resume to a Normal mode.

**Note:**

If users want to know the whole process, that is how to enter a Current Adjust mode, write Current Adjust codes and resume to a Normal mode, please refer to the contents in **Application Information**.

## Maximum Ratings

| Characteristic | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Supply Voltage | | $V_{DD}$ | 0~7.0 | V |
| Input Voltage | | $V_{IN}$ | -0.4~$V_{DD}$ + 0.4 | V |
| Output Current | | $I_{OUT}$ | +90 | mA |
| Output Voltage | | $V_{DS}$ | -0.5~+20.0 | V |
| Clock Frequency | | $F_{CLK}$ | 25 | MHz |
| GND Terminal Current | | $I_{GND}$ | 1440 | mA |
| Power Dissipation (On PCB, Ta=25°C) | CNS – type | $P_D$ | 1.52 | W |
| | CF – type | | 1.30 | |
| | CP – type | | 1.11 | |
| Thermal Resistance (On PCB, Ta=25°C) | CNS – type | $R_{th(j-a)}$ | 82 | °C/W |
| | CF – type | | 96 | |
| | CP – type | | 112 | |
| Operating Temperature | | $T_{opr}$ | -40~+85 | °C |
| Storage Temperature | | $T_{stg}$ | -55~+150 | °C |

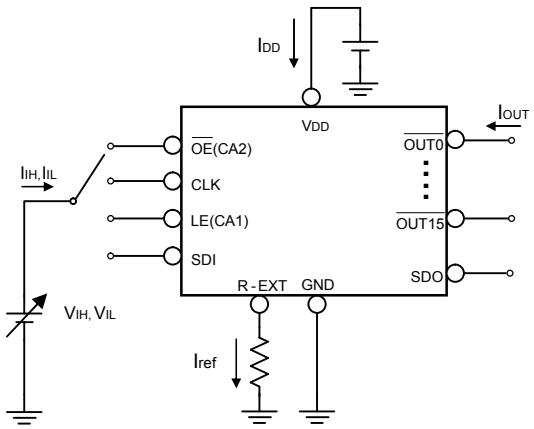
## Recommended Operating Conditions

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | - | 4.5 | 5.0 | 5.5 | V |
| Output Voltage | $V_{DS}$ | $\overline{OUT0}$ ~ $\overline{OUT15}$ | - | - | 17.0 | V |
| Output Current | $I_{OUT}$ | DC Test Circuit | 5 | - | 60 | mA |
| | $I_{OH}$ | SDO | - | - | -1.0 | mA |
| | $I_{OL}$ | SDO | - | - | 1.0 | mA |
| Input Voltage | $V_{IH}$ | CLK, $\overline{OE}$ (CA2), LE(CA1) and SDI | $0.8V_{DD}$ | - | $V_{DD}$+0.3 | V |
| | $V_{IL}$ | CLK, $\overline{OE}$ (CA2), LE(CA1) and SDI | -0.3 | - | $0.3V_{DD}$ | V |
| LE(CA1) Pulse Width | $t_{w(L)}$ | Normal Mode $V_{DD}$=4.5~5.5V | 40 | - | - | ns |
| $\overline{OE}$ (CA2) Pulse Width | $t_{w(OE)}$ | | 200 | - | - | ns |
| CLK Pulse Width | $t_{w(CLK)}$ | | 20 | - | - | ns |
| Setup Time for SDI | $t_{su(D)}$ | | 5 | - | - | ns |
| Hold Time for SDI | $t_{h(D)}$ | | 10 | - | - | ns |
| Setup Time for LE(CA1) | $t_{su(L)}$ | | 15 | - | - | ns |
| Hold Time for LE(CA1) | $t_{h(L)}$ | | 15 | - | - | ns |
| CLK Pulse Width | $t_{w(CLK)}$ | Current Adjust Mode $V_{DD}$=4.5~5.5V | 20 | - | - | ns |
| Setup Time for LE(CA1) | $t_{su(CA1)}$ | | 5 | - | - | ns |
| Hold Time for LE(CA1) | $t_{h(CA1)}$ | | 10 | - | - | ns |
| Setup Time for $\overline{OE}$ (CA2) | $t_{su(CA2)}$ | | 5 | - | - | ns |
| Hold Time for $\overline{OE}$ (CA2) | $t_{h(CA2)}$ | | 10 | - | - | ns |
| Clock Frequency | $F_{CLK}$ | Cascade Operation | - | - | 25.0 | MHz |
| Power Dissipation | $P_D$ | Ta=85°C (CNS type) | - | - | 0.79 | W |
| | | Ta=85°C (CF type) | - | - | 0.67 | |
| | | Ta=85°C (CP type) | - | - | 0.57 | |

## Electrical Characteristics

| Characteristic | | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Voltage | "H" level | $V_{IH}$ | Ta = -40~85ºC | | $0.8V_{DD}$ | - | $V_{DD}$ | V |
| | "L" level | $V_{IL}$ | Ta = -40~85ºC | | GND | - | $0.3V_{DD}$ | V |
| Output Leakage Current | | $I_{OH}$ | $V_{OH}$=17.0V | | - | - | 0.5 | μA |
| Output Voltage | SDO | $V_{OL}$ | $I_{OL}$=+1.0mA | | - | - | 0.4 | V |
| | | $V_{OH}$ | $I_{OH}$=-1.0mA | | 4.6 | - | - | V |
| Output Current 1 | | $I_{OUT1}$ | $V_{DS}$=0.6V | $R_{ext}$=720 Ω | - | 25.0 | - | mA |
| Current Skew | | $dI_{OUT1}$ | $I_{OL}$=25mA<br>$V_{DS}$=0.6V | $R_{ext}$=720 Ω | - | ±1 | ±3 | % |
| Output Current 2 | | $I_{OUT2}$ | $V_{DS}$=0.8V | $R_{ext}$=360 Ω | - | 50.0 | - | mA |
| Current Skew | | $dI_{OUT2}$ | $I_{OL}$=50mA<br>$V_{DS}$=0.8V | $R_{ext}$=360 Ω | - | ±1 | ±3 | % |
| Output Current vs. Output Voltage Regulation | | $\%/dV_{DS}$ | $V_{DS}$ within 1.0V and 3.0V | | - | ±0.1 | - | % / V |
| Output Current vs. Supply Voltage Regulation | | $\%/dV_{DD}$ | $V_{DD}$ within 4.5V and 5.5V | | - | ±1 | - | % / V |
| Pull-up Resister | | $R_{IN}$(up) | $\overline{OE}$ (CA2) | | 250 | 500 | 800 | KΩ |
| Pull-down Resister | | $R_{IN}$(down) | LE(CA1) | | 250 | 500 | 800 | KΩ |
| Supply Current | "OFF" | $I_{DD}$(off) 1 | $R_{ext}$=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | | - | 9 | - | mA |
| | | $I_{DD}$(off) 2 | $R_{ext}$=720 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | | - | 11 | - | |
| | | $I_{DD}$(off) 3 | $R_{ext}$=360 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | | - | 14 | - | |
| | "ON" | $I_{DD}$(on) 1 | $R_{ext}$=720 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On | | - | 11 | - | |
| | | $I_{DD}$(on) 2 | $R_{ext}$=360 Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On | | - | 14 | - | |

## Test Circuit for Electrical Characteristics

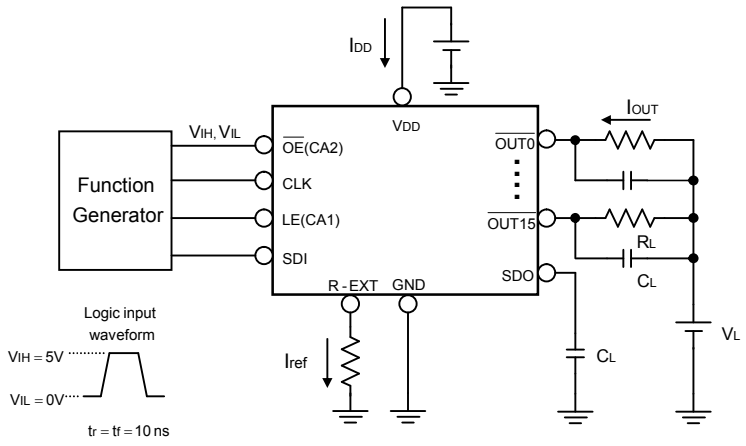


## Switching Characteristics

| Characteristic | | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Propagation Delay Time ("L" to "H") | CLK - $\overline{OUTn}$ | $t_{pLH1}$ | $V_{DD}$=5.0 V<br>$V_{DS}$=0.8 V<br>$V_{IH}$=$V_{DD}$<br>$V_{IL}$=GND<br>$R_{ext}$=300 Ω<br>$V_L$=4.0 V<br>$R_L$=52 Ω<br>$C_L$=10 pF | - | 50 | 100 | ns |
| | LE(CA1) - $\overline{OUTn}$ | $t_{pLH2}$ | | - | 50 | 100 | ns |
| | $\overline{OE}$ (CA2)- $\overline{OUTn}$ | $t_{pLH3}$ | | - | 20 | 100 | ns |
| | CLK - SDO | $t_{pLH}$ | | 15 | 20 | - | ns |
| Propagation Delay Time ("H" to "L") | CLK - $\overline{OUTn}$ | $t_{pHL1}$ | | - | 100 | 150 | ns |
| | LE(CA1) - $\overline{OUTn}$ | $t_{pHL2}$ | | - | 100 | 150 | ns |
| | $\overline{OE}$ (CA2)- $\overline{OUTn}$ | $t_{pHL3}$ | | - | 50 | 150 | ns |
| | CLK - SDO | $t_{pHL}$ | | 15 | 20 | - | ns |
| Pulse Width | CLK | $t_{w(CLK)}$ | | 20 | - | - | ns |
| | LE(CA1) | $t_{w(L)}$ | | 20 | - | - | ns |
| | $\overline{OE}$ (CA2) | $t_{w(OE)}$ | | 200 | - | - | ns |
| Hold Time for LE(CA1) | | $t_{h(L)}$ | | 5 | - | - | ns |
| Setup Time for LE(CA1) | | $t_{su(L)}$ | | 5 | - | - | ns |
| Maximum CLK Rise Time | | $t_r$** | | - | - | 500 | ns |
| Maximum CLK Fall Time | | $t_f$** | | - | - | 500 | ns |
| Output Rise Time of Iout | | $t_{or}$ | | - | 70 | 200 | ns |
| Output Fall Time of Iout | | $t_{of}$ | | - | 40 | 120 | ns |

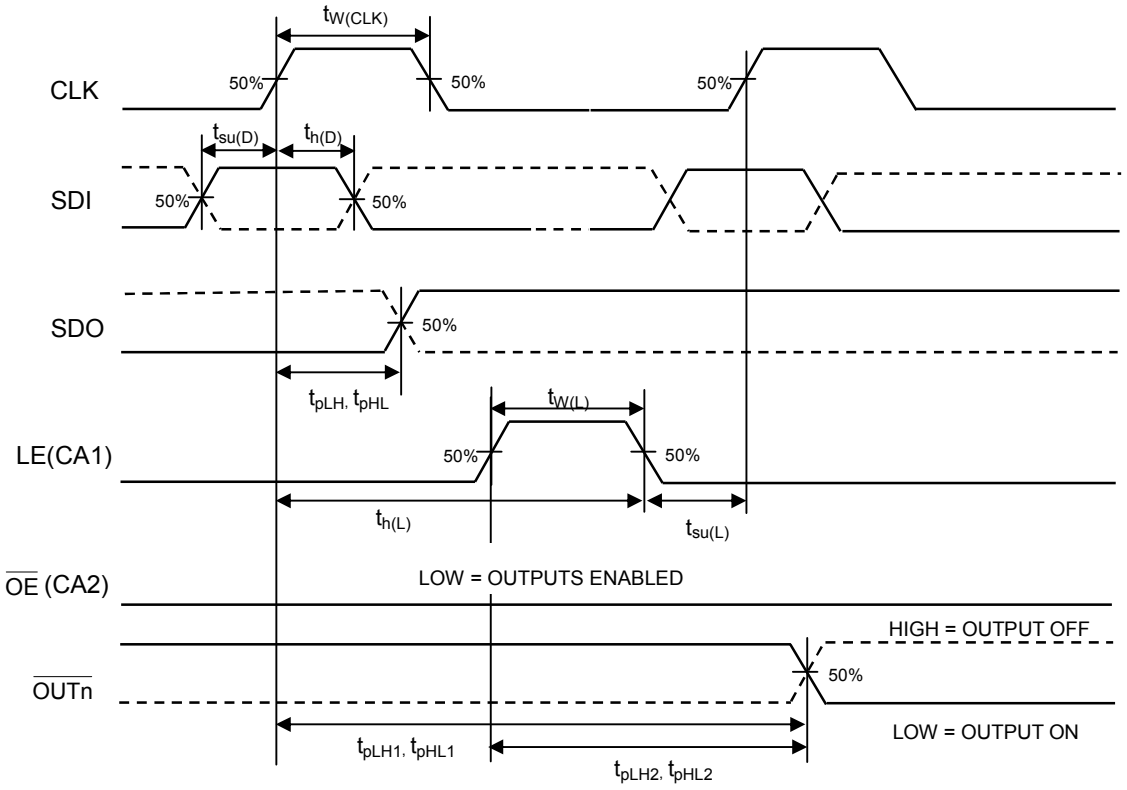
**If the devices are connected in cascade and $t_r$ or $t_f$ is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

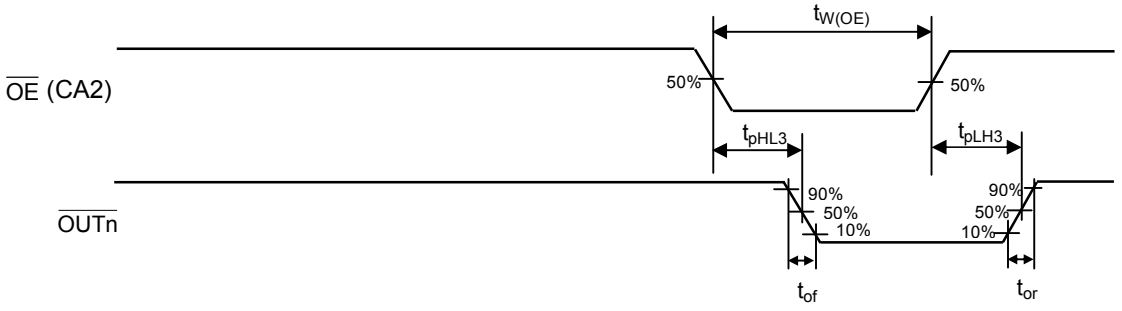
## Test Circuit for Switching Characteristics



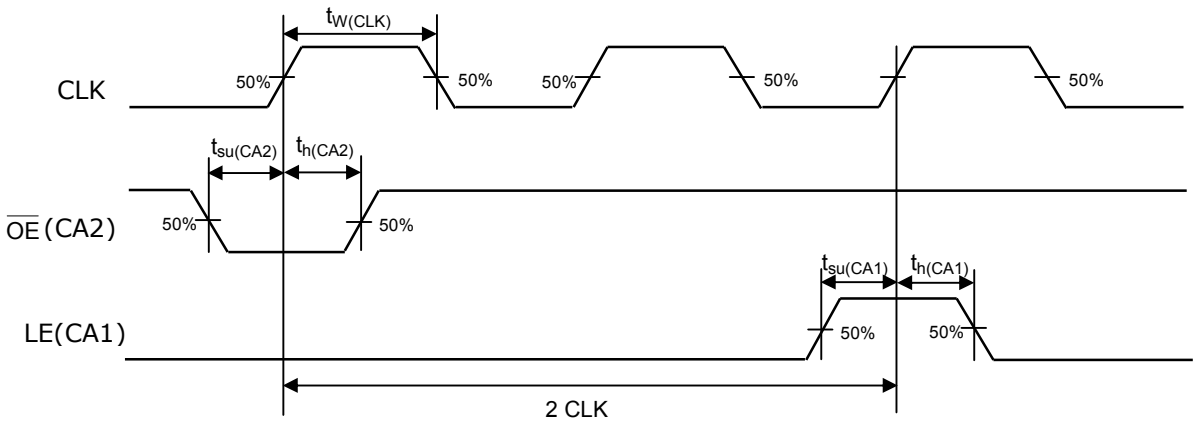
## Timing Waveform

### Normal Mode



## Entering Current Adjust Mode

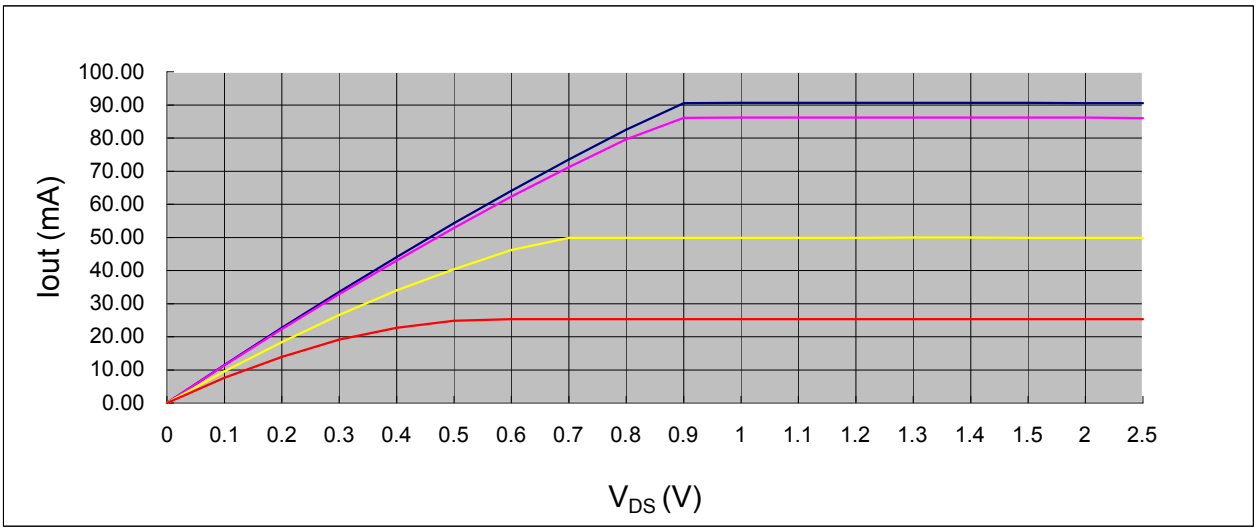


## Application Information

### Constant Current

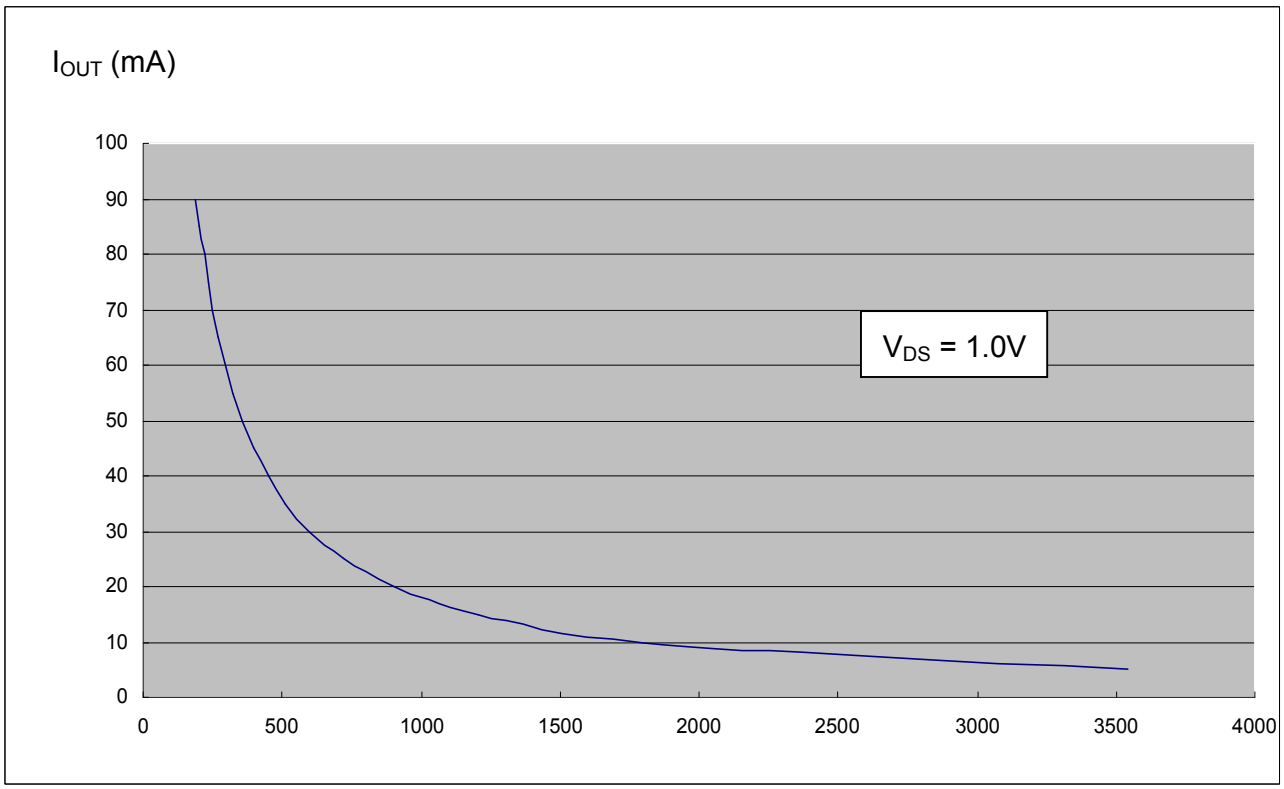
To design LED displays, MBI5028 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than ±3%, and that between ICs is less than ±6%.
2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (Vf). This performs as a perfection of load regulation.



## Adjusting Output Current

The output current of each channel ($I_{OUT}$) is set by an external resistor, $R_{ext}$. After a power-on status, the relationship between $I_{out}$ and $R_{ext}$ is shown in the following figure.




**Resistance of the external resistor, $R_{ext}$, in Ω**

Also, the output current in milliamps can be calculated from the equation:

$I_{OUT}$ is (625/ $R_{ext}$) x 14.4 x G, approximately,

where $R_{ext}$, in Ω, is the resistance of the external resistor connected to R-EXT terminal.

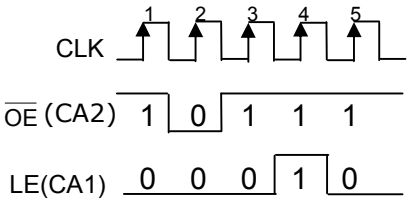
Conceptually, G is the digital current gain.

After a power-on status, the default value of G is 1.984.

Based on $I_{OUT}$ = (625/ $R_{ext}$) x 14.4 x G, thus, $I_{OUT}$ is (625/ $R_{ext}$) x 28.8

The magnitude of current is around 50mA at 360Ω and 25mA at 720Ω.

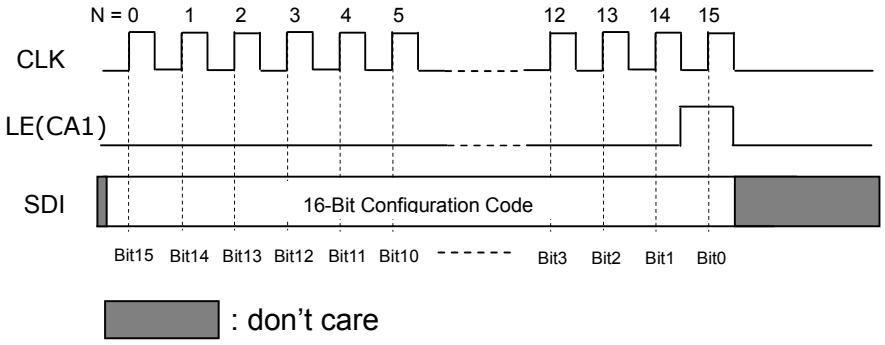
## Entering Current Adjust Mode




Each time the system controller sends the sequence patterns shown above, MBI5028 can enter the Current Adjust mode. During this phase, the system controller can still send data through SDI pin.

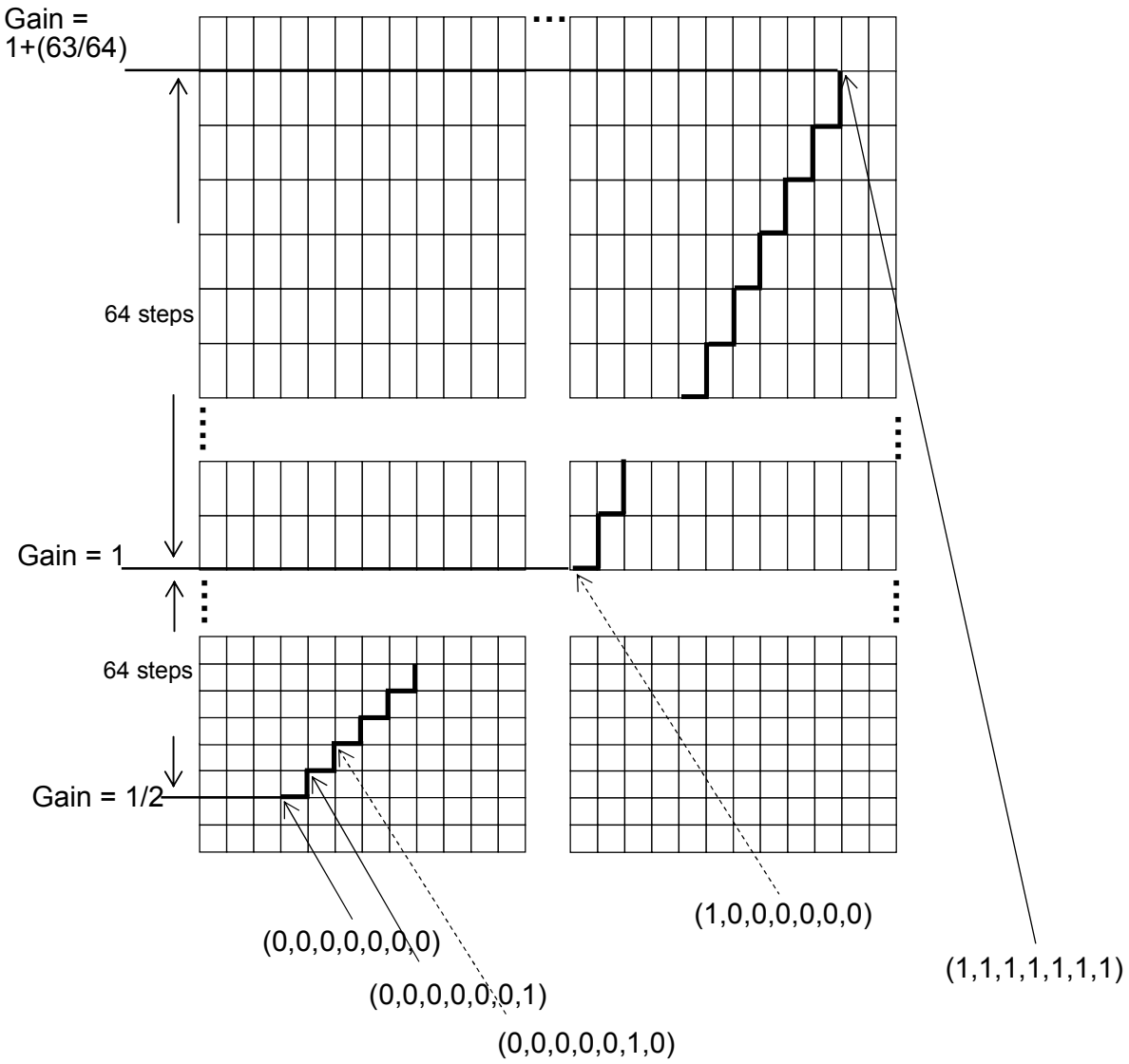
The state of $\overline{OE}$ (CA2) and LE(CA1) is sampled by the rising edge of each CLK. We use “0” and “1” to represent the state of “Voltage Low” and “Voltage High” respectively. The states of the successive five $\overline{OE}$ (CA2) and LE(CA1) are (1, 0), (0, 0), (1, 0), (1, 1) and (1, 0).

## Writing Configuration Code




After entering the Current Adjust mode, the system controller sends a 7-bit Current Adjust code to 16-bit Shift Register through MBI5028 SDI pin. Then sending LE(CA1) will transfer the contents in the Shift Register to a 16-bit Configuration Latch rather than the 16-bit Output Latch in a Normal mode. The 7-bit Current Adjust code in the Configuration Latch will directly affect the $I_O$ Regulator by a gain, G. The output current resulted by the gain values will be then defined as: (625/ $R_{ext}$) x 14.4 x G

## Current Gain




## 16-Bit Configuration Code

| | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 8 | Bit 9 | Bit 10 | Bit 11 | Bit 12 | Bit 13 | Bit 14 | Bit 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Meaning | - | HC | CC0 | CC1 | CC2 | CC3 | CC4 | CC5 | - | - | - | - | - | - | - | - |
| Default Value | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | - | - | - | - | - | - | - | - |

← 7-bit Current Adjust Code →

Binary Representation of the Current Adjust Code = {HC, CC〔0:5〕}
Gain, G = (1 + HC) x (1 + D/64)/2

where HC is 1 or 0 (HC=0 : Low current band; HC=1 : High current band) and

D = CC0 x $2^5$+ CC1 x $2^4$+ CC2 x $2^3$+ CC3 x $2^2$+ CC4 x $2^1$+ CC5 x $2^0$;

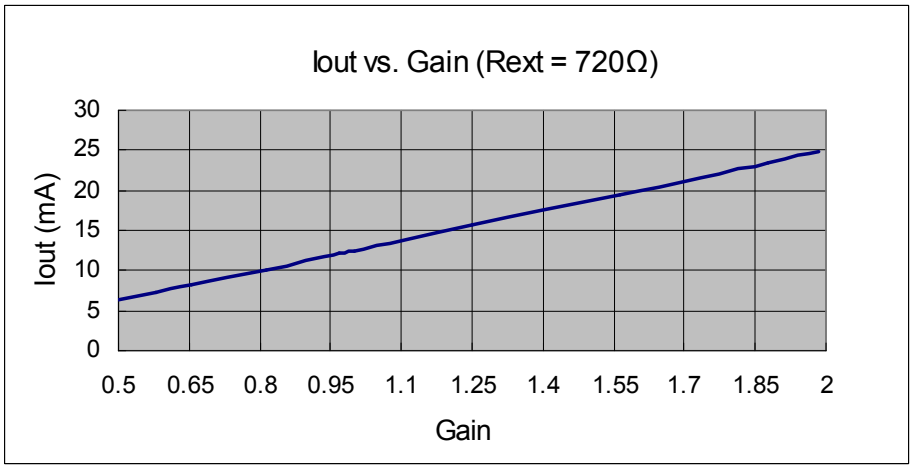
So, the Current Adjust Code is a floating number with one bit exponent HC and 6-bit mantissa.

For example,
when the Current Adjust Code is (1,1,1,1,1,1,1)
Gain, G = (1+1) x (1+ 63/64)/2 = 1.984

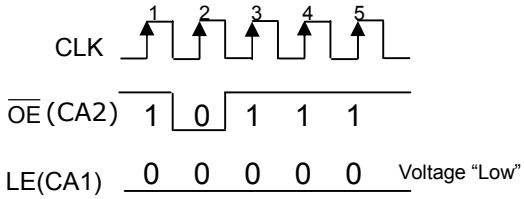
when the Current Adjust Code is (1,0,0,0,0,0,0)
Gain, G = (1+1) x (1+ 0/64)/2 = 1

when the Current Adjust Code is (0,0,0,0,0,0,0)
Gain, G = (1+0) x (1+ 0/64)/2 = 0.5

After power on, the default value of Current Adjust Code is (1,1,1,1,1,1,1). Thus, G is 1.984.
Typically, the output current resulted by the digital current gain, G, is shown as the figure below.




## Resuming to Normal Mode

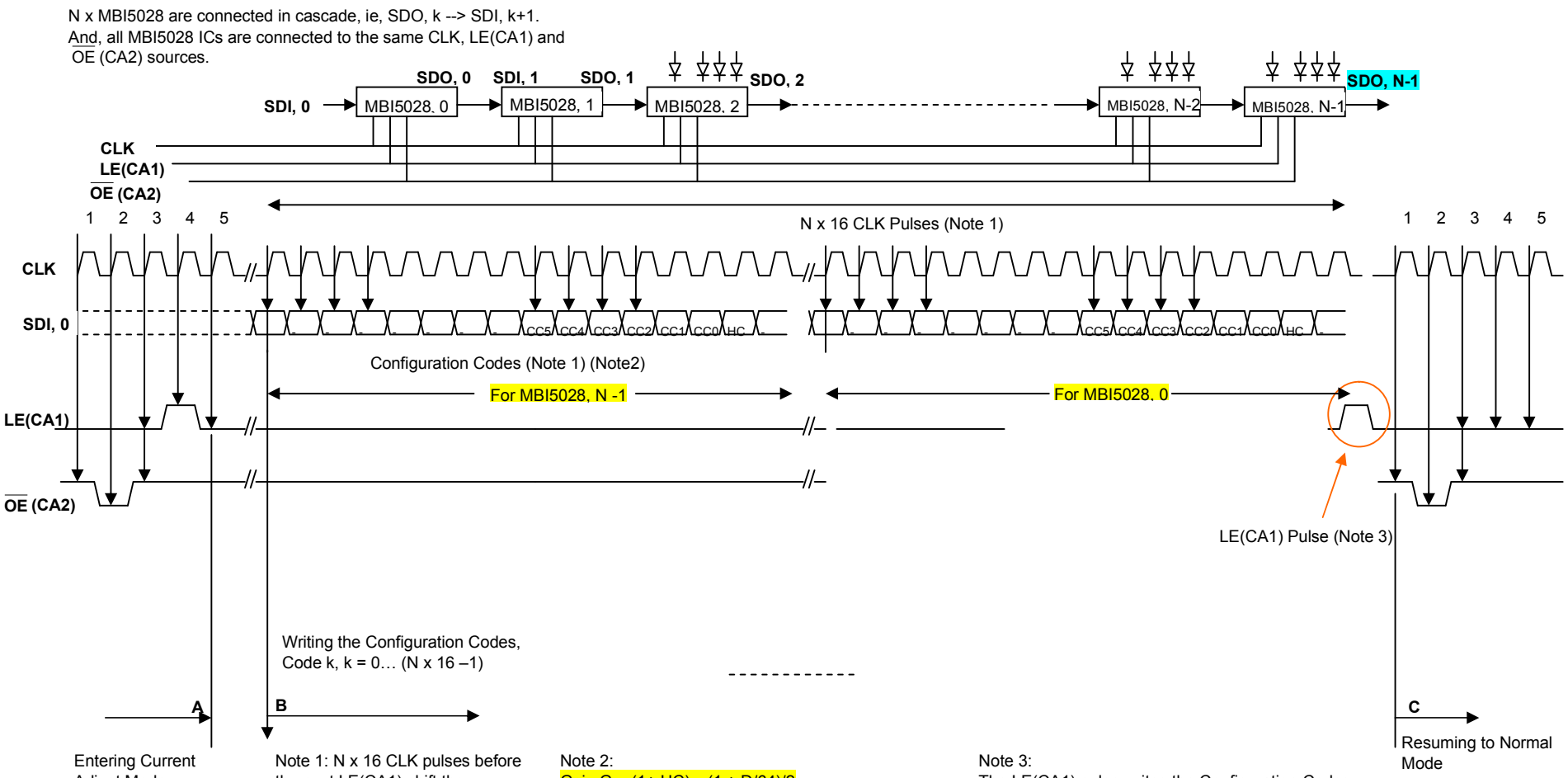



Each time the system controller sends the sequence patterns shown above, MBI5028 can resume to a Normal mode. During this phase, the system controller can still send data through SDI pin.

The state of $\overline{OE}$ (CA2) and LE(CA1) is sampled by the rising edge of each CLK. We use "0" and "1" to represent the state of "Voltage Low" and "Voltage High" respectively. The states of the successive five $\overline{OE}$ (CA2) and LE(CA1) are (1, 0), (0, 0), (1, 0), (1, 0) and (1, 0).

After resuming to the Normal mode, the Shift Register is again merely used for conveying the image data sent from the system controller. The gain will always be effective until power off or the Configuration Latch is re-written.

## Timing Chart for Current Adjust Mode (An Example)




Note 1: N x 16 CLK pulses before the next LE(CA1) shift the configuration codes. N 16-bit Configuration Codes are required, although only 7 bits are significant.

Note 2:
Gain G = (1+ HC) x (1 + D/64)/2
$D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$ .

Note 3:
The LE(CA1) pulse writes the Configuration Codes to each MBI5028.

## Package Power Dissipation ($P_D$)

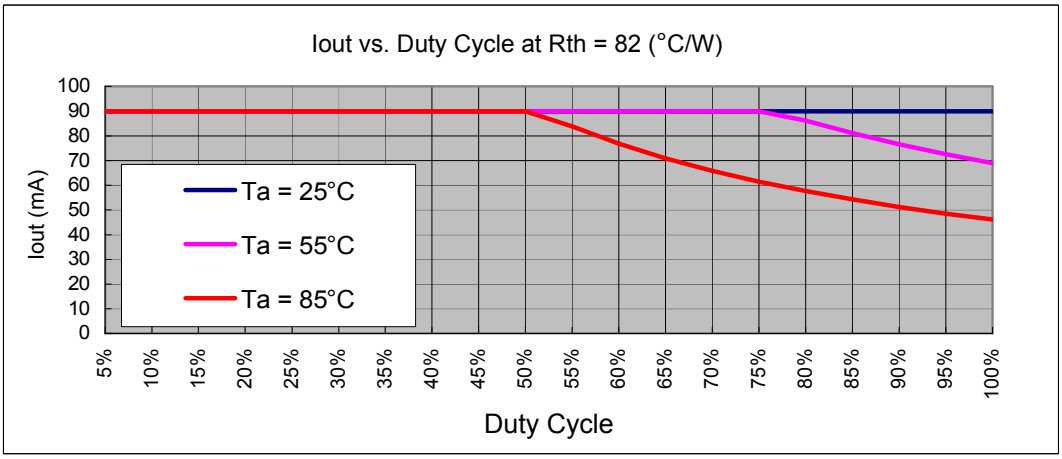
The maximum allowable package power dissipation is determined as $P_D(max) = (Tj – Ta) / R_{th(j-a)}$. When 16 channels are turned on simultaneously, the actual package power dissipation is $P_D(act) = (I_{DD} \times V_{DD}) + (I_{OUT} \times Duty \times V_{DS} \times 16)$. Therefore, to keep $P_D(act) \leq P_D(max)$, the allowable output current as a function of duty cycle is:

$I_{OUT} = \{ [ (Tj – Ta) / R_{th(j-a)} ] – (I_{DD} \times V_{DD}) \} / V_{DS} / Duty / 16,$

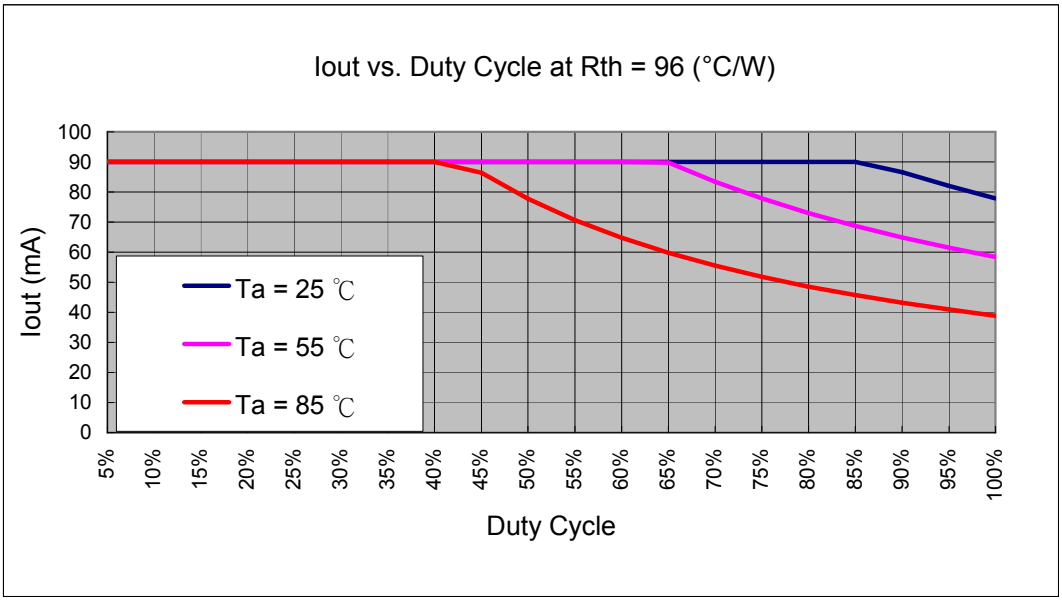
where Tj = 150°C.

### (A) $I_{out}$ = 90mA, $V_{DS}$ = 1.0V, 16 output channels active

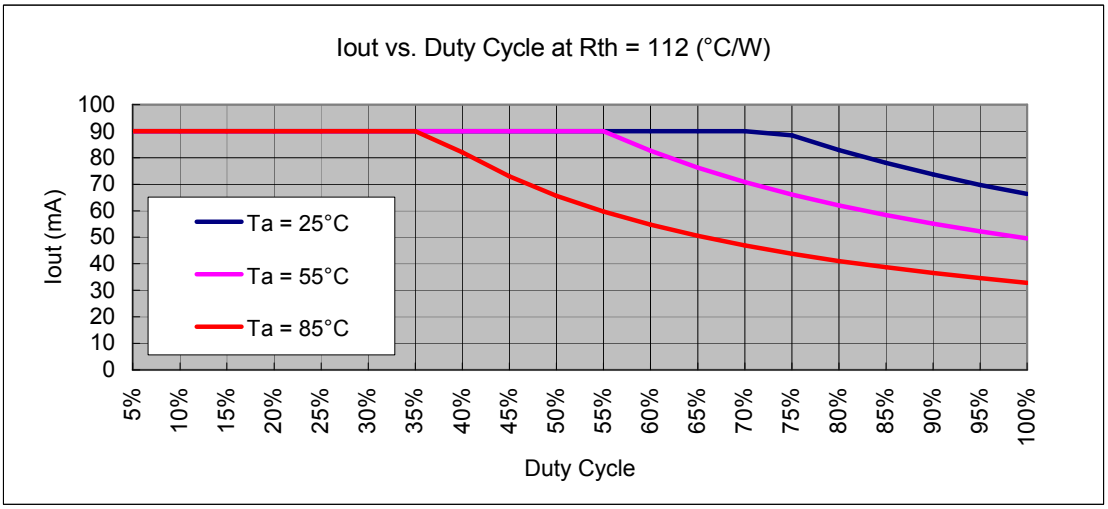
For CNS type package, the thermal resistance is $R_{th(j-a)}$ = 82 (°C/W)




For CF type package, the thermal resistance is $R_{th(j-a)}$ = 96 (°C/W)

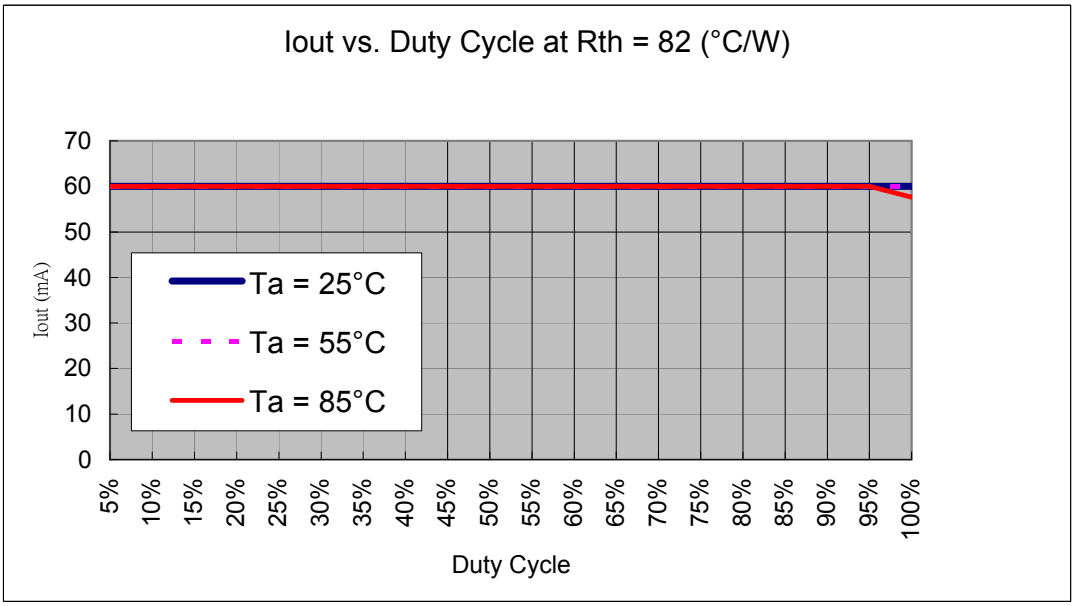


For CP type package, the thermal resistance is $R_{th(j-a)}$ = 112 (°C/W)

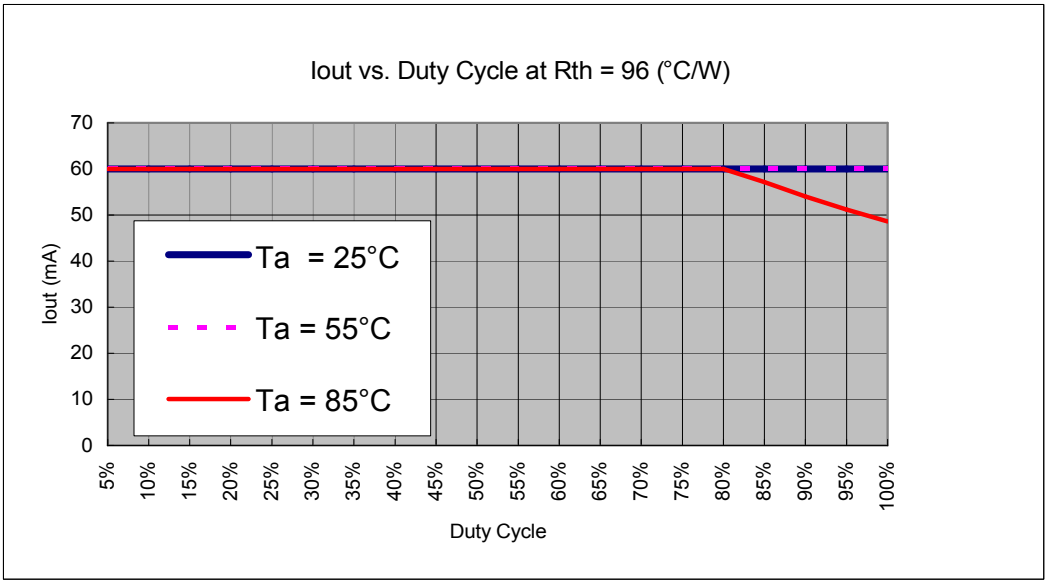



**(B) $I_{out}$ = 60mA, $V_{DS}$ = 0.8V, 16 output channels active**

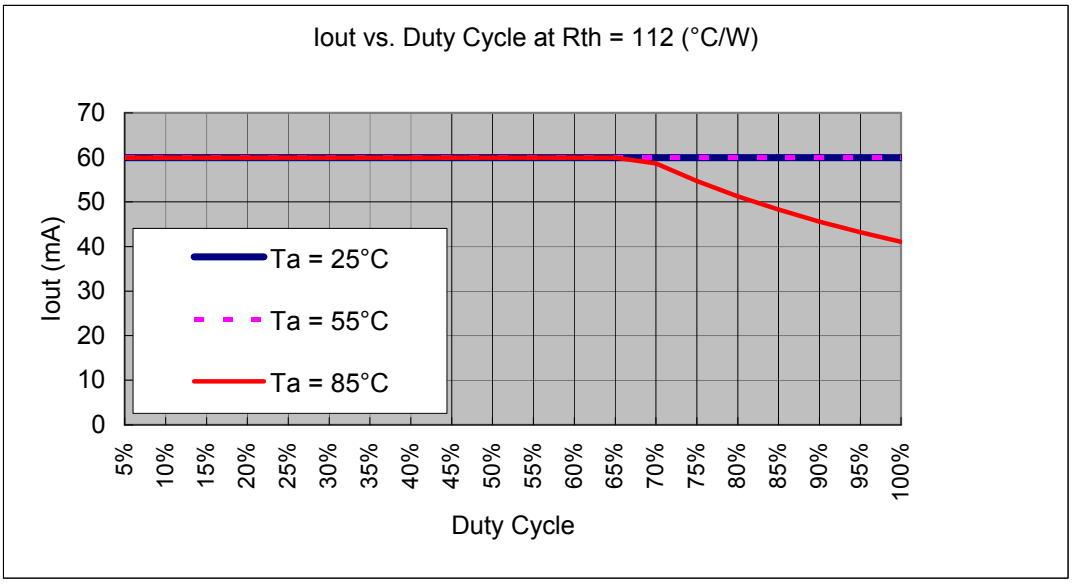
For CNS type package, the thermal resistance is $R_{th(j-a)}$ = 82 (°C/W)



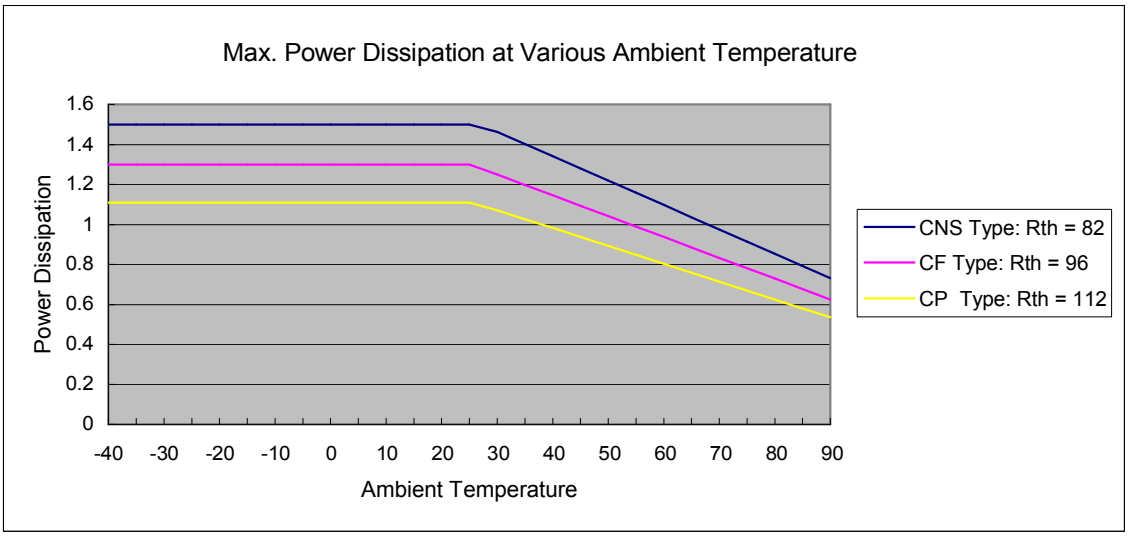
For CF type package, the thermal resistance is $R_{th(j-a)}$ = 96 (°C/W)




For CP type package, the thermal resistance is $R_{th(j-a)}$ = 112 (°C/W)



The maximum power dissipation, $P_D(max) = (Tj-Ta) / R_{th(j-a)}$ , decreases as the ambient temperature increases.

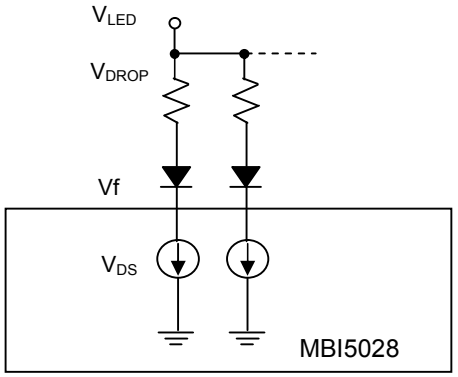


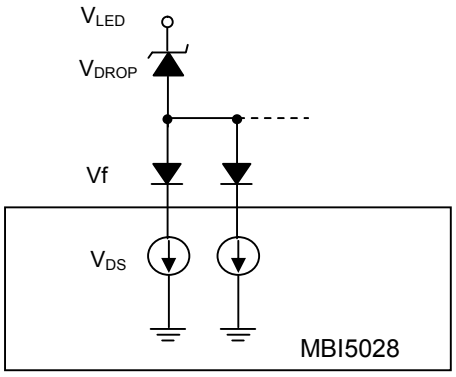

## Load Supply Voltage ($V_{LED}$)

MBI5028 are designed to operate with $V_{DS}$ ranging from 0.4V to 1.0V considering the package power dissipating limits. $V_{DS}$ may be higher enough to make $P_{D(act)} > P_{D(max)}$ when $V_{LED}$ = 5V and $V_{DS} = V_{LED} – Vf$, in which $V_{LED}$ is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer ($V_{DROP}$).

A voltage reducer lets $V_{DS} = (V_{LED} – Vf) – V_{DROP}$.

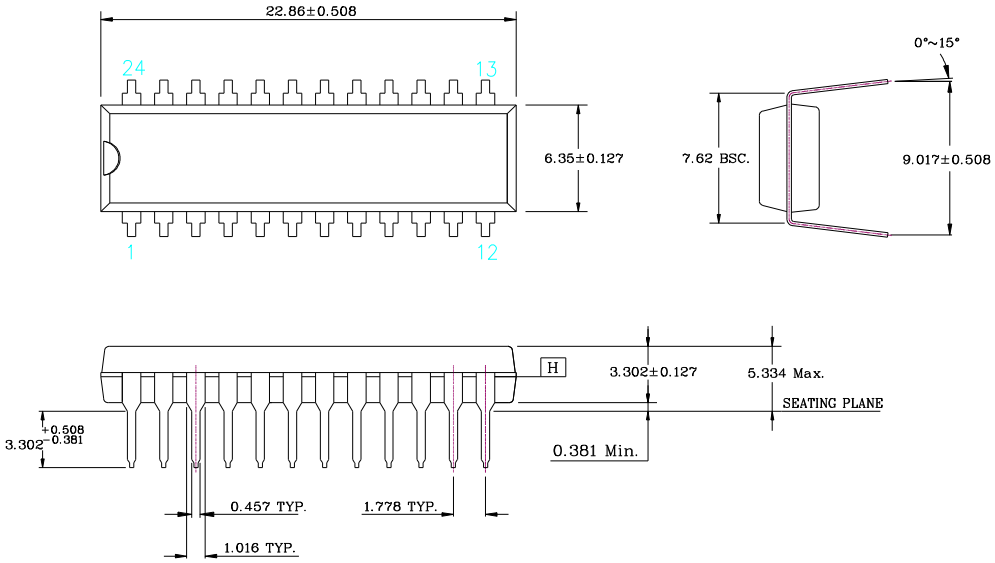
Resisters, or Zener diode can be used in the applications as the following figures.



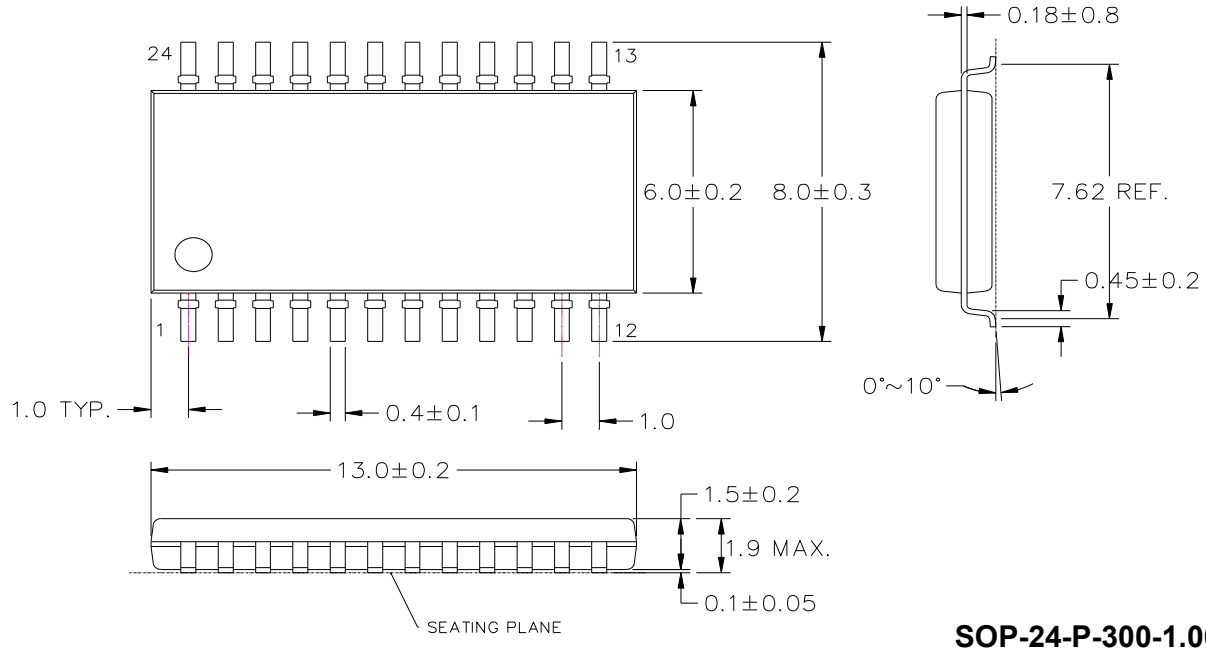
# Package Outlines

## MBI5028CNS Outline Drawing



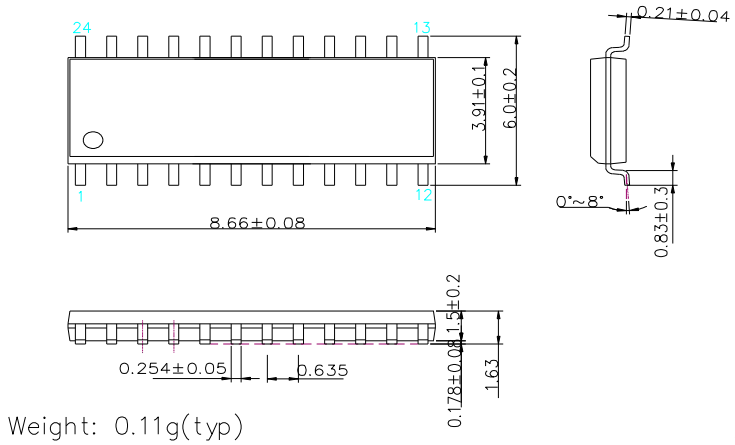

**SDIP-24-P-300-1.78**
**Units: mm**
**Weight: 1.11g (typ)**

## MBI5028CF Outline Drawing




**SOP-24-P-300-1.00**
**Units: mm**
**Weight: 0.28g (typ)**

## MBI5028CP Outline Drawing




Weight: 0.11g(typ)

**SSOP24-P-150-0.64**
**Units: mm**
**Weight: 0.11g (typ)**