4-Bit D Flip-Flop

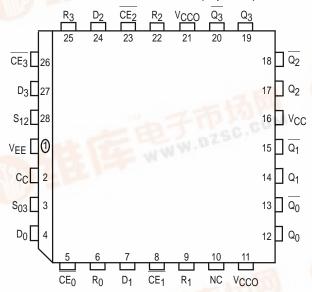
The MC10E/100E131 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable (C_E) inputs for clocking. Common clocking is achieved by holding the C_E inputs LOW and using C_C to clock all four flip-flops. In this case, the C_E inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both C_C and CE are LOW, and transfers to the slave when either C_C or CE (or both) go HIGH.

- 1100MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- Extended 100E VEE Range of 4.2V to 5.46V
- 75kΩ Input Pulldown Resistors

Pinout: 28-Lead PLCC (Top View)



* All VCC and VCCO pins are tied together on the die.

PIN NAMES

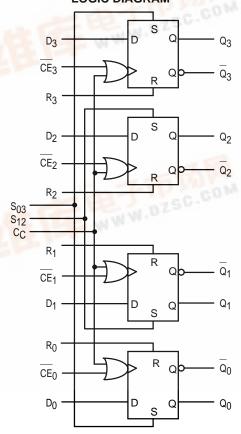
The second secon										
Pin	Function									
D ₀ - D ₃	Data Inputs									
D ₀ - D ₃ CE ₀ - CE ₃	Clock Enables (Individual)									
$R_0 - R_3$	Resets									
CC	Common Clock									
S ₀₃ , S ₁₂	Sets (paired)									
$Q_0 = Q_3$	True Outputs									
Q6 4 Q3 P	Inverting Outputs									

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4-BIT D FLIP-FLOP



LOGIC DIAGRAM



:dzsc.com

MC10E131 MC100E131

DC CHARACTERISTICS ($V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$)

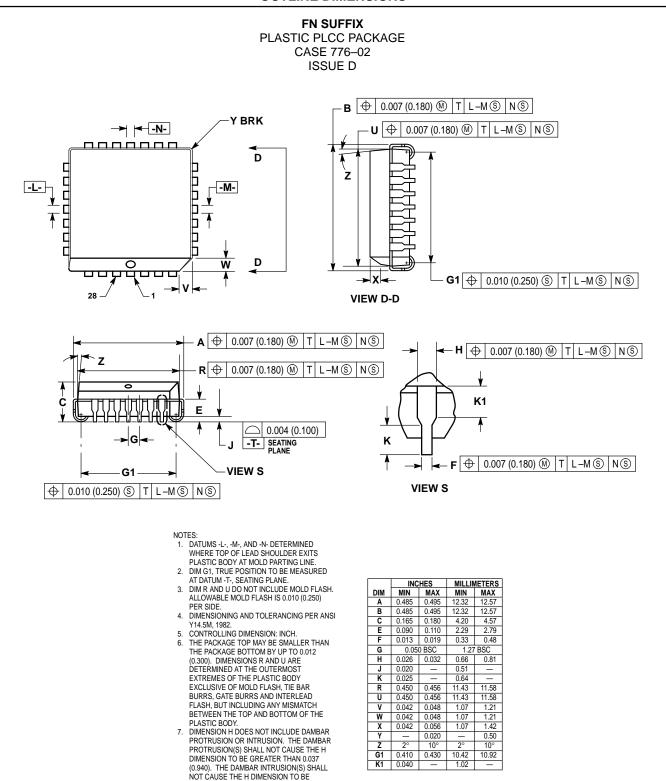
		–40°C		0°C		25°C			85°C						
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	Cond
lН	Input HIGH													μА	
	Current C _C			350			350			350			350	,	
	<u>_\$</u>			450			450			450			450		
	R, CE			300			300			300			300		
	D			150			150			150			150		
IEE	Power Supply													mA	
· -	Current 10E		58	70		58	70		58	70		58	70		
	100E		58	70		58	70		58	70		67	81		

$\textbf{AC CHARACTERISTICS} \; (\mathsf{V}_{EE} = \mathsf{V}_{EE}(\mathsf{min}) \; \mathsf{to} \; \mathsf{V}_{EE}(\mathsf{max}); \; \mathsf{V}_{CC} = \mathsf{V}_{CCO} = \mathsf{GND})$

			-40°C			O	°C to 85°0			
Symbol	Characteristic		Min	Тур	Max	Min	Тур	Max	Unit	Condition
fMAX	Maximum Toggle Frequency		1000	1400		1100	1400		MHz	
^t PLH ^t PHL	Propagation Delay to Output	CE CCR S	310 275 300 300	600 600 625 550	750 725 775 775	360 325 350 350	500 500 550 550	700 675 725 725	ps	
tS	Setup Time	D	200	20		150	20		ps	1
tH	Hold Time	D	225	-20		175	-20		ps	1
tRR	Reset Recovery Time		450	150		400	150		ps	
tpW	Minimum Pulse Width	CLK R, S	400 400			400 400			ps	
tSKEW	Within-Device Skew			60			60		ps	2
t _r /t _f	Rise/Fall Time	·	275	460	725	300	480	675	ps	20–80%

Setup/hold times guaranteed for both C_C and CE.
Within-device skew is defined as identical transitions on similar paths through a device.

OUTLINE DIMENSIONS



SMALLER THAN 0.025 (0.635).

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