

# Advance Information

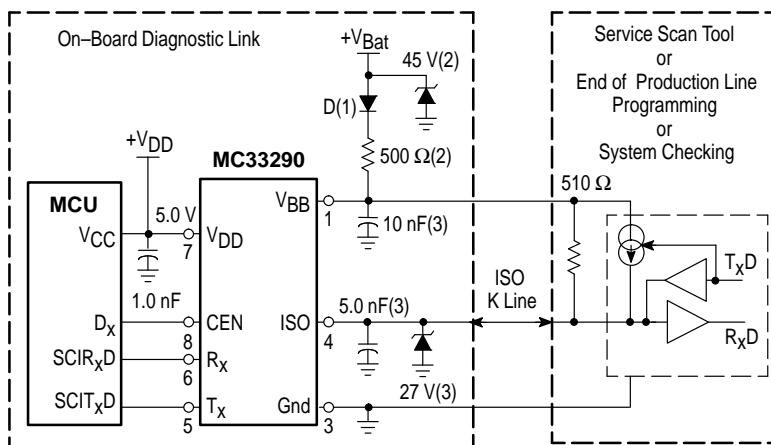
## ISO K Line Serial Link Interface

The MC33290 is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing in automotive diagnostic applications. It is designed to interface between the vehicle's on-board microcontroller and systems off-board the vehicle via the special ISO K line. The MC33290 is designed to meet the "Diagnostic Systems ISO9141" specification. The device's K line bus driver's output is fully protected against bus shorts and over temperature conditions.

The MC33290 derives its robustness to temperature and voltage extremes from being built on a SMARTMOS™ process, incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Though the MC33290 was principally designed for automotive applications, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  and  $8.0\text{ V} \leq V_{\text{BB}} \leq 18\text{ V}$  supply. The economical 8 pin DIP and SO-8 surface mount plastic packages make the MC33290 very cost effective.

- Designed to Operate Over Wide Supply Voltage of 8.0 to 18 V
- Ambient Operating Temperature of  $-40$  to  $125^{\circ}\text{C}$
- Interfaces Directly to Standard CMOS Microprocessors
- ISO K Line Pin Protected Against Shorts to Ground
- Thermal Shutdown with Hysteresis
- Maximum Transmission Speeds in Excess of 50 k Baud
- ISO K Line Pin Capable of High Currents
- ISO K Line can be Driven with up to 10 nF of Parasitic Capacitance
- 8.0 kV ESD Protection Attainable with Few Additional Components
- Standby Mode: No  $V_{\text{Bat}}$  Current Drain with  $V_{\text{DD}}$  at 5.0 V
- Low Current Drain during Operation with  $V_{\text{DD}}$  at 5.0 V

### Typical Application Schematic



Components Necessary for: Reverse Battery (1), Overvoltage Transient (2), and 8.0 kV ESD Protection (3) in a metal module case.

This device contains 85 active transistors.

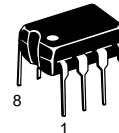
## MC33290

### ISO K LINE SERIAL LINK INTERFACE

#### SEMICONDUCTOR TECHNICAL DATA

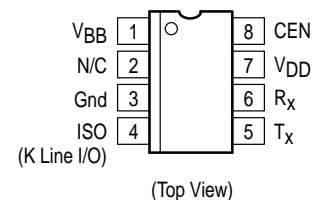


**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751  
(SO-8)



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626

### PIN CONNECTIONS

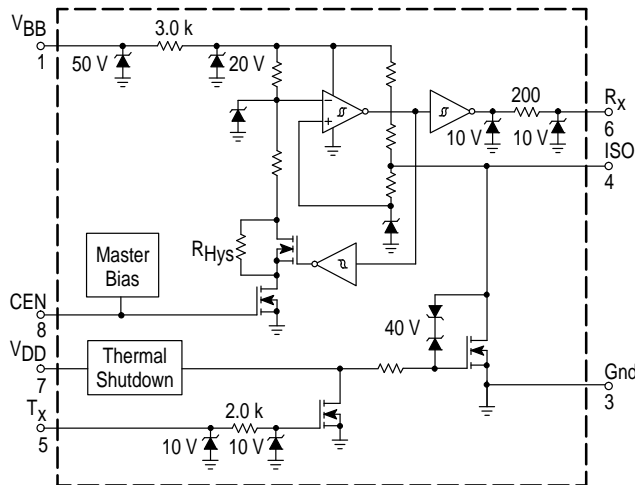


### ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33290D	$T_A = -40$ to $125^{\circ}\text{C}$	SO-8
MC33290P		DIP-8

# MC33290

Figure 1. Simplified Block Diagram



**MAXIMUM RATINGS** (All voltages are with respect to ground, unless otherwise noted.)

Rating	Symbol	Value	Unit
V <sub>DD</sub> DC Supply Voltage	V <sub>DD</sub>	-0.3 to 7.0	V
V <sub>BB</sub> Load Dump Peak Voltage	V <sub>BB(LD)</sub>	45	V
ISO Pin Load Dump Peak Voltage (Note 1)	V <sub>ISO</sub>	40	V
ISO Short Circuit Current Limit	I <sub>ISO(LIM)</sub>	1.0	A
ESD Voltage (Note 2)			V
Human Body Model (Note 3)	V <sub>ESD1</sub>	2000	
Machine Model (Note 4)	V <sub>ESD2</sub>	200	
ISO Clamp Energy (Note 5)	E <sub>clamp</sub>	10	mJ
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Operating Case Temperature	T <sub>C</sub>	-40 to +125	°C
Operating Junction Temperature	T <sub>J</sub>	-40 to +150	°C
Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>D</sub>	0.8	W
Lead Soldering Temperature (Note 6)	T <sub>solder</sub>	260	°C
Thermal Resistance (Junction-to-Ambient)	R <sub>θJA</sub>	150	°C/W

- NOTES:** 1. Device will survive double battery jump start conditions in typical applications for 10 minutes duration, but is not guaranteed to remain within specified parametric limits during this duration.  
 2. ESD data available upon request.  
 3. Testing in accordance with Human Body Model (C<sub>Zap</sub> = 100 pF, R<sub>Zap</sub> = 1500 Ω).  
 4. Testing in accordance with Machine Model (C<sub>Zap</sub> = 100 pF, R<sub>Zap</sub> = 0 Ω).  
 5. Non-repetitive clamping capability at 25°C.  
 6. Lead soldering temperature limit is for 10 seconds maximum duration; contact Motorola Sales Office for device immersion soldering time/temperature limits.

**ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions of 4.75 V ≤ V<sub>DD</sub> ≤ 5.25 V, 8.0 V ≤ V<sub>BB</sub> ≤ 18 V, -40°C ≤ T<sub>C</sub> ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>POWER AND CONTROL</b>					
V <sub>DD</sub> Sleep State Current (T <sub>X</sub> = 0.8 V <sub>DD</sub> , CEN = 0.3 V <sub>DD</sub> )	I <sub>DD(SS)</sub>	-	-	0.1	mA
V <sub>DD</sub> Quiescent Operating Current (T <sub>X</sub> = 0.2 V <sub>DD</sub> , CEN = 0.7 V <sub>DD</sub> )	I <sub>DD(Q)</sub>	-	-	1.0	mA
V <sub>BB</sub> Sleep State Current (V <sub>BB</sub> = 16 V, T <sub>X</sub> = 0.8 V <sub>DD</sub> , CEN = 0.3 V <sub>DD</sub> )	I <sub>BB(SS)</sub>	-	-	50	μA

- NOTES:** 1. When I<sub>BB</sub> transitions to >100 μA.  
 2. When I<sub>BB</sub> transitions to <100 μA.  
 3. Enable pin has an internal current pull-down equivalent to greater than 50 kΩ.  
 4. Measured by ramping T<sub>X</sub> down from 0.7 V<sub>DD</sub> and noting T<sub>X</sub> value at which ISO falls below 0.2 V<sub>BB</sub>.  
 5. Measured by ramping T<sub>X</sub> up from 0.3 V<sub>DD</sub> and noting the value at which ISO rises above 0.9 V<sub>BB</sub>.  
 6. T<sub>X</sub> pin has internal current pull-up equivalent to greater than 50 kΩ. Pull-Up current measured with T<sub>X</sub> pin at 0.7 V<sub>DD</sub>.  
 7. Thermal Shutdown performance (T<sub>LIM</sub>) is guaranteed by design but not production tested.

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**ELECTRICAL CHARACTERISTICS (continued)** (Characteristics noted under conditions of  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ,  $8.0\text{ V} \leq V_{BB} \leq 18\text{ V}$ ,  $-40^\circ\text{C} \leq T_C \leq 125^\circ\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>POWER AND CONTROL</b>					
$V_{BB}$ Quiescent Operating Current ( $T_X = 0.2 V_{DD}$ , $CEN = 0.7 V_{DD}$ )	$I_{BB(Q)}$	–	–	1.0	mA
Chip Enable					V
Input High Voltage Threshold (Note 1)	$V_{IH(CEN)}$	$0.7 V_{DD}$	–	–	
Input Low Voltage Threshold (Note 2)	$V_{IL(CEN)}$	–	–	$0.3 V_{DD}$	
Chip Enable Pull-Down Current (Note 3)	$I_{PD(CEN)}$	2.0	–	40	$\mu\text{A}$
$T_X$ Input Low Voltage Threshold ( $R_{ISO} = 510\ \Omega$ ) (Note 4)	$V_{IL(T_X)}$	–	–	$0.3 \times V_{DD}$	V
$T_X$ Input High Voltage Threshold ( $R_{ISO} = 510\ \Omega$ ) (Note 5)	$V_{IH(T_X)}$	$0.7 \times V_{DD}$	–	–	V
$T_X$ Pull-Up Current (Note 6)	$I_{PU(T_X)}$	–40	–	–2.0	$\mu\text{A}$
$R_X$ Output Low Voltage Threshold ( $R_{ISO} = 510\ \Omega$ , $T_X = 0.2 V_{DD}$ , $R_X$ Sinking 1.0 mA)	$V_{OL(R_X)}$	–	–	$0.2 V_{DD}$	V
$R_X$ Output High Voltage Threshold ( $R_{ISO} = 510\ \Omega$ , $T_X = 0.8 V_{DD}$ , $R_X$ Sourcing 250 $\mu\text{A}$ )	$V_{OH(R_X)}$	$0.8 V_{DD}$	–	–	V
Thermal Shutdown (Note 7)	$T_{LIM}$	150	170	–	$^\circ\text{C}$

- NOTES:**
1. When  $I_{BB}$  transitions to  $>100\ \mu\text{A}$ .
  2. When  $I_{BB}$  transitions to  $<100\ \mu\text{A}$ .
  3. Enable pin has an internal current pull-down equivalent to greater than  $50\ \text{k}\Omega$ .
  4. Measured by ramping  $T_X$  down from  $0.7 V_{DD}$  and noting  $T_X$  value at which ISO falls below  $0.2 V_{BB}$ .
  5. Measured by ramping  $T_X$  up from  $0.3 V_{DD}$  and noting the value at which ISO rises above  $0.9 V_{BB}$ .
  6.  $T_X$  pin has internal current pull-up equivalent to greater than  $50\ \text{k}\Omega$ . Pull-Up current measured with  $T_X$  pin at  $0.7 V_{DD}$ .
  7. Thermal Shutdown performance ( $T_{LIM}$ ) is guaranteed by design but not production tested.

**ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions of  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ,  $8.0\text{ V} \leq V_{BB} \leq 18.0\text{ V}$ ,  $-40^\circ\text{C} \leq T_C \leq 125^\circ\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ISO I/O</b>					
Input Low Voltage Threshold ( $R_{ISO} = 0\ \Omega$ , $T_X = 0.8 V_{DD}$ ) (Note 1)	$V_{IL(ISO)}$	–	–	$0.4 \times V_{BB}$	V
Input High Voltage Threshold ( $R_{ISO} = 0\ \Omega$ , $T_X = 0.8 V_{DD}$ ) (Note 2)	$V_{IH(ISO)}$	$0.7 \times V_{BB}$	–	–	V
Input Hysteresis (Note 3)	$V_{Hys(ISO)}$	$0.05 \times V_{BB}$	–	$0.1 \times V_{BB}$	V
Internal Pull-Up Current (Note 4) ( $R_{ISO} = \infty\ \Omega$ , $T_X = 0.8 V_{DD}$ , $V_{ISO} = 0.5 V_{BB}$ )	$I_{PU(ISO)}$	10	–	60	$\mu\text{A}$
Short Circuit Current Limit (Note 5) ( $R_{ISO} = 0\ \Omega$ , $T_X = 0.4 V_{DD}$ , $V_{ISO} = V_{BB}$ )	$I_{SC(ISO)}$	50	–	1000	mA
Output Low Voltage ( $R_{ISO} = 510\ \Omega$ , $T_X = 0.2 V_{DD}$ )	$V_{OL(ISO)}$	–	–	$0.1 \times V_{BB}$	V
Output High Voltage ( $R_{ISO} = \infty\ \Omega$ , $T_X = 0.8 V_{DD}$ )	$V_{OH(ISO)}$	$0.95 \times V_{BB}$	–	–	V
Fall Time (Note 6) ( $R_{ISO} = 510\ \Omega$ to $V_{BB}$ , $C_{ISO} = 10\ \text{nF}$ to Ground)	$t_{fall(ISO)}$	–	–	2.0	$\mu\text{s}$
ISO Propagation Delay (Note 7)	$t_{PD(ISO)}$				$\mu\text{s}$
High to Low; ( $R_{ISO} = 510\ \Omega$ , $C_{ISO} = 500\ \text{pF}$ ) (Note 8)		–	–	2.0	
Low to High; ( $R_{ISO} = 510\ \Omega$ , $C_{ISO} = 500\ \text{pF}$ ) (Note 9)		–	–	2.0	

- NOTES:**
1. ISO ramped from  $0.8 V_{BB}$  to  $0.4 V_{BB}$ . Monitor  $R_X$ . Value of ISO voltage at which  $R_X$  transitions to  $0.3 V_{DD}$ .
  2. ISO ramped from  $0.4 V_{BB}$  to  $0.8 V_{BB}$ . Monitor  $R_X$ . Value of ISO voltage at which  $R_X$  transitions to  $0.7 V_{DD}$ .
  3. Input Hysteresis,  $V_{Hys(ISO)} = V_{IH(ISO)} - V_{IL(ISO)}$ .
  4. ISO Pull-Up has  $>100\ \text{k}\Omega$  internal pull-up to  $V_{BB}$ .
  5. ISO has internal current limiting.
  6. Time required ISO voltage to transition from  $0.8 V_{BB}$  to  $0.2 V_{BB}$ .
  7. Changes in the value of  $C_{ISO}$  affect the rise and fall time but have minimal effect on Propagation Delay.
  8. Step  $T_X$  voltage from  $0.2 V_{DD}$  to  $0.8 V_{DD}$ ; Time measured from  $V_{IH(ISO)}$  until  $V_{ISO}$  reaches  $0.3 V_{BB}$ .
  9. Step  $T_X$  voltage from  $0.8 V_{DD}$  to  $0.2 V_{DD}$ ; Time measured from  $V_{IL(ISO)}$  until  $V_{ISO}$  reaches  $0.7 V_{BB}$ .

Figure 2. ISO Input Threshold/ $V_{BB}$  versus Temperature

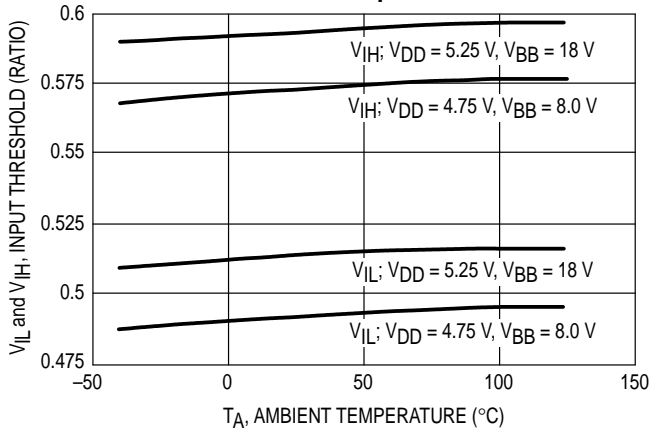


Figure 3. ISO Output/ $V_{BB}$  versus Temperature

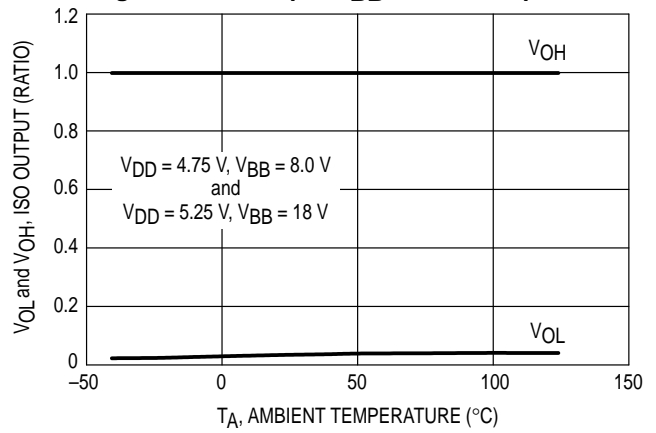


Figure 4. ISO Fall Time versus Temperature

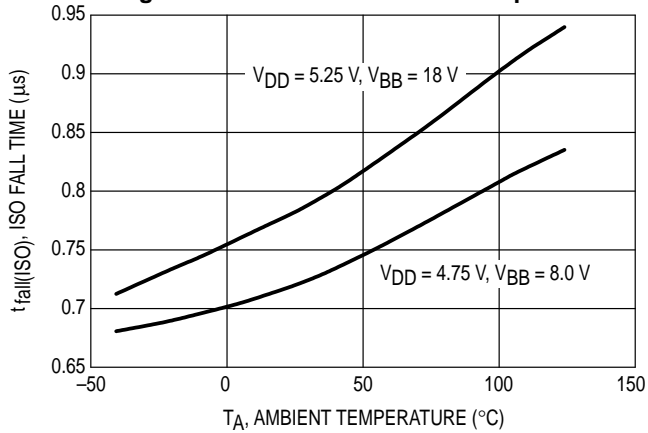
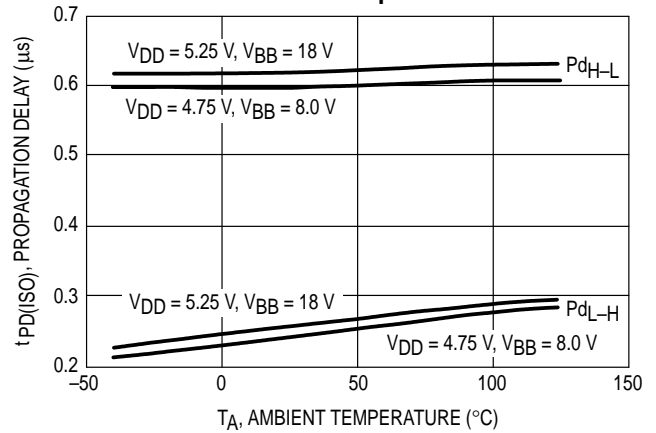


Figure 5. ISO Propagation Delay versus Temperature



# MC33290

## APPLICATIONS INFORMATION

### Introduction

The MC33290 is a serial link bus interface device conforming to the ISO-9141 physical bus specification. The device was designed for automotive environment usage's compliant with On-Board Diagnostic (OBD) requirements set forth by the California Air Resources Board (CARB) using the ISO K line; The device does not incorporate an ISO L line. It provides bi-directional half-duplex communications interfacing from a microcontroller to the communication bus. The MC33290 incorporates circuitry to interface the digital translations from 5.0 V microcontroller logic levels to battery level logic and from battery level logic to 5.0 V logic levels. The MC33290 is built using Motorola's SMARTMOS™ process and is packaged in both an 8 pin plastic DIP and an 8 pin plastic SOIC.

### Functional Description

The MC33290 transforms 5.0 V microcontroller logic signals to battery level logic signals and visa-versa. This serial link interface device, operating in a typical automotive diagnostic application, operates at bit rates up to 10.4 Kbits/s with less than 2.0  $\mu$ s propagation delay and less than 2.0  $\mu$ s fall time. Rise time is a function of the resistor used in the application to pull-up the bus up to battery voltage, working in conjunction with the total capacitance present on the bus. The serial link interface will remain fully functional over a battery voltage range of 6.0 to 18 V. The device is parametrically specified over a dynamic  $V_{BB}$  voltage range of 8.0 to 18 V.

Required input levels from the microcontroller are ratio-metric with the  $V_{DD}$  voltage; normally used to power the

microcontroller. This enhances the MC33290's ability to remain in harmony with the  $R_X$  and  $T_X$  control input signals of the microcontroller. The  $R_X$  and  $T_X$  control inputs are compatible with standard 5.0 V CMOS circuitry. For fault tolerant purposes; the  $T_X$  input from the microcontroller has an internal passive pull-up to  $V_{DD}$  of approximately 125 k $\Omega$  while the CEN input has an internal passive pull-down to ground of approximately 125 k $\Omega$ .

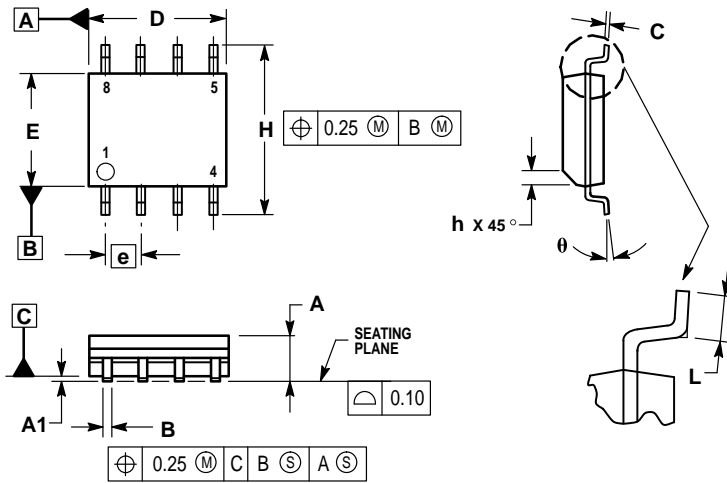
In the receive mode; All ISO K Line bus input signals greater than the  $0.7 \times V_{BB}$  thresholds are valid for a high level signal and less than the  $0.4 \times V_{BB}$  thresholds for a low level signal. In the transmit mode; Valid ISO K line bus output signal levels are greater than  $0.95 \times V_{BB}$  and less than  $0.1 \times V_{BB}$ . A pull-up resistor of  $\geq 100$  k $\Omega$  to battery is internally provided as well as an active data pull-down. The internal active pull-down is current limit protected against shorts to battery and further protected by thermal shutdown. Typical applications have reverse battery protection by the incorporation of an external 510  $\Omega$  pull-up resistor and diode to battery.

Reverse battery protection of the device is provided for in the Typical Application Schematic by using a reverse batter blocking diode (D). Battery line transient protection of the device is provided for by using a 45 V zener and a 500  $\Omega$  resistor connected to the  $V_{BB}$  source as shown in the same schematic. Device ESD protection from the communication lines exiting the module is through the use of the 10 nF connected to the  $V_{BB}$  device pin and the 5.0 nF used in conjunction with the 27 V zener connected to the ISO pin.

# MC33290

## OUTLINE DIMENSIONS

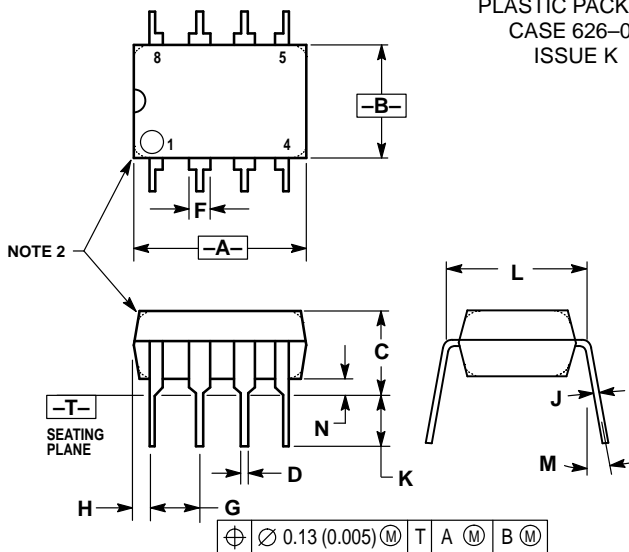
### D SUFFIX PLASTIC PACKAGE CASE 751-06 ISSUE T (SO-8)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. DIMENSIONS ARE IN MILLIMETER.
  3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.


DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

### P SUFFIX PLASTIC PACKAGE CASE 626-05 ISSUE K



- NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
  3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—		10°	
N	0.76	1.01	0.030	0.040

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