Advance Information

System Basis Chip with Low Speed Fault Tolerant CAN

MC33389

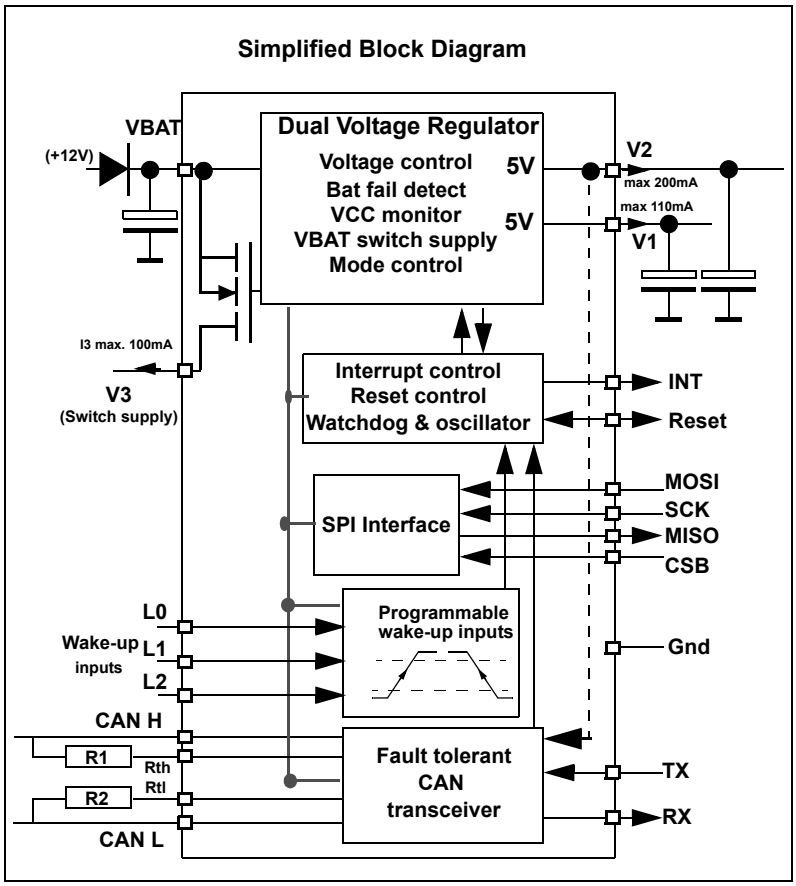
AUTOMOTIVE SBC
SYSTEM BASIS CHIP

SILICON MONOLITHIC
INTEGRATED CIRCUIT

The MC33389 is a monolithic integrated circuit combining many functions frequently used by automotive ECUs. It incorporates a low speed fault tolerant CAN transceiver.

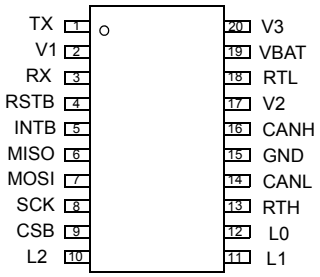
- Dual Low Drop Voltage Regulators, with Respectively 100mA and 200mA Current Capabilities, Current Limitation and Over Temperature Detection with Prewarning
- 5V Output Voltage for V1 Regulator
- Three Operational Modes (Normal, Standby and Sleep Mode) Separated from the CAN Interface Operating Modes
- Low Speed 125kBaud Fault Tolerant CAN Interface, Compatible with MC33388 Standalone Physical Interface
- V1 Regulator Monitoring and Reset Function
- Three External High Voltage Wake-up Inputs, Associated with V3 V_{bat} Switch
- 100mA Output Current Capability for V3 V_{bat} Switch Allowing Drive of External Switches or Relays
- Low Standby and Sleep Current Consumption
- V_{bat} Monitoring and V_{bat} Failure Detection Capabilities
- DC Operating Voltage up to 27V
- 40V Maximum Transient Voltage
- Programmable Software Window Watchog and Reset
- Wake up Capabilities (CAN Interface, Local Programmable Cyclic Wake up)
- Interface with MCU through SPI
- Programmable Interupt Function

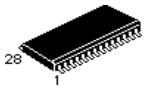
Simplified Block Diagram



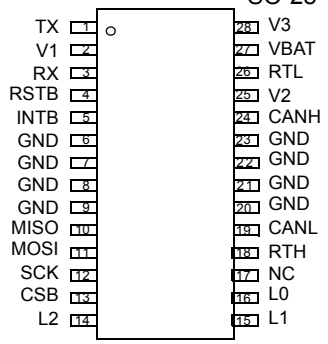
PIN CONNECTIONS

DH SUFFIX
POWER PACKAGE
CASE 979C
HSOP-20





DW SUFFIX
PLASTIC PACKAGE
CASE 751F
SO-28



ORDERING INFORMATION

Device and version	Operating Temperature Range	Package
MC33389ADW (1)	T_A = -40 to 125°C	SO-28
MC33389ADH (1)	T_A = -40 to 125°C	HSOP20
MC33389CDW (2)	T_A = -40 to 125°C	SO-28
MC33389CDH (2)	T_A = -40 to 125°C	HSOP20
MC33389DDW (3)	T_A = -40 to 125°C	SO-28

(1) Version A: If device remains in reset greater than 100ms due to V1 undervoltage, device switches to sleep mode to minimise current consumption. Wake-up configuration active.

(2) Version C: In V1 undervoltage condition, device remains in permanent reset state until V1 returns to nominal conditions. V1 protected by overcurrent and over temperature functions.

(3) Version D: In V1 undervoltage condition, device remains in permanent reset state until V1 returns to nominal conditions. V1 protected by overcurrent and over temperature functions. Change of undervoltage reset threshold. Refer to electrical parameter table, V1 PIn 5V.

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MOTOROLA intelligence everywhere™ digital dna™

MAXIMUM RATINGS

Description	Symbol	Min	Typ	Max	Unit	Test Conditions
DC Voltage at Pin V_{bat}	V_{bat}	-0.3		27	V	
Transient Voltage at Pin V_{bat}				40	V	t<500ms (Load Dump)
DC Voltage at Pins CANH CANL		-20		27	V	
Transient Voltage at Pins CANH CANL		-40		40	V	0<V2<5.5, V_{bat}>0, t<500ms
Coupled Transient Voltage at Pins CANH CANL		-100		100	V	With 100Ω Termination Resistors. Coupled Through 1nF (note1)
DC Voltage at Pins V1 V2		-0.3		6	V	
DC Current at output pins: RX, MISO, RSTB, INTB		-20		20	mA	
DC Voltage at input pins TX, MOSI, SCLK, CSB, RSTB		-0.3		6	V	
DC Voltage at Pins L0, L1, L2		-0.3		40	V	0<V_{bat}<40V
Current at Pins L0, L1, L2		-15			mA	
Transient Current at Pin V3		-30		20	mA	
DC Voltage at Pins RTH, RTL		-0.3		40	V	
ESD Voltage on any Pin (HBM 100pF, 1.5K)		-2		2	kV	
ESD Voltage on L0, L1, L2, CANH, CANL, V_{bat}		-2		2	kV	
ESD Voltage on any Pin (MM 200pF, 0Ω).		-150		150	V	
Junction Temperature	T_j	-40		150	°C	
Junction Temperature	T_{jt}	-40		160	°C	
Storage Temperature	T_s	-65		150	°C	
RTH, RTL Termination Resistance		500		16k	Ω	
Junction to Heatsink Thermal Resistance for HSOP20			3.1		K/W	33% Power on V1, 66% on V2 (Including CAN), Note 2
Junction to Pin Thermal Resistance for SO28WB			17		K/W	Note 2, Note 3

NOTE 1: Pulses 1, 2, 3a, 3b according to ISO7637.
NOTE 2: Refer to thermal management in device description section.
NOTE 3: pins 6,7,8,9,20,21,22,23 of SO28WB package

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ELECTRICAL PARAMETERS V_{bat}=5.5V to 18V, -40°< Tj < 150°C, unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{bat} PIN						
Nominal Vbat Operating Range		5.5		18	V	
Functional Vbat Operating Range		5.5		27	V	
Vbat Threshold for BatFail Flag	BatFail	2		4	V	0<V1<5,1V
Delay for Signalling BatFail	T_{fail}		150	400	µs	V_{bat}<BatFail, measured from Vbat low to INT active
Overvoltage Vbat Threshold	BAThigh	18	20	22	V	
Delay for Setting BAThigh Flag	T_{high}	4	18	50	µs	V_{bat}>BatHigh
Supply Current in Sleep Mode	I_{sleep1}		75	125	µA	Forced Wake-up and Cyclic Sense Disabled V_{bat}=12V,Tj = 25°C to150°C
Supply Current in Sleep Mode	I_{sleep2}			210	µA	Forced Wake-up and Cyclic Sense Disabled V_{bat}=12V, Tj = -40°C to 25°C
Supply current in sleep mode	I_{sleep3}		105	155	µA	Forced Wake-up or Cyclic Sense Enabled. V_{bat}=12V, Tj = 25°C to 150°C
Supply Current in Sleep Mode	I_{sleep4}			250		Forced Wake-up or Cyclic Sense Enabled V_{bat}12V, Tj -40 to 25°C,
Supply Current in Sleep Mode	I_{sleep5}			300		Forced Wake-up or Cyclic Sense Enabled. V_{bat} 6V to 16V, Tj -40 to 150°C
Supply Current in Standby Mode	I_{stb2}		0.5	1	mA	
Supply Current in Normal Mode	I_{nrec}		3.5	7	mA	Normal Mode with I(V1)=I(V2)=0 Bus in Recessive State
V1 PIN 5V						
Output Voltage	$V1_{nom}$	4.85	5	5.15	V	0mA<I_{out}<100mA 5.5V<V_{bat}<27V
Output Voltage	V1	4.8	5	5.2	V	I_{out}=<100mA 27V<V_{bat}<40V
Drop Voltage	$V1_{drop}$		0.35	0.5	V	I_{out}=100mA (Note 4)
Output Current Limitation	$I1_{max}$	130	170	200	mA	$V1_{nom}$-100mV
V1 Overtemp Shut-off Threshold	$TV1_h$	160		190	°C	Junction Temperature
V1 Pre-warning Temp Threshold	$TV1_l$	130		160	°C	Junction Temperature
Temperature Threholds Difference	$TV1_h$-$TV1_l$	20		40	°C	
Reset Threshold on V1 (A and C versions)	V_{r1}	4.1	4.3	4.8	V	5.5V<V_{bat}<27V

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Reset Threshold on V1 (D version)	V_{r1}	V1-0.4	V1-0.28	V1-0.1	V	5.5V<V_{bat}<27V
Reset Active V1 Range	$V1_r$	1	V_{r1}		V	
Reset Delay Time	t_d	2		20	µs	
Line Regulation		-15	2	+15	mV	9V<V_{bat}<16.5,I_{load}=10mA
Line Regulation		-50	10	+50	mV	5.5V<V_{bat}<27V,I_{load}=10mA
Load Regulation		-50		+50	mV	1mA<I_{load}<100mA
Line Ripple Rejection		30	55		dB	100Hz, 1V_{pp} on V_{bat}=12V, I_{load}=100mA, guaranteed by design
Line Transient Response			27		mV	V_{bat} from 12V to 40V in 1µs,(10µF, ESR=3Ω)
Load Transient Response			400		mV	I_{load} from 10µA to 100mA in 1µs (C_{load}=10µF esr=3Ω) (Note 5)
Load Transient Response			16		mV	I_{load} from 10µA to 100mA in 1µs (C_{load}=10µF esr=0.1Ω)
Reverse Current From V1 to V_{bat} and Gnd	I_{Rev}			1	mA	V1=4.9V, 0<V_{bat}<4.9 V

NOTE 4: Measured when V1 has dropped 100mV below its nominal value.
NOTE 5: This condition does not produce reset.

V2 PIN

Output Voltage	$V2_{nom}$	4.75	5	5.25	V	0mA<I_{out}<200mA 5.5V<V_{bat}<40V
Drop Voltage	$V2_{drop}$		0.2	0.5	V	I_{out}=200mA (Note 6)
Drop Voltage	$V2_{drop}$		0.05	0.15	V	I_{out}=20mA (Note 6)
Output Current Limitation	$I1_{max}$	220	280	350	mA	$V2_{nom}$-100mV
Threshold on V2 to Report V2 off	V_{r2}	4.1	4.55	4.75	V	V2 Nominal
V_{r2} Delay Time		20		70	µs	
V2 Overtemp Pre-warning Threshold	T_{V2l}	130		160	°C	V2 Junction Temperature
V2 Overtemp Switch-off Threshold	T_{V2h}	155		185	°C	V2 Junction Temperature
Line Regulation		-15		+15	mV	9V<V_{bat}<16.5
Load Regulation		-75		+75	mV	4mA<I_{load}<200mA
Line Ripple Rejection		30	55		dB	100Hz, 1V_{pp} on V_{bat}, guaranteed by design
Percentage Difference V2-V1		-3		3	%	V_{bat}>9V, I_{V1}=20mA, I_{V2}=40mA

NOTE 6: Measured when V2 has dropped 100mV below its nominal value.

V3 PIN

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
High Level Voltage Drop	$V3_{drop}$		0.4	1	V	I_{V3}=-50mA, 9V<V_{bat}<40V
High Level Voltage Drop	$V3_{drop}$			1.5	V	I_{V3}=50mA, 6V<V_{bat}<9V
V3 Output Current Limitation	$I3_{lim}$	100	15	250	mA	5.5V<V_{bat}<27V
V3 Leakage Current	$I3_{leak}$			15	μA	V3=0 (V3 off)
V3 Overtemp Detection	T_{V3}	155		185	°C	Junction Temperature
V3 voltage with -30mA (negative current for Relay Switch off)	V_{V3}	0.3		0.5	V	For t≤100ms, no Functional Error Allowed
CAN TRANSCEIVER						
V2 for Forced BusStandby Mode (Fail Safe)	V_{rc2}	3	3.9	4.7	V	
CANH, CANL Pins						
Differential Receiver, Threshold Voltage		-3.2		-2.5	V	
Differential Receiver, Dominant to Recessive Threshold		-3.2		-2.5	V	(Bus failures 1, 2, 5)
CANH Recessive Output Voltage	V_{canh}			0.2	V	TX=high, R(RTH)<4k
CANL Recessive Output Voltage	V_{canl}	V2-0.2			V	TX=high, R(RTL)<4k
CANH Output Voltage, Dominant	V_{canh}	V2-1.4			V	TX=0V ; BusNormal Mode, I_{canh}= -40mA
CANL Output Voltage, Dominant	V_{canl}			1.4	V	TX=0V ; BusNormal Mode, I_{canl}=40mA
CANH Output Current Limit	I_{canh}	50	75	100	mA	(V_{canh}=0, TX=0)
CANL Output Current Limit	I_{canl}	50	95	130	mA	(V_{canl}=14V, TX=0)
Detection Threshold for Short-circuit to Battery Voltage	$V_{canh}V_{canl}$	7.3	7.9	8.9	V	BusNormal Mode
Detection Threshold for Short-circuit to Battery Voltage	V_{canh}	V_{bat}/2+3		V_{bat}/2+5	V	BusStandby Mode
CANH Output Current, Failure3			5	10	μA	BusStandby Mode V_{canh}=12V
CANL Output Current, Failure4			0	2	μA	BusStandby Mode, V_{canl}=0V, V_{bat}=12V
CANL Wake up Voltage Threshold	V_{wakeL}	2.5	3.3	3.9	V	BusStandby Mode
CANH Wake up Voltage Threshold	V_{wakeH}	1.2	2	2.7	V	BusStandby Mode
Wake up Threshold Difference	V_{wakeL}-V_{wakeH}	0.2			V	
CANH Single Ended Receiver Threshold	V_{canh}	1.5	1.85	2.15	V	Failures 4,6,7
CANL Single Ended Receiver Threshold	V_{canl}	2.8	3.05	3.4	V	Failures 3,8
CANL Pull up Current	I_{canlpu}	45	75	90	μA	BusNormal Mode

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
CANH Pull Down Current	I_{canlpd}	45	75	90	μA	BusNormal Mode
Receiver Differential Input Impedance CANH / CANL	R_{diff}	100		180	kΩ	
Differential Receiver Common Mode Voltage Range	V_{com}	-8		8	V	
RTH, RTL Pins						
RTL to V2 Switch on Resistance	R_{rtl}	10	25	70	Ω	I_{out}<-10mA, BusNormal Operating Mode
RTL to BAT Switch Series Resistance	R_{rtl}	8	12.5	20	kΩ	BusStandby Mode
RTH to Ground Switch on Resistance	R_{rth}		25	70	Ω	I_{out}<10mA, All Mode
THERMAL SHUTDOWN						
Shutdown Temperature	T_{sd}		165		°C	
AC CHARACTERISTICS						
CANL and CANH Slew Rates, Rising or Falling Edges, Tx from Recessive to Dominant State		3.5	5	10	V/μs	C_{load}=10nF, 133Ω Termination Resistors
CANL and CANH Slew Rates, Rising or Falling Edges, Tx from Dominant to Recessive State		2	3.5	10	V/μs	C_{load}=10nF, 133Ω Termination Resistors
Propagation Delay TX to RX Low	T_{dh}		1.2	2	μs	C_{load}=10nF, 133Ω Termination Resistors
Propagation Delay TX to RX High	T_{dl}		2	3	μs	C_{load}=10nF, 133Ω Termination Resistors
Min. Dominant Time for Wake-up on CANL or CANH	T_{wake}	4		40	μs	BusStandby Mode, V_{bat}=12V
Failure 3 Detection Time		10		60	μs	BusNormal Mode
Failure 3 Recovery Time		10		60	μs	BusNormal Mode
Failure 6 Detection Time		50		400	μs	BusNormal Mode
Failure 6 Recovery Time		150		1000	μs	BusNormal Mode
Failure 4, 7, 8 Detection Time		0.75		4	ms	BusNormal Mode
Failure 4, 7, 8 Recovery Time		10		60	μs	BusNormal Mode
Failure 3, 4, 7 Detection Time		0.8		8	ms	BusStandby Mode, V_{bat}=12V
Failure 3, 4, 7 Recovery Time			2.5		ms	BusStandby Mode,V_{bat}=12V
Edge Count Difference Between CANH and CANL for Failures 1, 2, 5 Detection			3			BusNormal Mode
Edge Count Difference Between CANH and CANL for Failures 1, 2, 5 Recovery			3			BusNormal Mode

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
TX Permanent Dominant Timer Disable Time	T_{txd}	0.75		4	ms	BusNormal Mode and Failure Mode
TX, MOSI, SCK, CSB						
High Level Input Voltage		0.7V1		V1+0.3V		
CSB Threshold for SPI Wake-up			2.2		V	SBC in Sleep Mode, V1<1.5V
CSB Filter Time for SPI Wake-up				3	µs	SBC in Sleep Mode, V1<1V
Low Level Input Voltage		-0.3		0.3 V1	V	
High Level Input Current on CSB		-100		-20	µA	V_i=4V
Low Level Input Current (CSB)		-100		-20	µA	V_i=1V
TX High Level Input Current	I_{TX}	-200	-80	-25	µA	V_i=4V
TX Low Level Input Current	I_{TX}	-800	-320	-100	µA	V_i=1V
SI, SCK Input Current		-10		10	µA	$0<V_{IN}<V1$
RX, INTB, MISO						
High Level Output Voltage	Voh	V1-0.9		V1	V	I_0=-250µA
Low Level Output Voltage	Vol	0		0.9	V	I_0=1.5mA
Tristated SO Output Current	Iz	-2		+2	µA	$0V<V_{so}<V1$
RSTB Pin						
High Level Input Voltage	Vih	0.7V1		V1+0.3V		
Low Level Input Voltage	Vil	-0.3		0.3V1	V	
High Level Output current 1		-50	-30	-10	µA	$0<V_{out}<0.5V1$
High Level Output current 2			-300		µA	$0.5<V_{out}<V1$
Low Level Output Voltage (I_0=1.5mA)		0		0.9	V	$1v<V_{bat}<27V$
Reset Duration after V1High	t_{res}		1		ms	
L0, L1, L2 WAKE-UP INPUTS						
Positive Switching Threshold	V_{wup}	3	3.7	4.5	V	$6V<V_{bat}<16V$
Negative Switching Threshold	V_{wun}	2.5	3	3.8	V	$6V<V_{bat}<16V$
Hysteresis	V_{hyst}		700		mV	$6V<V_{bat}<16V$
Leakage Current $0<Vwu<V_{bat}$		-5		+5	µA	
Wake up Filter Time		8	20	38	µs	
Lx input current @ 40V	Vin		350	600	µA	
DIGITAL INTERFACE TIMING						
SCLK Clock Period	t_{pSCLK}	500			ns	

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SCLK Clock High Time	t_{wSCLKH}	175			ns	
SCLK Clock Low Time	t_{wSCLKL}	175			ns	
Falling Edge of CSB to Rising Edge of SCLK	t_{lead}	250	50		ns	
Falling Edge of SCLK to Rising Edge of CSB	t_{lead}	250	50		ns	
SI to Falling Edge of SCLK	t_{SISU}	125	25		ns	
Falling Edge of SCLK to SI	$t_{SI(hold)}$	125	25		ns	
SO Rise Time (CL = 220pF)	t_{rSO}		25	75	ns	
SO Fall Time (CL = 220pF)	t_{fSO}		25	75	ns	
SI, CSB, SCLK Incoming Signal Rise Time	t_{rSI}			200	ns	
SI, CSB, SCLK Incoming Signal Fall Time	t_{fSI}			200		
Time from Falling Edge of CSB to SO Low Impedance High Impedance	$t_{SO(en)}$ $t_{SO(dis)}$			200 200	ns	
Time from Rising Edge of SCLK to SO Data Valid	t_{valid}		50	125		0.2 V1 or V2≤SO≥ 0.8V1 or V2, C_L=200pF

SOFTWARE WATCHDOG TIMINGS

(note 1: software watchdog timing accuracy are based on the running mode oscillator tolerance)

Running mode oscillator tolerance		-12		+12	%	normal request, normal and standby modes. (Note 1)
Software Watchdog Timing 1	SWt1	4.4	5	5.6	ms	(Note 1)
Software Watchdog Timing 2	SWt2	8.8	10	11.2	ms	(Note 1)
Software Watchdog Timing 3	SWt3	17.6	20	22.4	ms	(Note 1)
Software Watchdog Timing 4	SWt4	28	32	36	ms	(Note 1)
Software Watchdog Timing 5	SWt5	44.8	51	58	ms	(Note 1)
Software Watchdog Timing 6	SWt6	65	74	83	ms	(Note 1)
Software Watchdog Timing 7	SWt7	88	100	112	ms	(Note 1)
Software Watchdog Timing 8	SWt8	178	202	226	ms	(Note 1)

FORCED WAKE-UP AND CYCLIC SENSE TIMINGS

(note 2: cyclic sense and forced wake up timing accuracy are based on the sleep mode oscillator tolerance)

Sleep mode oscillator tolerance		-30		+30	%	sleep mode (Note 2)
Cyclic Sense / FWU timing 1	CYt1	22.4	32	41.6	ms	sleep mode (Note 2)
Cyclic Sense / FWU timing 2	CYt2	44.8	64	83.2	ms	sleep mode (Note 2)
Cyclic Sense / FWU timing 3	CYt3	89.6	128	166.4	ms	sleep mode (Note 2)

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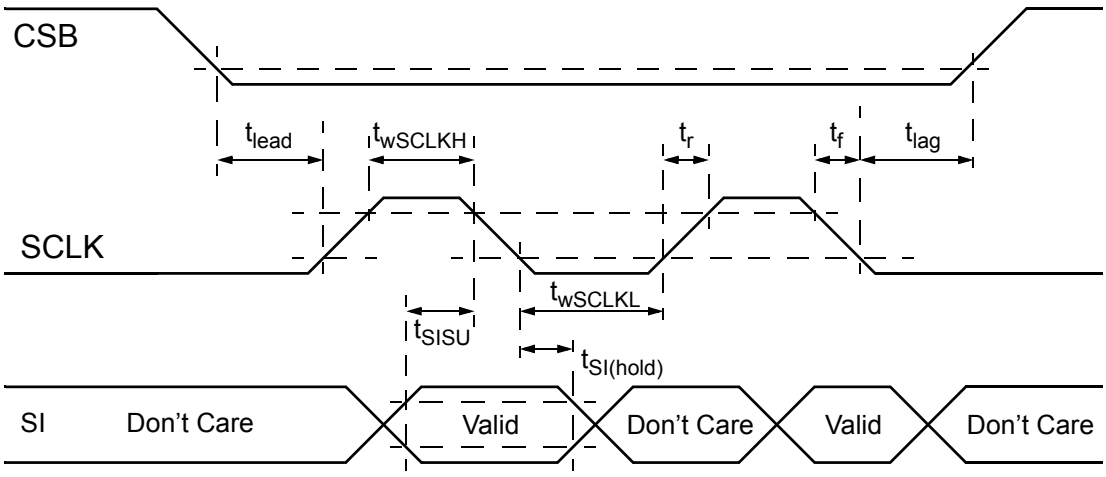
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Cyclic Sense / FWU timing 4	CYt4	179	256	333	ms	sleep mode (Note 2)
Cyclic Sense / FWU timing 5	CYt5	358	512	665	ms	sleep mode (Note 2)
Cyclic Sense / FWU timing 6	CYt6	717	1024	1331	ms	sleep mode (Note 2)
Cyclic Sense / FWU timing 7	CYt7	1434	2048	2662	ms	sleep mode (Note 2)
Cyclic Sense / FWU timing 8	CYt8	5734	8192	10650	ms	sleep mode (Note 2)

GND SHIFT DETECTION
(note 3: no over lap between two adjacent thresholds).

Ground Shift Threshold 1 (Note 3)	GS1	-1	-0.7	-0.3	V	CAN Transceiver Active In Two-wire Operation
Ground Shift Threshold 2 (Note 3)	GS2	-1.5	-1.2	-0.8	V	CAN Transceiver Active In Two-wire Operation
Ground Shift Threshold 3 (Note 3)	GS3	-2	-1.7	-1.3	V	CAN Transceiver Active In Two-wire Operation
Ground Shift Threshold 4 (Note 3)	GS4	-2.6	-2.2	-1.7	V	CAN Transceiver Active In Two-wire Operation

Figure 1. Input Timing Switch Characteristics



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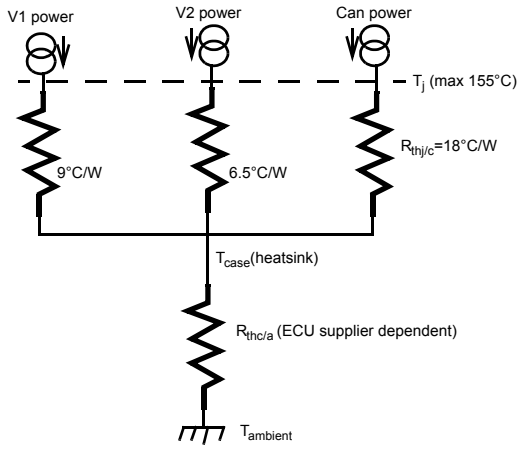
Thermal Management

The MC33389 is proposed in two different packages. HSOP20 for high power applications and SO28WB with 8 pins to the leadframe for medium power applications.

HSOP20 Package

For such a package, the heat flow is mainly vertical and each heat source (dissipating element) can be seen as an independent thermal resistance to the Heatsink. The thermal network can be roughly depicted as:

Figure 2. HSOP20 Simplified Thermal Model



Example

Assuming I_{V1}=100mA at V_{bat}=16V,
I_{V2}=150mA at V_{bat}=16V (Excluding CAN consumption).
I_{CAN}=50mA at V_{bat}=16V, we have :
P_{V1}=1.1W, P_{V2}=1.65W, P_{can}=0.55W

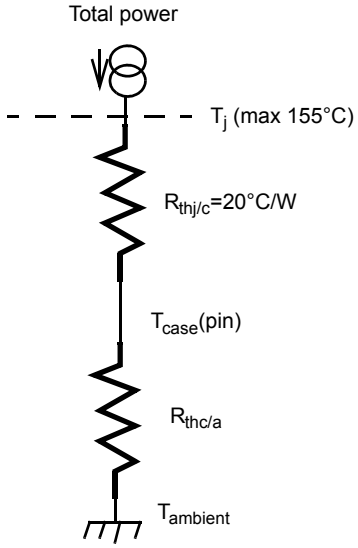
System assumptions:
If T_{amb}=85°C and $R_{thc/a}$=18°C/W, this gives:
$T_{case}=T_{amb}+R_{th\ c/a}$ x 3.3W = 85+18 x 3.3=145°C
and $T_jV1=T_jV2=T_{jcan}$=155°C.

This example represents the limit for the maximum power dissipations with a HSOP20.

SO28WB Package

The case(pin) to junction R_{th} is here represented by only one thermal resistance for the total power since the 3 power sources strongly interact on the silicon for such a package.

Figure 3. SO28WB Simplified Thermal Model



Example

Assuming I_{V1}=45mA at V_{bat}=16V,
I_{V2}=45mA at V_{bat}=16V (Excluding CAN consumption).
I_{CAN}=50mA at V_{bat}=16V, we have :
P_{V1}=0.5W, P_{V2}=0.5W, P_{can}=0.55W thus P_{total}=1.55W

System assumptions:
If T_{amb}=85°C and $R_{thc/a}$=25°C/W, this gives:
$T_{case}=T_{amb}+R_{thc/a}$ x 1.55W=85+25x1.55 =124°C
and T_jV1=124 + 20 x 1.55= 155°C.

This example represents the limit for the maximum power dissipations with a SO28WB.

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Introduction

The System Basis Chip is an integrated circuit dedicated to car body applications. It includes three main blocks :

- A dual voltage regulator
- Reset, watchdog, wake up inputs, cyclic wake up
- CAN low speed fault tolerant physical interface

Supplies

Two low drop regulators and one switch to V_{bat} are provided to supply the ECU microcontroller or peripherals, with independent control and monitoring through SPI.

Voltage Regulator V1

V1 is a 5V, 3% low drop voltage regulator dedicated to the microcontroller supply. It can deliver up to 100mA and is totally protected against short to ground (current limitation) and overtemperature. V1 is active in Normal request, Normal and standby modes.

No forward parasitic diode exists from V1 to V_{bat}. This means that, if V_{bat} voltage drops below V1, no high current flowing from V1 to V_{bat} will discharge the capacitor connected to V1. Its stored energy will only be used to supply the microcontroller and gives time to save all relevant data.

Undervoltage Reset

V1 is monitored for undervoltage (power up, power down) and a reset is provided at RSTB output for 1ms. This ensures proper initialization of the microcontroller at power-on or after supply is lost. On top of that, a flag is set in RSR register readable via the SPI.

Overtemperature Protection

V1 internal ballast transistor is monitored for overtemperature. Two detection thresholds are provided. A pre-warning threshold at 145°C and a shut-off threshold at 175°C. Once the first threshold is reached, a flag is set in the OTSR register. A maskable interrupt can be sent to the microcontroller. Once the second threshold is reached, a flag is set in the OTSR register, a maskable interrupt is sent to the microcontroller and V1 is switched off.

Once the junction temperature is back to the pre-warning threshold, V1 regulator it will be automatically switched on.

Table 4. V1 Control

Conditions For V1 On	Conditions For V1 Off
NormalRequest mode (at V1 power on)	Sleep mode (via SPI)
Normal mode (via SPI)	Shut-off temperature threshold reached
Standby mode (via SPI)	No V_{bat} power supply (cold start)
V1 below pre-warning temperature threshold	Emergency mode
During Reset	

Note: current capability of V1, V2 and V3 depends upon the thermal management. Over temperature shutdown might be reached and lead to turn off of V1, V2 and V3 for output current below their max current capability.

Voltage Regulator V2

V2 is a 5V low drop voltage regulator dedicated to peripherals supply. It can deliver up to 200mA and is protected against short to ground (current limitation) and overtemperature. V2 is active in Normal mode.

Undervoltage Detection

V2 is monitored for undervoltage and a flag is set in the VSSR register.

Overtemperature Protection

V2 internal ballast transistor is monitored for overtemperature. Two detection thresholds are provided. A pre-warning threshold at 140°C and a shut-off threshold at 165°C. Once the first threshold is reached, a flag is set in the OTSR register which is readable. A maskable interrupt can be sent to microcontroller.

Once the second threshold is reached, a flag is set in the OTSR register, V2 is switched off. It can only be switched on again via the SPI.

Table 5. V2 Control

Conditions For V2 On	Conditions For V2 Off
Normal mode (via SPI) AND V2 below shut off temperature threshold	Sleep mode, or standby mode or NormalRequest or emergency mode (via SPI)
	Shut-off temp. threshold reached
	V1 disabled (for any reason)

Switch V3

V3 is a 10Ω switch to V_{bat}, it can be used to supply external contacts or relays. A great flexibility is given for the different possible ways for its control. It is protected against short to ground (current limitation).

Overtemperature Protection

V3 output transistor is monitored for overtemperature. Once the threshold is reached, a flag is set in the VSSR register, V3 is switched off. It will be automatically switched on once the junction temperature is back to the pre-warning threshold.

Table 6. V3 Control

Conditions For V3 On	Conditions For V3 Off
Permanently in Normal mode if configured via SPI	Permanently in Normal mode if configured
Permanently in Standby mode if configured via SPI	NormalRequest mode
In sleep mode, during enable time of cyclic sense if configured	Permanently in Standby mode if configured
	Permanently in sleep mode if configured
	In sleep mode, during disable time of cyclic sense if configured
	Overtemp threshold reached
	V1 disabled (for any reason)
	V2 over temperature shutdown

Supply and V_{bat} Block

V_{bat} Monitoring

V_{bat} is the main power supply coming from the Battery voltage after an external protection diode (for reverse battery).

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V_{bat} is monitored for undervoltage and overvoltage.

V_{bat} Undervoltage

V_{bat} is monitored for undervoltage, if it is below 4V the BatFail flag is set in the VSSR register and a maskable interrupt is sent to the microcontroller.

V_{bat} Overvoltage

When V_{bat} is > 20V, the BatHigh flag is set in the VSSR register. A maskable interrupt is sent to the microcontroller. No specific action is taken to reduce current consumption (to limit power dissipation). This is to let the entire flexibility at the microcontroller for decision.

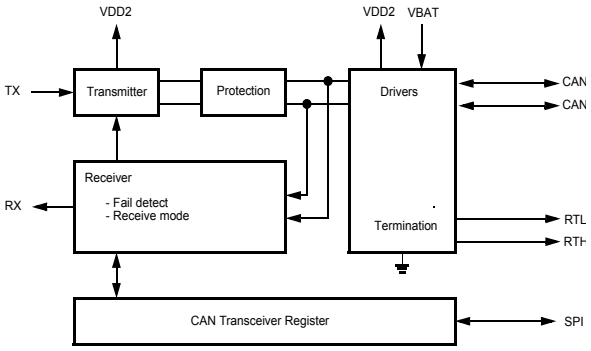
CAN Transceiver

The device incorporates a low speed 125kBaud CAN physical interface. Its electrical parameters for the CANL, CANH, Rtl,Rth,RX and TX pins are identical to the MC33388, standalone CAN physical interface.

The mode control for the CAN transceiver (normal, V_{bat} standby, sleep, etc...) are selectable through the MC33389 SPI interface.

- Baud Rate up to 125kBit/s
- Supports unshielded bus wires
- Short-circuit proof to Battery and Ground in 12V powered systems
- Supports single-wire transmission modes with Ground offset voltages up to 1.5V
- Automatic switching to single wire mode in case of Bus failures
- Automatic reset to differential mode if bus failure is removed
- Low EMI due to built in slope control and signal symmetry.
- Fully integrated receiver filters
- Thermally protected
- Bus lines protected against Automotive transients.
- Low Current BusStandby mode with wake-up capability via the Bus.
- An unpowered node does not disturb the bus lines.

Figure 7. CAN Simplified Block Diagram



CAN transceiver simplified block diagramm

CAN Transceiver Description

The CAN transceiver is an interface between CAN protocol controller and the physical bus. It is intended for low speed applications up to 125kBit/s in passenger cars. It provides differential transmission capability, but will switch in error condition to single wire transmitter and/or receiver.

The rise and fall slopes are limited to reduce RFI. This allows use of an unshielded twisted pair or a parallel pair of wires for the bus. It supports transmission capability on either bus wire if one of the bus wire is corrupted. The logic failure detection automatically selects a suitable transmission mode.

In normal operation (no wiring failures), the differential bus state is output to RX. The differential receiver inputs are connected to CANH and CANL through integrated filters. The filtered inputs signals are also used for the single wire receivers. The CANH and CANL receivers have threshold voltages that assure maximum noise margin in single wire modes. In the RXOnly mode, the transmitter is disabled but the receive part of the transceiver remains active. In this mode, RX reports bus and TX activity ($\overline{RX}$ = $\overline{TX}$ or Bus dominant). Failure detection and management is the same as BusNormal mode.

Failure Detector

The failure detector is active in RXTX and RXOnly operation mode and detects the following single bus failures and switches to an appropriate mode.

1- CANH wire interrupted
2- CANL wire interrupted or shorted to 5V
3- CANH short-circuited to battery
4- CANL short-circuited to ground
5- CANH short-circuited to ground
6- CANL short-circuited to battery
7- CANL mutually shorted to CANH
8- CANH to V2 (5V)

Note : Shorts-circuit failures are detected for 0 to 50Ω shorts.

The differential receiver (CANH-CANL) threshold is set at -2.8V, this assures a proper reception in the normal operating modes. In case of failures 1, 2 and 5 the on-going message is not destroyed due to noise margin

Failures 3 and 6 are detected by comparators respectively connected to CANH and CANL. If the comparator threshold is exceeded for a certain time, the reception is switched to single wire mode. This time is needed to avoid false triggering by external RF fields. Recovery from these failures is detected automatically after a certain time-out (filtering).

Failures 4 and 7 initially result in a permanent dominant level at RX. After a time out, the CANL driver and the RTL pin are switched off, only a weak pull up at CANL remains. Reception continues by switching to single wire mode through CANH. When the failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold for a certain time, reception and transmission switch back to the differential mode.

If any of the 8 wiring failure occurs, a flag is set in the TESRH and TESRL status registers. 8 different types of errors are distinguished out of these 8 errors and are separately stored in these register (See SPI Register Description Section on page 21). A maskable interrupt is sent to the microcontroller. On error recovery, the corresponding flag is reset after read-out operation.

During all single wire transmissions, the EMC performance (both immunity and emission) is worse than in differential mode. Integrated receiver filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In single wire mode, low frequency noise can not be distinguished from the wanted signal.

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In the event of a permanent dominant TX state (for more than 2ms) the output drivers are disabled. That assures the operation of the complete system in case of a permanent dominant TX state of one control unit. A defect control unit autonomous go to RXOnly or TermVCC mode.

Low Power Modes

The transceiver provides a low power modes which can be entered and exit by a SPI command. This is the BusStandby mode with the lowest power consumption (for the transceiver). CANL is biassed to the battery voltage via the RTL output and the pull-up current source on CANL and pull-down current source on CANH are disabled. Wake-up requests are recognized by the transceiver, when a dominant state is detected on either bus lines (Bus wake-up). On a Bus wake-up request the SBC will activate the INTB output or, if it is in sleep mode, switch to NormalRequest mode. This event is stored in the WUISR status register.

To prevent false wake-up due to transients or RF fields, wake-up threshold levels have to be maintained for a certain time. In the transceiver low power mode, failure detection circuit remains partly active to prevent increased power consumption in cases of error 3, 4,7 and 8.

Power On

After the V_{bat} supply is switched on, the SBC is in NormalRequest mode. The corresponding mode for the CAN transceiver is BusStandby.

The CAN transceiver is supplied by V2. As long as V2 is below its undervoltage threshold, the transceiver is forced to BusStandby mode (fail safe property).

Protection

A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage. If the junction temperature exceeds a maximum value, the transmitter output stages are disabled. Because the transmitter is responsible for a part of the power dissipation, this will result in a reduced power dissipation and hence a lower chip temperature. All other parts of the transceiver will remain operating. The CANH and CANL inputs are protected against electrical transients which may occur in an automotive environment.

Consequence Of Failure Detections

S1 is the switch from RTH to Ground
S2 is the switch from RTL to V2 and
S3 is the switch from RTL to V_{bat}

For each failure type is given which switch is open and which driver is disabled.

Failure 1 : nothing done
Failure 2 : nothing done
Failure3 : S1 open. Driver CANH is disabled
Failure4 : S2 and S3 open. Driver CANL is disabled
Failure5 : Nothing done
Failure6 : S2 and S3 open. Driver CANL disabled
Failure7: S2 and S3 open. Driver CANL disabled
Failure8: S1 open. CANH driver disabled

CAN Transceiver Modes

The CAN transceiver has its own functioning modes: RXTX mode, TermVBAT/TermVCC mode, and RXOnly mode. They are controlled by TCR register.

RXTX mode

Full transmitting and receiving capabilities are enabled. Full failure detection is enabled.

Note: Standard/RXTX and Extended/RXTX are equivalent.

RXOnly mode

The transmitter is disabled but the receive part of the transceiver remains active. In this mode, RX reports bus and TX activity ($\overline{RX}$ = $\overline{TX}$ or Bus dominant).

Note: Standard/RXOnly and Extended/RXOnly are equivalent.

BusStandby Mode

This is the low power mode for the CAN transceiver. The driver and receivers are disabled. Wake-up capability on both bus lines as well as failure 3, 4, 7, 8 detection are enabled. In bus standby mode RTL termination is set to V_{bat}.

Global Power Save Concept

The SBC allows to minimize power consumption of the ECU. Several operating modes are available to go to low power consumption when the full activity is not required. Several possibilities are provided to wake-up the ECU. This allows to have peripherals or the microcontroller switched off when no activity on the ECU is required.

Two switchable independent supply voltages (V1 and V2) are provided for optimum ECU power management.

Generalities

The SBC can be operated in four modes: Sleep, Standby, Normal and Emergency mode. After reset, the MC33389 is automatically initialised to a temporally mode, NormalRequest, Waiting for microcontroller configuration.

Reset Mode

This mode is entered after SBC power up, or if an incorrect Software W/D trigger occurs. The minimum duration for reset mode is 1ms typical, and unless a V1 failure condition, the SBC enters the NormalRequest mode after reset.

In case of V1 failure condition leading to V1 low (ex: short to gnd), the SBC goes in reset mode. If V1 is still below reset threshold after 100ms, the behavior depends upon the device version A, C or D:

- A version : will enter sleep mode.
- C and D versions: will stay in reset mode.

NormalRequest Mode

This is the default mode after MC33389 reset. V1 is active, V2 and V3 are passive. The SBC is not configured. The default values are set in the registers. The SBC is waiting for configuration data via the SPI.

If no SPI data is received 75ms after the Reset is released, then the SBC switches itself to sleep mode.

The data the SBC must receive to consider that the microcontroller starts the configuration sequence is the SW timing word (in SWCR register). Once received this SW timing word, the watchdog timer becomes active. Then any other control data can be sent from the microcontroller to SBC.

The watchdog is not active in NormalRequest mode before the SW timing word is programmed into the SBC. In this mode, neither V2 nor the CAN transmitter are active.

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SBC MODES

Table 8. NormalRequest: V1 active, V2&V3 passive

Entering NormalRequest	Leaving NormalRequest
SBC reset just released	When firstly receiving the SW timing word, SBC goes to Normal
	If time-out without receiving SPI commands (75ms), SBC goes to sleep

SBC Normal Mode

In this mode, V1 and V2 are active, V3 can be set active or passive via the SPI. Therefore, the whole ECU can be operated. Normal mode is entered by a SWCR register configuration in NormalRequest mode.

Table 9. SBC Normal Mode: V1 And V2 Are Active. V3 Is Active Or Passive

Entering Normal Mode	Leaving Normal Mode
By SPI command	By SPI command, going to any other mode
After SWCR register configuration in NormalRequest mode	Watchdog time out, going to NormalRequest after activating Reset
	V1 undervoltage detection, going to NormalRequest mode after activating Reset

SBC Standby Mode

In this mode V1 is active, V2 is passive. V3 can be either permanently active or permanently passive. This is a low power mode with V1 active in order to have a fast reaction time in case of any wake-up.

For standby mode, the SBC monitors the SW. It means the microcontroller runs and is monitored and must serve a watchdog trigger.

Table 10. Standby: V1 Active V2 Passive, V3 Active Or Passive, Watchdog Is Active

Entering Standby	Leaving Standby
	If SW time-out going to NormalRequest after microcontroller Reset
By SPI command	By SPI command going to any other mode
	V1 undervoltage detection, going to NormalRequest mode after activating Reset
	External activation of the RSTB pin

SBC Sleep Mode

This is a low power consumption mode. V1 and V2 are disabled. V3 can be permanently disabled or cyclically active.

Table 11. SBC Sleep Mode: V1 And V2 Are Passive, V3 Passive Or Cyclic.

Entering Sleep Mode	Leaving Sleep Mode
If SW timing not configured 75ms after entering NormalRequest mode	CAN wake-up, going to NormalRequest
By SPI command	If a wake-up is detected with cyclic sense
For MC33389ADW only: If V1 is below V1 reset for more than 100ms	If a wake-up is detected with wake-up not connected to V3 (permanent sense)
	Forced wake-up (See Forced Wake up Section)
	SPI wake-up (See Wake up by SPI Section)

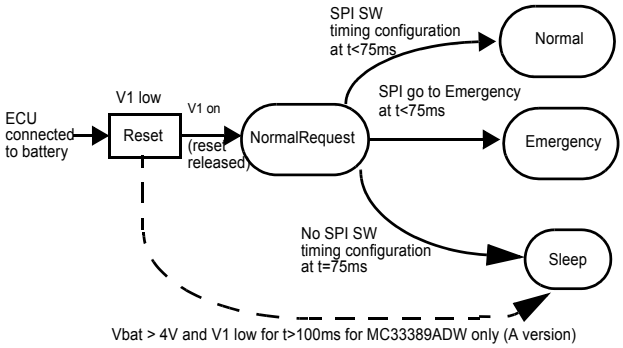
Emergency Mode

In case the microcontroller detects the ECU or the system is not under control any more, it may decide to switch the SBC to the Emergency mode. V1, V2, V3 will be passive and wake-up are not detected. The only way to leave this mode is to disconnect the ECU from the Battery voltage (BatFail detection).

Table 12. SBC Emergency Mode: V1 And V2 V3 Are Passive

Entering Emergency Mode	Leaving Emergency Mode
By SPI command	SBC BatFail detection (Disconnection of the Battery voltage)

Figure 13. Typical Behaviour At Power On



Note: In Normalrequest, if an SPI command is received before the SW timing configuration (SWCR register), it will not

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be taken into account by the SBC (except for the go to Emergency mode).

Correspondence between SBC and CAN Transceiver Modes

The table here below gives the different possible CAN transceiver modes versus SBC modes.

Table 14. CAN Modes Versus SBC Modes

When SBC Is In The Following Mode	CAN Transceiver Can Be In
Reset condition	Bus Standby mode
NormalRequest	Bus Standby mode
Normal	RXTX or RXOnly or BusStandby
Standby	Bus Standby
Sleep	Bus Standby
Emergency	Bus Standby
Normal & V2 off (over load) (note)	Bus standby

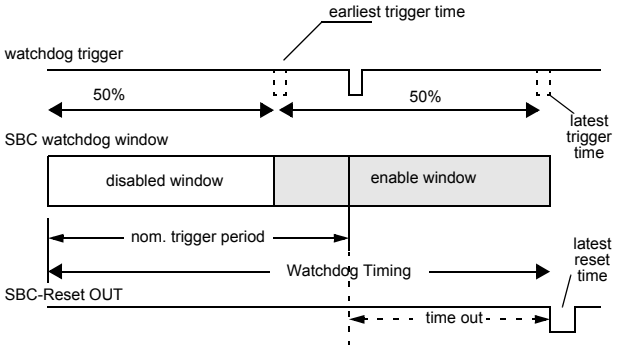
Note: In case V2 is turned off either by SPI command (standby mode) or by the SBC itself due to V2 over load condition (V2 short to gnd or V2 over temperature) the CAN is automatically set into the Bus standby mode and does not return to TXRX mode automatically when V2 is back to 5V. The CAN must be re configured to TXRX or RXonly mode after a V2 turn off.

Watchdog

General

The software window watchdog function is used to monitors the microcontroller operation in Normal and in Standby modes. The window watchdog timing is derived from the SBC-clock. The desired watchdog timing must be first transmitted during the SBC configuration, in NormalRequest mode, via SPI to SWCR register. It can also be changed later on. Selectable watchdog timings are 5ms, 10ms, 20ms, 33ms, 50ms, 75ms, 100ms and 200ms. These timings correspond to the full disable window plus full enable window.

Figure 15. Window Watchdog Timing



As soon as the watchdog trigger is received in the enable window, the internal counter is reset and start a new disable window. The SBC triggers the watchdog word at CSB low to high transition. Any watchdog trigger outside the enable window leads to SBC reset.

In Normal and Standby Modes

In normal mode the SBC get the watchdog word from the microcontroller via SPI. In case of a trigger time failure (no trigger or trigger outside the enable window) the SBC-reset is switched to active.

NormalRequest, Sleep And Emergency Mode

Watchdog is not active in this modes.

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WAKE-UP CAPABILITIES

Several wake up capabilities are available.

Forced Wake-up

The forced wake-up is enabled and disabled by SPI in V3R register. It is used in sleep mode to automatically wake-up the system by supplying V1 with proper reset. This correspond to jump into NormalRequest mode. If then, the SBC is not properly configured within 75ms, it switches back to sleep mode till the next wake-up. If both Cyclic sense and forced wake-up are enabled by the SPI in sleep mode, only Cyclic sense will be active.

The period of forced wake-up are 32ms, 64ms, 128ms, 256ms, 512ms, 1024ms, 2048ms, 8192ms, chosen by SPI in CYTCR register.

Wake-up Inputs (Local Wake-up) / Cyclic Sense

SBC provides 3 wake-up inputs to monitor external events such as closing/opening of switches. The wake-up feature is available in Normal, Standby and sleep modes. The switches can be directly connected to V_{bat} or to V3. The SBC must be properly configured by setting bit WI2V3 in register V3R. In this case, wake-ups are only detected when V3 is On. It can take advantage of V3 cyclic sense feature. If both Cyclic sense and forced wake-up are enabled by the SPI in sleep mode, only Cyclic sense will be active.

Options For Wake Input

Different conditions for wake-up can be chosen for wake-up input pins (via SPI in WUICR register).

No wake-up: No wake-up is detected, whatever occurs on wake-up inputs.

High state: if the input pin voltage is above the detection threshold during more than a 20µs filter time, a wake-up is detected. A flag is set in the WUISR register.

Low state: if the input pin voltage is below the detection threshold during more than a 20µs filter time, a wake-up is detected. A flag is set in the WUISR register.

Change of state: each change of the wake-up input pin is considered as a wake-up, if it lasts more than a 20µs filter time. The first reference state (no wake-up) is the wake-up input state when the SBC is programmed to this option. A flag is set in the WUISR register.

Multiple sampling events: when wake-up inputs are used with V3 in cyclic sense in sleep mode.

For positive edge sensitivity, 2 samples Low followed by 2 samples High are necessary to validate the wake-up condition.

For negative edge sensitivity, 2 samples High followed by 2 samples Low are necessary to validate the wake-up condition.

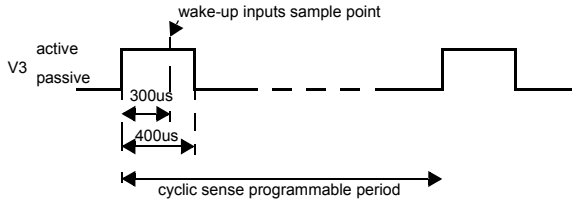
For both edge sensitivity, 2 samples at a given state followed by 2 samples in the opposite state are necessary to validate the wake-up condition.

Wake-up Inputs With Cyclic Sense

Connecting the external switches to V3 allows power saving since V3 can be programmed to be active, passive or cyclic (cyclic sense). This gives a great flexibility to reduce total power consumption while allowing full wake-up capabilities. Cyclic sense is available only in sleep mode.

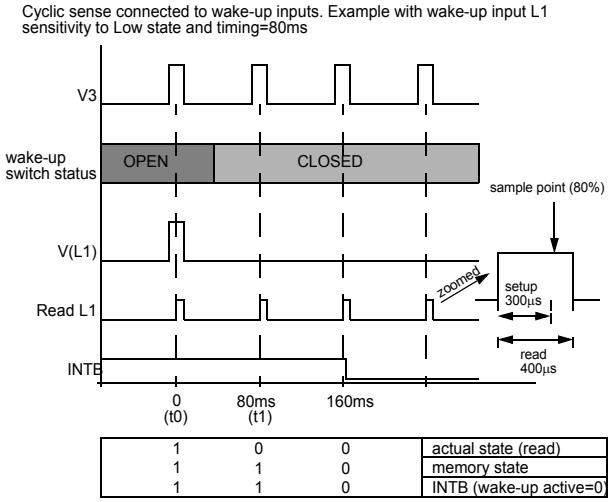
The period of the Cyclic sense can be chosen out of 8 different timings: 32ms, 64ms, 128ms, 256ms, 512ms, 1024ms, 2048ms, 8192ms programmable via SPI in CYTCR register. Once activated, V3 remains 'on' during 400µs. The wake-up inputs states are sampled at 300µs.

Figure 16. V3 Timing



Note: In sleep mode, the Cyclic Sense feature 'EXCLUSIVE OR' the forced Wake-up is chosen (not both).

Figure 17. Cyclic Sense Timing



Wake Up Inputs With Permanent Sense

Wake up detection can also be done on a permanent way in Normal and Standby mode. If the contacts are connected to V3, wake ups are only detected if V3 is on.

Wake ups are also detected on a permanent way in sleep mode if the contacts are directly connected to V_{bat} (if they are connected to V3, only cyclic sense is available in sleep mode).

Local Wake-up Consequences

In normal or standby modes, the real time state of each wake-up input pin is stored in the readable register WUIRTI. Wake-ups are detected according to the option chosen. A flag is set in the WUISR register. A maskable interrupt is sent via INTB output.

In sleep mode, a local wake-up leads to a jump to NormalRequest mode (via proper reset of the microcontroller). A flag is set in the WUISR register.

Table 18. SBC Mode Versus Local Wake-up Behaviour

SBC Modes	Local Wake-up Behaviour
NormalRequest	No detection

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WAKE-UP CAPABILITIES

SBC Modes	Local Wake-up Behaviour
Normal and Standby	Detection active according to the option. The event is stored in WUISR register.The SBC may activate INTB output. Real time state of each wake-up input pin available in WUIRTI register
Sleep	Detection active according to the option. The event is stored in WUISR register. The SBC switches to NormalRequest mode
Emergency	No detection

Wake-up By SPI

In some applications, the microcontroller might be supplied by an external VDD and remains powered in SBC Sleep mode. In this case, a feature is provided which makes possible to wake-up the SBC by SPI activity.

After V1 is totally switched off in sleep mode (V1<1.5V), if a falling edge occurs on CSB (crossing 2.5V threshold), a wake-up by SPI is detected, the SBC switches to NormalRequest mode. A flag is set in ISR2.

Interrupt Output

The INTB output may be activated in the following cases:

- V_{bat} overvoltage (BatHigh)
- V_{bat} undervoltage (BatFail)
- High temperature on V1 or V2
- Pre-warning temperature on V1 or V2
- CAN bus failure
- SPI error
- Local wake-up (can be used for low battery detection)
- Bus wake-up

All these interrupts are maskable (See Register Description Section).

RSTB Input/Output

The RSTB (reset) pin is an input/output pin. The typical reset duration from SBC to microcontroller is 1ms. If longer times are required, an external capacitor can be used. SBC provides two RSTB output pull-up currents.

A typical 30μA pull up when Vreset is below 2.5V and a 300uA pull up when reset voltage is higher than 2.5V.

RSTB is also an input for the SBC. It means the MC33389 is forced to NormalRequest mode after RSTB is released by the microcontroller

GND SHIFT DETECTION

General

When normally working in two-wire operating mode, the CAN transmission can afford some ground shift between different nodes without trouble. Nevertheless, in case of bus failure, the transceiver switches to single-wire operation, therefore working with less noise margin. The affordable ground shift is decreased in this case.

The SBC is provided with a ground shift detection for diagnosis purpose. Four ground shift levels are selectable and the detection is stored in the GSLR register which is accessible via the SPI.

Detection Principle

The gnd shift to detect is selected via the SPI out of 4 different values (-0.7V, -1.2V, -1.7V, -2.2V). At each TX falling edge (end of recessive state) CANH voltage is sensed. If it is detected to be below the selected gnd shift threshold, the bit SHIFT is set at 1 in GSLR register. No filter is implemented. Required filtering for reliable detection should be done by software (e.g. several trials).

DEVICE DIFFERENT VERSIONS

The MC33389 is proposed in several package versions, and also offers slight differences in term of functionalities.

The device version is identified in the device part number by the first letter after the 389 number.

The package identification is done by the last two letters of the part number (DW for SO28 wide body, DH for power SO20).

Differences between A, C and D versions:

Behavior for V1 low:

A version:

If V1 is below reset threshold, device enters reset mode, and if V1 stays below reset threshold for more than 100ms, then the SBC automatically enters sleep mode. This could be the case if V1 is shorted or permanently over loaded, and going to sleep mode would then avoid system over current consumption.

This concerns the device reference: MC33389ADW and MC33389ADH.

C and D versions:

If V1 is below reset threshold, the SBC enters and stays in reset mode (reset low) permanently.

This concerns the device reference: MC33389CDW and MC33389CDH and MC33389DDW

Reset threshold specification:

A and C versions:

The reset threshold is defined per table “electrical parameter, V1 pin 5V.

This concerns device MC33389ADW, ADH, CDW and CDH

D version : The reset threshold for the D version is slightly higher than the A and C versions. Refer to device electrical parameter table, V1 pin 5V

This concerns device reference MC33389DDW.

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Table 19. SBC Operation Mode

mode	V1 & V2 regulators, V3 switch	Wake up capabilities (if enabled)	Reset pin	INT	Software Watchdog	CAN cell
Reset state	V1: ON (unless failure condition V2: OFF V3: OFF		Low (duration 1ms)			TermVbat
Normal Request	V1: ON (75ms time out) V2: OFF V3: OFF		High. (Active low -go to reset state- if V1 under voltage occurs)			Term Vbat
Normal	V1: ON V2: ON V3: ON or OFF		High. (Active low -go to reset state- if W/D or V1 under voltage occurs)	If enabled, signal failure condition or L0/L1/L2 inputs state change.	Running	Tx/Rx, or Rx Only, or TermVbat
Standby	V1: ON V2: OFF V3: ON or OFF		same as Normal Mode	same as Normal Mode	Running	TermVbat
Sleep	V1: OFF V2: OFF V3 OFF or cyclic	- CAN - SPI - L0,L1,L2 - Cyclic sense - Forced Wake up	Low	Not active	Not Running	TermVbat + Wake up capability
Emergency	V1: OFF V2: OFF V3 OFF	none	Low	Not active	Not Running	TermVbat

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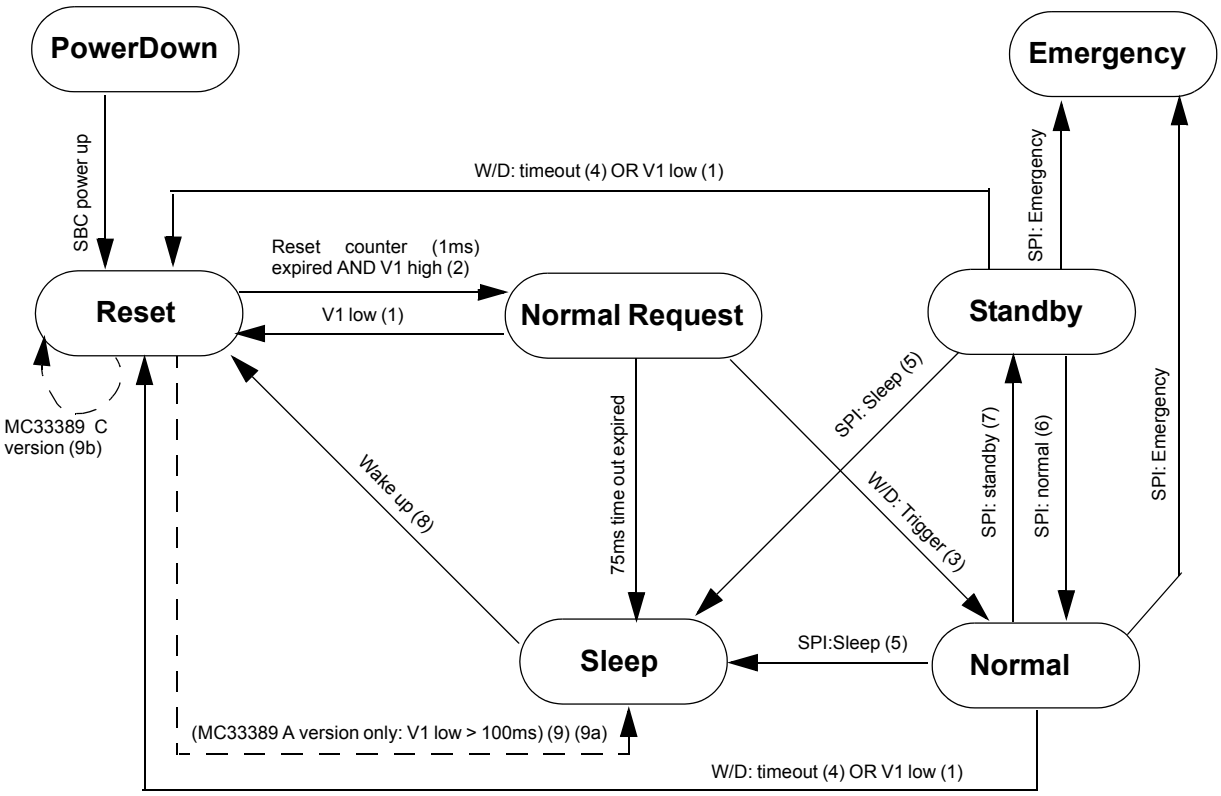
Figure 20. State Machine



Legend:
1: “V1 low” means V1 below reset threshold
2: “V1 high” means V1 above reset threshold
3: “W/D: Trigger” means SCWR register write operation during Normal Request mode.
4: “W/D: time out” means SWCR register not written before W/D time out period expired, or W/D written in incorrect time window. In normal request mode time out is 75ms.
5: “SPI: Sleep” means SPI write command to MCR and MCVR registers, data sleep
6: “SPI: Normal” means SPI write command to MCR and MCVR registers, data normal
7: “SPI: Standby” means SPI write command to MCR and MCVR registers, data standby
8: “Wake up” means one of the following event occur: CAN wake up, Forced wake, Cyclic sense wake up, Direct Lx wake up or SPI CSB wake up.

9: “V1 low > 100ms” means V1 below reset threshold for more than 100ms.
9a: This condition leads to SBC in sleep mode only for the MC33389ADW (SO28 package).
9b: V1 low for > 100ms does not lead to sleep mode for the MC33389CDW (SO28WB package) and for the MC33389CDH (HSOP20 package).

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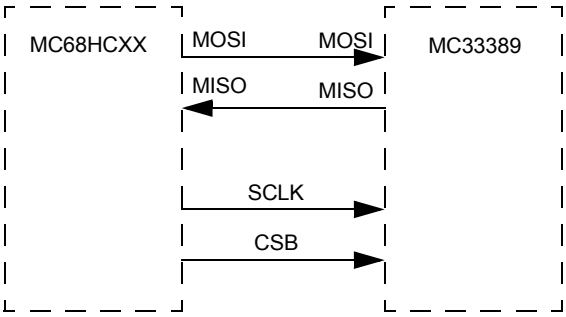
General Description

The SPI system is flexible enough to communicate directly with numerous standard peripherals and MCUs available from Motorola and other semiconductor manufacturers. SPI reduces the number of pins necessary for input/output on the MC33389. The SPI system of communication consists of the MCU transmitting, and in return, receiving one databit of information per clock cycle. Databits of information are simultaneously transmitted by one pin, Microcontroller Out Serial In (MOSI), and received by another pin, Microcontroller In Serial Out (MISO), of the MCU. Figure 21 below shows the basic SPI configuration between an MCU and one MC33389. The SPI serial operation is guaranteed to 2.0 MHz.

Figure 21. SPI Interface With Microcontroller



Control and Status Reporting of the MC33389

The MCU is responsible for the control data transfer to the MC33389, while the MC33389 reports its status to the MCU. Summarized below are the major data for control and status reporting.

- SPI initialization during start up
- MC33389 control during operation
- Watchdog triggering
- Reading status registers of the MC33389

Control Data

The control data are transferred from the MCU to the MC33389. A control word includes an address of a certain control register and the appropriate data. Basically the following data will be transferred (See the SPI Register Description section on page 21).

- MC33389 mode control
- Supply control
- Forced wake-up timing
- Cyclic sense control
- Watchdog control
- Transceiver control

Status Data

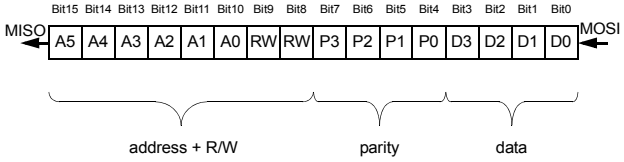
The status data are transmitted from the MC33389 to the MCU. After receiving a valid register address from the MCU, the MC33389 returns the appropriate status. Some of the major status data are listed below:

- Current operation mode status
- Wake-up sources
- Reset status
- Error status
- Overtemperature status
- Transceiver status

Data Transfer

The data to and from the MC33389 are transferred in form of two bytes.The structure of the transferred information is the same for control the MC33389 and status reporting. The address field A5 to A0 (Bit15 to Bit10) contains the address of a control or status register in the MC33389. RW (Bit9 and Bit8) contains the read/write flag for the data field. The parity field is located at P3 to P0 (Bit7 to Bit4). The data field D3 to D0 (Bit3 to Bit0) is attached to the 2 byte data word, see figure below.

Figure 22.



The SBC is accessible via the SPI interface in NormalRequest mode, Normal mode and Standby mode. In all other modes (Sleep mode, Emergency mode), the voltage supply for the microcontroller in permanently switched off and the SBC input logic for MISO, MOSI, CSB and SCLK isn't working (except SPI wake-up function in Sleep mode).

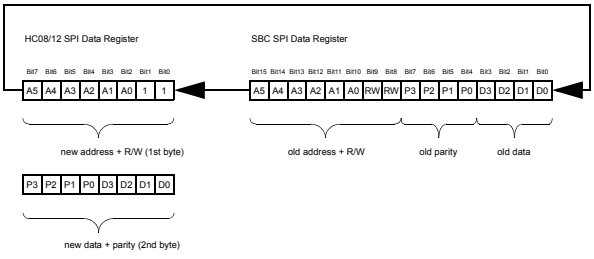
Writing Data

To write data in a SPI register, two one-byte transmissions have to performed. The first byte contains the address of the register (MSB first) and the read/write bits which have to be set to 1. The second byte contains the new data addressed by the previous byte (MSB first) and the parity information. The calculation of the parity field P3-P0 has to follow the equations below:

$$P3 = D3 \oplus D0 \quad \text{(EX-OR)}$$
$$P2 = D3 \oplus D2$$
$$P1 = D2 \oplus D1$$
$$P0 = D1 \oplus D0$$

Note, that during the transmission of the two bytes the CSB pin remains 0. See figure23 hereafter.

Figure 23.



The SBC sends back the old address, R/W, parity, and data information from a previous transmission. This data contains no useful information (e.g. status).It shouldn't be used.

In case of a wrong address field or parity mismatch, an interrupt will be issued and the SBC retains the old state.

Reading Data

To read data from a dedicated register two one-byte transmissions have to be performed. The first byte contains the address of the register (MSB first) and the read/write flag setting to 0. The second byte needn't to contain valid data,

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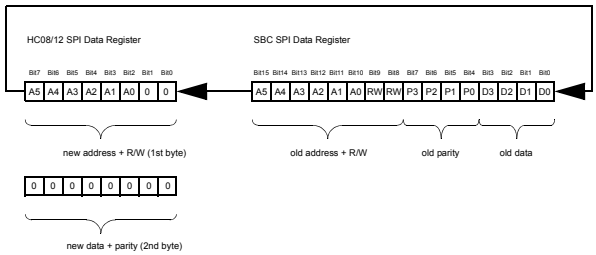
nevertheless the parity calculation has to performed to avoid an interrupt caused by a parity mismatch.

During a read operation the SBC sends back the old address and R/W bits and the new data addressed by the first transmitted byte starting with P3 after the last valid read/write bit has been received.

Note, that during the transmission of the two bytes the CSB pin remains 0.

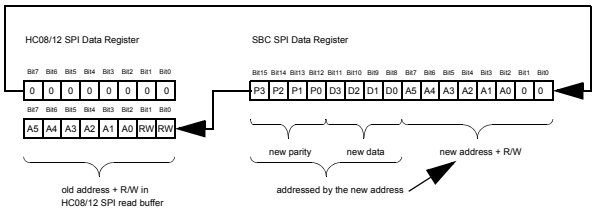
Figure below shows the content of the HC08/12 SPI DataRegister and the SBC SPI Data Register before the transmission. The new address and R/W bits are already in the SPI Data Register while the new data and parity bits are still in an appropriate microcontroller register or memory. This 2nd byte has to be loaded into the HC08/12 SPI Data Register after the first byte has been transmitted to the SBC.

Figure 24.



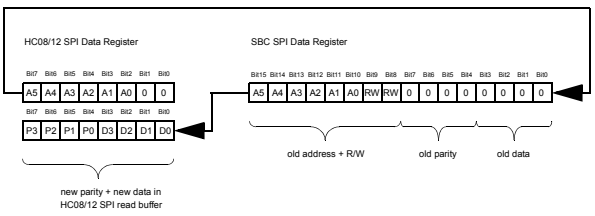
After transmission of the 1st byte the HC08/12 SPI read buffer contains the old address and R/W bits received from the SBC. An appropriate operation in the microcontroller loads the new data and parity into the HC08/12 SPI Data Register (2nd byte). In the SBC the internal logic loads P3-P0 and D3-D0 to the location of Bit15 to Bit8 in the SBC SPI Data Register and will shift this data within the remaining eight clock cycles (Figure below 25).

Figure 25.



After sixteen clock cycles the microcontrollers read buffer contains the new parity and data and is now ready for the next transmission (See figure hereafter 26)

Figure 26. .



Safety Concept

Due the fact the SPI interface is an on-board interface without any data fault detection capabilities, the SPI interface of the MC33389 provides built-in fail save functions.

Address coding, based on increasing the Hamming distance, parity check and generation for data.

For the address and the read/write bits only codes with a Hamming distance < 2 will be used. So, any single bit failure caused by disturbances will be recognized and handled. When one bit toggles in the address field during the transmission, no misbehaviour occurs.

Additionally, validation registers are implemented to validate safety critical settings in the MC33389, e.g. the mode control register MCR and its validation register MCVR. To change the appropriate settings, both registers must have the same content to switch to another mode.

To increase data integrity a parity check is used. A parity module in the MC33389 ascertains the parity of the data field and compares the result with the received parity. When the parity check is successfully passed, data will be written into the addressed registers. The parity bits P3 to P0 results from the logic equations below:

$$P3 = D3 \oplus D0 \quad \text{(EX-OR)}$$

$$P2 = D3 \oplus D2$$

$$P1 = D2 \oplus D1$$

$$P0 = D1 \oplus D0$$

In case of error detection, the incoming data is not taken in the SBC and an error flag is set in an SPI register.CSB Pin

The system MCU selects the MC33389 to be communicated with, through the use of the CSB pin. Whenever the pin is in logic low state, data can be transferred from the MCU to the MC33389 and vice versa. Clocked-in data from the MCU is transferred from the MC33389 shift register and latched into the addressed registers on the rising edge of the CSB signal if the read/write bit is set and the parity check was successful.

The CSB pin controls the output driver of the serial output pin. Whenever the CSB pin goes to a logic low state, the MISO pin output driver is enabled allowing information to be transferred from the MC33389 to the MCU. To avoid any spurious data, it is essential that the high-to-low transition of the CSB signal occur only when SCLK is in a logic low state.

SCLK Pin

The system clock pin (SCLK) clocks the internal shift registers of the MC33389. The serial input pin (MOSI) accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (MISO) shifts data information out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to guarantee validity of data. It is essential that the SCLK pin be in a logic low state whenever chip select bar pin (CSB) makes any transition. For this reason, it is recommended though not necessary, that the SCLK pin be kept in a low logic state as long as the device is not accessed (CSB in logic high state). When CSB is in a logic high state, any signal at the SCLK and MOSI pin is ignored and MISO is tristated (high impedance).

MOSI Pin

This pin is for the input of serial instruction data. MOSI information is read in on the falling edge of SCLK. To program the MC33389 by setting appropriate programming registers, an sixteen bit serial stream of data is required to be entered

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the MOSI pin starting with Bit15, followed by Bit14, Bit13, etc., to Bit0. For each fall of the SCLK signal, with CSB held in a logic low state, a databit is loaded into the shift register per the databit MOSI state.The shift register is full after sixteen bits of information have been entered.

MISO Pin

The serial output (MISO) pin is the tri-stateable output from the shift register. The MISO pin remains in a high impedance state until the CSB pin goes to a logic low state. The MISO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. The MOSI/MISO shifting of data follows a first-in-first-out protocol with both input and output words transferring the MSB first.

Module Address Map, the module address map is shown in table below.

Table 27. Module Address Map

Address	Register	Register Name
$000	Mode Control Register	MCR
$003	Mode Control Validation RegisterMCVR	MCVR
$005	V3 control register	V3R
$006	Cyclic timing control register	CYTCR
$009	Software watchdog control register	SWCR
$00A	Ground shift level register	GSLR
$00C	Wake-up input control register	WUICR
$00F	Wake-up input status register	WUISR
$011	Wake up input real time information	WUIRTI
$012	Overtemperature status register	OTSR
$014	Transceiver error status register for CANH	TESRH
$017	Transceiver error status register for CANL	TESRL
$018	Reset source register	RSR
$01B	Voltage supply status register	VSSR
$01D	Interrupt mask control register 1	IMR1
$01E	Interrupt mask control register 2	IMR2
$021	Interrupt source register 1	ISR1
$022	Interrupt source register 2	ISR2
$024	Transceiver control register	TCR

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Table 28. MCR —Mode Control Register

MCR and MCVR registers are used to control the mode of the SBC. To change the operating mode of the SBC, both registers must have the same content. The order of writing the registers has to be taken into account. To set the SBC mode properly, MCR has to be written first then followed by MCVR write. A write operation sets the MCR and MCVR registers, a read operation perform a read out of the current status (MSR - mode status register).

The Emergency mode is a regular mode.

A reset of both MCR and MCVR registers occurs when RSTB = low and the SBC is set to NormalRequest mode.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCR $000	R						MSR2	MSR1	MSR0
	W						MCR2	MCR1	MCR0
RESET							0	0	0

Table 29. MCVR — Mode Control Validating Register

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCVR $003	R						MSVR2	MSVR1	MSVR0
	W						MCR2	MCR1	MCR0
RESET							0	0	0

Table 30.

MC(V)R2	MC(V)R1	MC(V)R0		MSR2	MSR1	MSR0
Automatically entered after reset			NormalRequest	0	0	0
0	0	1	Normal	0	0	1
0	1	0	Standby	0	1	0
1	0	0	Sleep	1	0	0
1	1	1	Emergency	1	1	1

Table 31. V3R — V3R Control Register

This register is used to configure the state of V3 high side switch in normal and standby modes, and the V3 operation and the Forced wake up or the cyclic sense option for the sleep mode operation.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
V3R $005	R					WI2V3	FWU	CYS	V3R0
	W								
RESET						1	0	0	0

Table 32.

WI2V3	FWU	CYS	V3R0		Comments
X	0	0	0	V3 off	Only In Normal And Standby Mode Available
X	0	0	1	V3 on	
X	X	1	X	Cyclic Sense On	

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WI2V3	FWU	CYS	V3R0		Comments
X	1	0	X	Forced Wake-up On	Only In Sleep Mode Available
1	X	X	X	wake-up inputs linked to V3	

Note: In low power modes cyclic sense has priority. A reset of the register occurs when RSTB = low.

Table 33. CYTCR — Cyclic Timing Control Register

This register is used to select the cyclic sense or force wake up timing.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CYTCR $006	R						CYTCR2	CYTCR1	CYTCR0
	W								
RESET							0	0	0

Table 34.

CYTCR2	CYTCR1	CYTCR0	Comments	t(ms) typical
0	0	0	Timer on, t1 (default)	32
0	0	1	Timer on, t2	64
0	1	0	Timer on, t3	128
0	1	1	Timer on, t4	256
1	0	0	Timer on, t5	512
1	0	1	Timer on, t6	1024
1	1	0	Timer on, t7	2048
1	1	1	Timer on, t8	8192

A reset of the register occurs when RSTB = low

Table 35. SWCR — Software Watchdog Control Register

This register is used to select the window watchdog time period. Open window of the selected period is only the second half of the selected period.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SWCR $009	R						SWCR2	SWCR1	SWCR0
	W								
RESET							0	0	0

Table 36.

SWCR2	SWCR1	SWCR0	Comments	t(ms) typical
0	0	0	Timer on, t1 (default)	5

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SWCR2	SWCR1	SWCR0	Comments	t(ms) typical
0	0	1	Timer on, t2	10
0	1	0	Timer on, t3	20
0	1	1	Timer on, t4	33
1	0	0	Timer on, t5	50
1	0	1	Timer on, t6	75
1	1	0	Timer on, t7	100
1	1	1	Timer on, t8	200

The SW watchdog is only running in Normal and Standby mode. A reset of this register occurs when RSTB = low

Table 37. GSLR — Ground Shift Level Register

This register is used to monitor the ground shift of the vehicle network.

r

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GSLR $00A	R					TXDOM	SHIFT	GSLR1	GSLR0
	W								
RESET							0	0	0

Table 38.

GSLR1	GSLR0	Typ GND Shift Level
0	0	0.7V
0	1	-1.2V
1	0	-1.7V
1	1	-2.2V

SHIFT

1=ground shift above the threshold selected by GSLR1 and GSLR2. 0=no ground shift

The SHIFT information is latched until a read operation of the GSLR register occurs. The GSLR register is set to 0 after power on reset. A reset of GSLR1 and GSLR0 occurs when RSTB = low.

TXDOM

0 = no failure on TX

1 = TX permanent dominant

Table 39. WUICR — Wake-up Input Control Register/SPI And Bus Wake-up Status

This register is used to configure the wake up level for the L0, L1 and L2 inputs. in read operation it reports the CAN wake up and SPI (csb) wake up events

.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WUICR $00C	R					SPIWU	BUSWU	WUICR1	WUICR0
	W								
RESET						0	0	0	0

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Table 40.

WUICR1	WUICR0	Description	Comments
0	0	Wake-up inputs disabled	
0	1	Positive edge sensitive	
1	0	Negative edge sensitive	
1	1	Positive and negative sensitive	

Table 41.

SPIWU	BUSWU	Description	Comments
0	0	No wake-up events	
X	1	Wake-up event on CAN bus	
1	X	Wake-up event on SPI bus	

The information in SPIWU and BUSWU is latched. Bits SPIWU and BUSWU will be reseted by a read operation of the WUICR register and are set to 0 after a power on reset. A reset of WUICR1 and WUICR0 occurs when RSTB = low.

Table 42. WUISR — Wake-up Input Status Register

This register is used to read back the wake input (L0, L1 or L2) which has cause the SBC to wake up.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WUISR $00F	R						WUISR2	WUISR1	WUISR0
	W								
RESET							0	0	0

Table 43.

WUISR2	WUISR1	WUISR0		Comments
0	0	0	No Event on Wake-up Inputs	
X	X	1	Event on L0	
X	1	X	Event on L1	
1	X	X	Event on L2	

In case of a wake-up event, the appropriate bit is set to 1. The bits will be reseted by a read operation of the register. After power on reset all bits are set to 0.

Table 44. WUIRTI — Wake-up Input Real-time Information

This register reports the real time information on the state (high or low) of the L0, L1 and L2 inputs.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WUIRTI $011	R						WUIRTI2	WUIRTI1	WUIRTI0
	W								
RESET									

The bits WUIRTI2-0 contain the real time logic value coming from the wake-up inputs (0 mean input below threshold, 1 mean input above threshold. Typical threshold is 3.5V).

Table 45. OTSR — Overtemperature Status Register

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This register is used to read back the overtemperature status for the V1 and V2 regulators. In write mode, it is used to turn V2 on after a V2 over temperature shutdown has occurred.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OTSR $012	R					OPWV2	OPWV1	OTV2	OTV1
	W							OTV2C	
RESET						0	0	0	0

OTV1: 1=V1 overtemperature shutdown, 0=V1 no overtemperature
OTV2: 1=V2 overtemperature shutdown, 0=V2 no overtemperature
OPWV1: 1=V1 overtemperature pre-warning, 0=V1 normal temperature
OPWV2: 1=V2 overtemperature pre-warning, 0=V2 normal temperature

In case of V1 or V2 overtemperature the appropriate voltage regulators are switched off automatically and the overtemperature flags are set (latched). The flags can be reseted by a read operation of the register OTSR.

Once V2 has been switched off because of overtemp (OTV2=1) it can only be switched on again by forcing OTV2C=0 by a write operation.

The V1 and V2 pre-warning flags are set as long as the first overtemperature exists. The flags disappear, when the temperature is below the threshold. An overtemperature of the V2 power supply will also switch off V3. After a power on reset all bits of the register are set to 0.

Table 46. TESRH — Transceiver Error Status Register For CANH

Register used to report the CAN H failure status

.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TESRH $014	R					TESRH3	TESRH2	TESRH1	TESRH0
	W								
RESET						0	0	0	0

Table 47.

TESRH3	TESRH2	TESRH1	TESRH0	
0	0	0	0	No failure on CANH
0	X	0	1	CANH wire interruption
X	X	1	X	CANH short circuited to V_{bat}
0	1	0	X	CANH short circuited to ground
1	X	0	X	CANH short circuited to V_{CC}

In case of CANH line failures, the appropriate bit(s) are set according to table 46. This information is latched. The register can be reseted by a read operation. After power on reset, all bits are set to 0.

Table 48. TESRL — Transceiver Error Status Register For CANL And Tx

Register used to report the CANL and Tx permanent dominant failure status

.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TESRL $017	R					TESRL3	TESRL2	TESRL1	TESRL0
	W								
RESET						0	0	0	0

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Table 49.

TESRL3	TESRL2	TESRL1	TESRL0	
0	0	0	0	No failure
0	X	0	1	CANL wire interruption
0	1	0	X	CANL short circuited to ground/ CANH mutually shorted to CANL
X	X	1	X	CANL short circuited to V_{bat}
1	X	0	X	CANL short circuited to Vdd

In case of CANL line failures, the appropriate bit(s) are set according to table 48. This information is latched and the register can be reseted by a read operation. After power on reset, all bits are set to 0.

Table 50. RSR — Reset Source Register

This register reports the source of a reset that has occurred

.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RSR $018	R						RSR2	RSR1	RSR0
	W								
RESET							1	0	1

RSR0: 1 => VDD1 undervoltage occurred (RSR2=1 in this case), 0=> no undervoltage on VDD1 occurred
RSR1: 1 =>SW watchdog reset occurred (RSR2=1 in this case), 0=>no SW watchdog reset occurred
RSR2: 1 =>external reset occurred (RSR0=RSR1=0 in this case), 0=>no external reset occurred
Events related to the bits in register RSR are latched. All bits can be reseted by a read operation of the register. After a power on reset, RSR2 and RSR0 are set to 1. Therefore the first read out of the register after power on delivers RSR[2:0] = [101].

Table 51. VSSR — Voltage Supply Status Register

Register used to monitor the status of the V2, V3 and Vbat voltage level.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VSSR $01B	R					V3SR	V2SR	VBSR1	VBSR0
	W								
RESET						0	0		
POR						0	0	0	1

Table 52.

VBSR1	VBSR0	
0	0	No failure on V_{bat}
X	1	Undervoltage (BatFail)
1	X	Overvoltage (BatHigh)

V2SR: 1=V2 on, 0=V2 off
V3SR: 1=V3 overtemperature, 0=V3 no overtemperature
VBSR1 is a real time information and cannot be reseted. Bits V3SR, V2SR and VBSR0 are latched and can be reseted by a read operation of the register.

Table 53. IMR1 — Interrupt Mask Control Regis

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The next two registers (IMR1 and IMR2) are used to mask the interrupt function.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IMR1 $01D	R					HV	HTPW	MTPW	BATU
	W								
RESET						0	0	0	0

Table 54. IMR2 — Interrupt Mask Control Register 2

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IMR2 $01E	R						BUSF	SPIE	WU
	W								
RESET							0	0	0

To enable the appropriate interrupt, the mask bit has to be set to 1. For disabling the interrupt the bit must be cleared to 0. After a power on reset or RSTB = low, the bits are cleared to 0. All interrupts are disabled. Explanation for the abbreviations:
HV : V_{bat} high voltage
HT : High temperature on V1 or V2
MTPW : Medium temperature pre-warning on V1 or V2
BATU: Battery undervoltage (BatFail)
BUSF : CAN bus failure
SPIE : SPI error
WU : Wake-up

Table 55. ISR1 — Interrupt Source Register

The next two registers (ISR1 and ISR2) are used to read the interrupt source.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISR $021	R					HV	HTPW	MTPW	BATU
	W								
RESET						0	0	0	0

Table 56. ISR2 — Interrupt Source Register 2

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISR $022	R						BUSF	SPIE	WU
	W								
RESET							0	0	0

All bits in registers ISR1 and ISR2 are copies of the appropriate bits in different SPI registers. For a faster read out, these bits are merged in ISR1 and ISR2. A reset cannot be done for registers ISR1 and ISR2.

Table 57. TCR—Transceiver Control/Status Register

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This register is used to control the state of the CAN transceiver (CAN transceiver state is also dependant upon the SBC mode). When it is read, this register reports the CAN transceiver state and a CAN overtemperature condition

.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TCR $024	R					TOT	TSR2	TSR1	TSR0
	W						TCR2	TCR1	TCR0
RESET						0	0	0	0

Table 58.

TCR2	TCR1	TCR0		TSR2	TSR1	TSR0
0	0	0	Standard/TermV_{bat}	0	0	0
	1	0	Standard/RXOnly	0	1	0
	1	1	Standard/RXTX	0	1	1

TOT
1 => Transceiver overtemperature
0 => normal temperature
The MODE bit selects between the standard and extended physical layer mode.
Any conditions forcing the transceiver to TermVbat lead to reset of TCR0 TCR1 bits.
After power on reset all bits of the register are set to 0. The information TOT is latched.
To reset TOT a read operation of TCR has to be performed. In case of RSTB = low the register content remains unchanged.

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Sleep Mode Activation

Once in sleep mode, the SBC turns off V1 and V2 regulator. Thus the micro controller can not run any mode.

in order to have it run again, the SBC should enable and turn on V1, and this is achieve by an SBC wake up event.

Several options are available to wake up the SBC and the application and have the micro controller in run mode.

Some wake up are selectable, some are always active in sleep mode.

- Wake up from CAN interface and wake up from SPI (CSB) are always active.

- Wake up from L0/L1/L2 inputs, with and without cyclic sense and the FWU (Forced Wake Up) are selectable. The selection must be done while the SBC is in Normal or Standby mode, and prior to enter sleep mode.

General Condition To Enter Sleep Mode

In order to make sure the SBC enters the sleep mode, and in addition to the write into MCR and MCVR register, all previous wake up conditions must have been cleared. To clear a wake up condition requires that the appropriate register is read.

After an SBC power up from “zero” (battery power up or cold start), the following registers must be read:

- WUICR: possible wake up event report from CAN bus
- RSR: report a V1 undervoltage
- VSSR: reports a Vbat fail flag

Once these read operation are done, the wake up conditions or flag are reset.

The VSSR register bit VBSR0 can be used to determined if the SBC has experience a loss of battery voltage.

After an SBC wake up from “sleep mode” the following registers indicate the wake up source and must be cleared in order to allow the SBC to enter sleep mode again:

- WUICR: wake up event report for CAN or SPI buses.
- WUISR: Wake up event report for the L0/L1/L2 inputs.
- RSR: report a V1 undervoltage
- VSSR: reports a Vbat fail flag
- etc

The paragraphs below describe the write operation to be done for the several sleep mode and wake up control options.

In addition to FWU, cyclic sense and direct wake up, the CAN and SPI wake will always be activated.

Sleep Mode With CAN And SPI Wake Up

The enter sleep mode and activate the only the CAN or SPI wake up, no dedicated wake up condition must be done. In sleep mode the SBC has CAN and SPI wake up always active. To enter sleep mode in this case, while the SBC is in normal or standby mode:

- Write to V3R register: data 0000 (this clear the bit WI2V3 which is set to1 after reset).
- Write to MCR register: data SLEEP (100)
- Write to MCVR register: data SLEEP (100)

The SBC then enters sleep mode.

Sleep Mode Enter With Forced Wake Up

To enter sleep mode and activate the forced wake up the following register must be written:

- Write to V3R register, data 0100), this set the FWU bit to 1.
- Write to CYTCR register the desired wake up time. (This sets the time the SBC will stay in sleep mode).
- Write to MCR register: data SLEEP (100)
- Write to MCVR register: data SLEEP (100)

The SBC then enters sleep mode. It will wake up after the time period selected in the CYTCR register.

Sleep Mode Enter With Cyclic Sense

To enter sleep mode and activate the cyclic sense wake up the following register must be written:

- Write to V3R register, data 1010, this set the VI2V3 and CYS bits to 1.
- Write to CYTCR register the desired cyclic sense period. (This sets the time the SBC will wait in sleep mode to turn on V3 and sense the Lx inputs).
- Write to WUICR bits 0 and 1 to select the edge sensitivity for the Lx inputs.
- Write to MCR register: data SLEEP (100)
- Write to MCVR register: data SLEEP (100)

The SBC then enters sleep mode. It will periodically turn on V3 and while V3 is on, sample the level of the Ls inputs.

If any of the 3 Lx inputs is in the correct state for two consecutive samples, SBC will wake up. If not, it will stay in sleep mode. (refer to device description for detail).

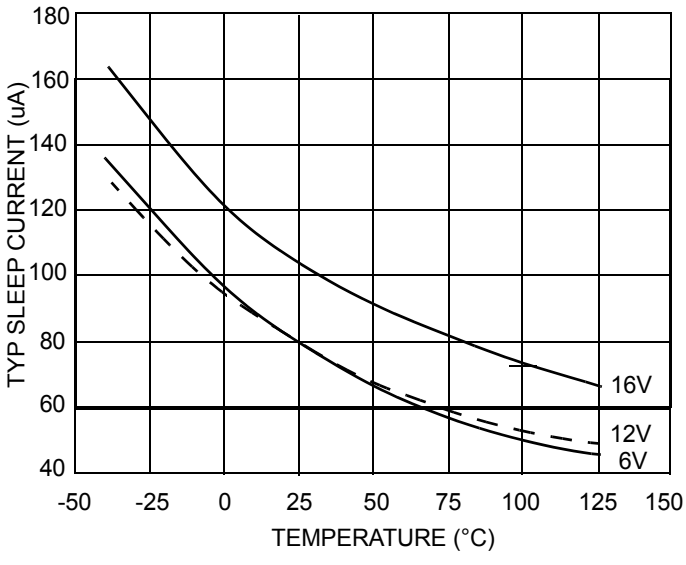
Sleep Mode Enter With Direct Lx Input Wake Up

To enter sleep mode and activate the direct wake up from the Lx inputs, the following register must be written:

- Write to V3R register, data 0000), this clear VI2V3 bit.
- Write to WUICR bits 0 and 1 to select the edge sensitivity for the Lx inputs.
- Write to MCR register: data SLEEP (100)
- Write to MCVR register: data SLEEP (100)

The SBC then enters sleep mode. It will wake up as soon as any of the Lx input read the correct state.

Figure 59. Typical Sleep Current vs Temp and Batt



Voltage

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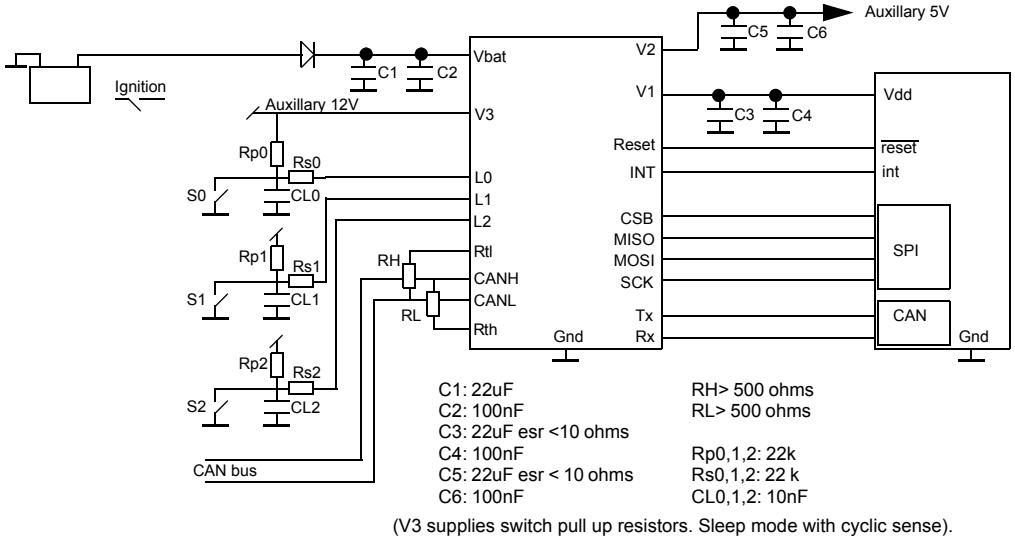
Figure 60. Typical Application Schematic 1



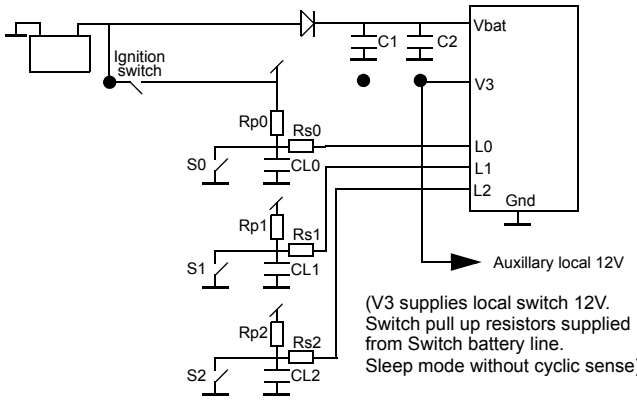
C1: 22uF
C2: 100nF
C3: 22uF esr <10 ohms
C4: 100nF
C5: 22uF esr < 10 ohms
C6: 100nF

RH> 500 ohms
RL> 500 ohms

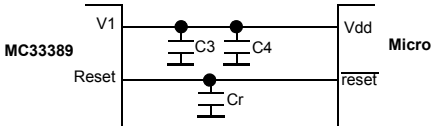
Rp0,1,2: 22k
Rs0,1,2: 22 k
CL0,1,2: 10nF

(V3 supplies switch pull up resistors. Sleep mode with cyclic sense).

Figure 61. Typical Application: V3 used as auxilaary ECU supply - Reset Duration Extension

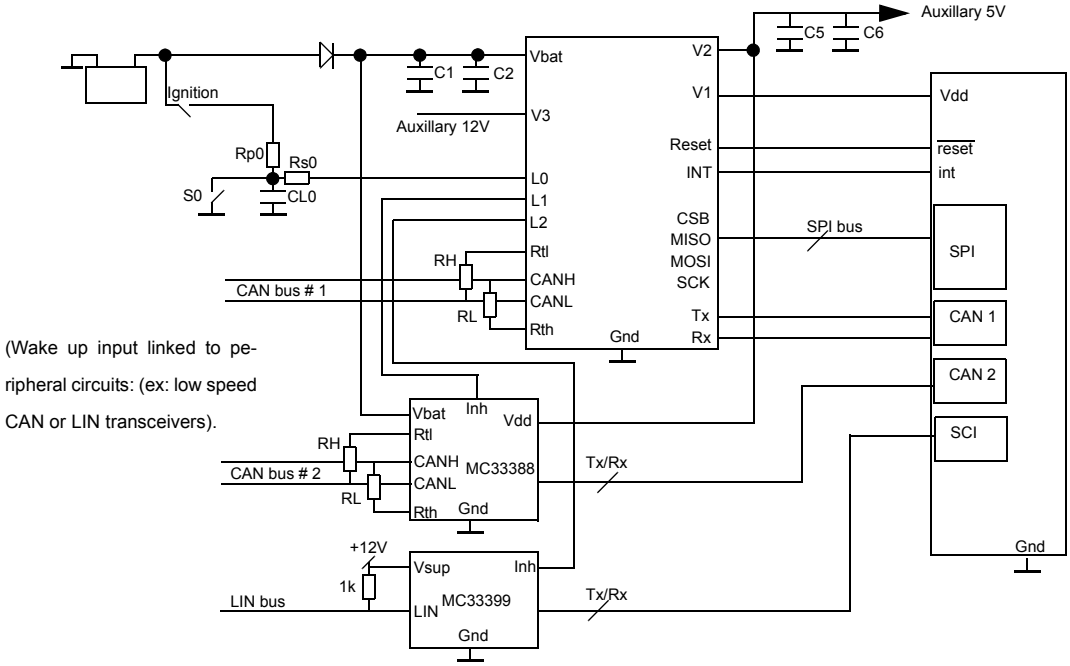


(V3 supplies local switch 12V.
Switch pull up resistors supplied
from Switch battery line.
Sleep mode without cyclic sense).



Reset duration extension

Figure 62. Typical Application Schematic



(Wake up input linked to peripheral circuits: (ex: low speed CAN or LIN transceivers).

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The SBC offers several capabilities to help user debug its application.

- External bias of V1 and reset pin.
- Turn off of the software watchdog in standby mode.
- Special debug samples with software watchdog disable at power up (contact local Motorola representative).

Debug And Program Download Into Flash Memory

While the SBC is powered it enters normal request and expect within the 75ms time period of the NR mode an SPI tigger word (to enter normal mode and select the W/D time period). If this does not occurs, the SBC enter sleep mode and turn off V1.

When the software is been debug, and when using development tools, it is not always easy to make sure these events properly. It is thus possible to externally power the V1 line with an external 5V supply, and to force the Reset pin to V1 or to and external 5V. These can be done at nominal voltage and temperature. By doing this, 5V is provided to the MCU Vdd and reset lines.

Under this condition the SBC is not operational. However the reset pin is pulled low and is sinking 5mA to ground. This means that the external circuitry which drive reset must have a current capability higher than 5mA in order to drive the reset in high state.

Disable Of Software Watchdog In Standby Mode

The software watchdog can be disable in standby mode only. In order to disable it the following operation must be done:

- Write to MCR register: data 011 (bit 2, bit 1, bit 0)
- Write to MCVR register: data 011 (bit 2, bit 1, bit 0)

Then the SBC enters the standby mode without software watchdog. However the V2 can not be turn on, and the CAN cell can not be used.

Special Device

Special components are available to make the debug even easier. These device has a special behaviour which at power up disable the watchdog. These device can be available through marketing only. Contact local Motorola representative for more detail.

The behaviour of such special parts is as follow:

- At power up (from Vbat =0V), the SBC enters "normal request mode" and stays in this mode permanently. V1 is on, V2 and V3 off, CAN in Term Vbat. For reference, with MC33389ADW and MC33389CDH units it stays there 75ms only and go to sleep if no SPI.
- To get the SBC out on NormalRequest mode, write to SWCR register any valid data. This will enable the SBC to enter Normal mode, with V1 and V2 on. Once this is done, the SBC is controllable through SPI, in the same way as the normal versions. It can be turned in sleep. After wake up it enters NR mode (same as after power up described above).

Only difference is that there is no need to refresh the software watchdog. Internally, the watchdog is running but when time out elapsed a reset is not generated.

When application debug is advanced enough, it is possible to enable the W/D-reset function.

To re activated the W/D effect, the VSSR register, bit VBSR0 (bat fail) must be read (cleared). When this is done, the W/D and 75ms timer of the NR mode effects are activated.

However, due to re synchronisation, it is likely that at some point a reset is generated and that the SBC enter reset state then Normalrequest mode.

When the SBC has had it W/D reactivated it is not possible to deactivated it again by software. The only way to do this is to remove battery supply voltage (Vbat < 3V for more than 200us) and then power up the SBC.

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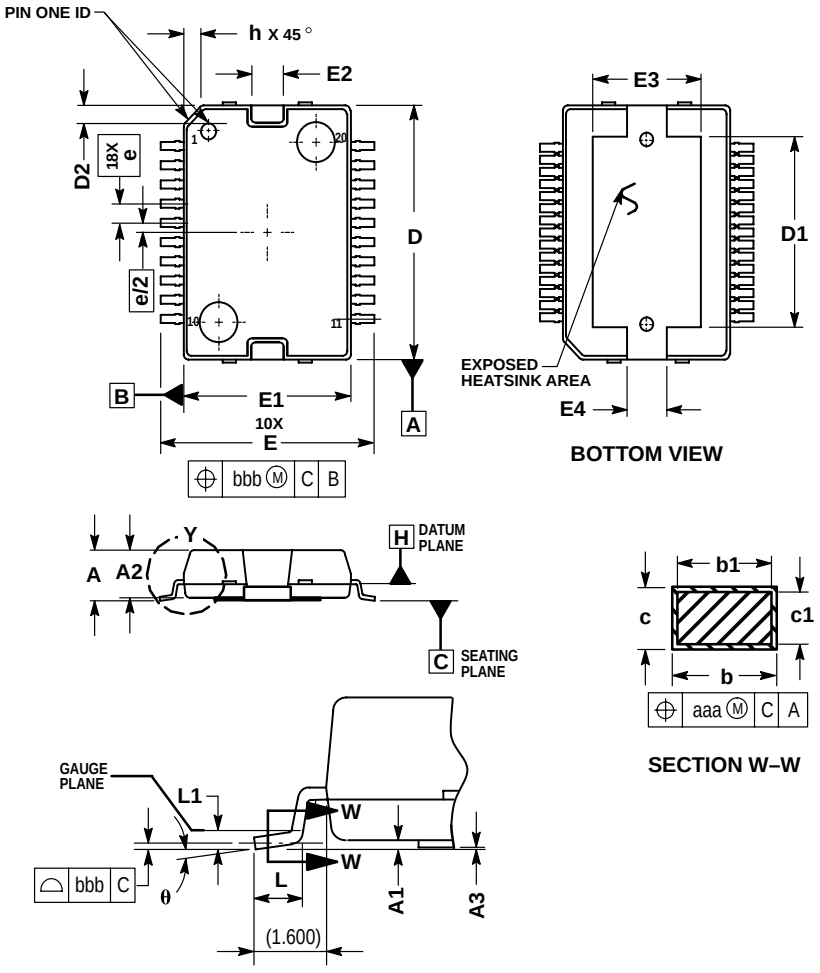

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	3.000	3.400
A1	0.100	0.300
A2	2.900	3.100
A3	0.00	0.100
D	15.800	16.000
D1	11.700	12.600
D2	0.900	1.100
E	13.950	14.450
E1	10.900	11.100
E2	2.500	2.700
E3	6.400	7.200
E4	2.700	2.900
L	0.840	1.100
L1	0.350 BSC	
b	0.400	0.520
b1	0.400	0.482
c	0.230	0.320
c1	0.230	0.280
e	1.270 BSC	
h	—	1.100
θ	0 °	8 °
aaa	0.200	
bbb	0.100	

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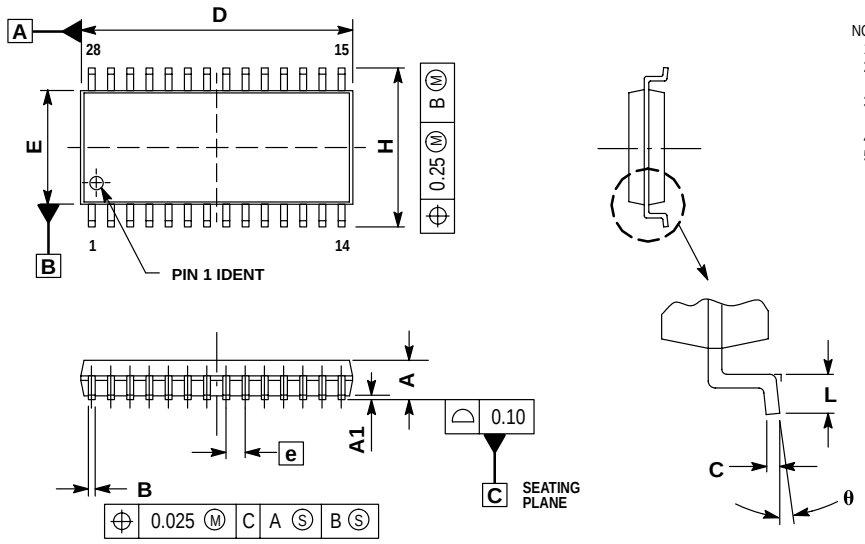

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0°	8°

CASE 751F–05
ISSUE F

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