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Technical Data

MC44BC373/374
Rev. 3.5, 7/2003

MC44BC373/374 Multi-Standard or PAL/NTSC Modulator with integrated antenna booster/splitter ICs

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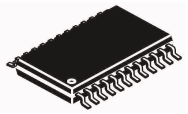
MC44BC373/374



TSSOP 24 Package

Ordering Information

Device	Temp Range	Package
MC44BC373DTB,R2 MC44BC374DTB,R2	−10°C to +80°C	TSSOP24
NOTE: For tape and reel, add R2 suffix.		

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These modulator ICs are for use in VCRs, games, set-top boxes, and similar devices. Figure 1 shows the pin connections.

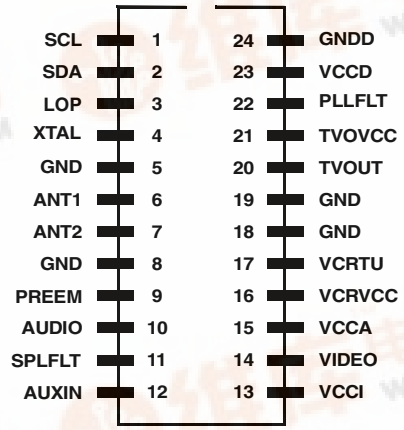

Figure 1. MC44BC373/374 Pin Connections

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1 Features

MC44BC373: Multi-Standard PAL/SECAM/NTSC with integrated booster splitter

MC44BC374: PAL/NTSC with integrated booster splitter

The channel is set by an on-chip high-speed I^2C compatible bus receiver. A Phase-Locked Loop (PLL) tunes the modulator over the full UHF range. The modulator incorporates a sound subcarrier oscillator and uses a second PLL to derive 4.5, 5.5, 6.0, and 6.5MHz subcarrier frequencies. These frequencies are selected using the bus.

The picture-to-sound ratio is adjusted using the bus. In addition, an on-chip video test pattern generator can be switched ON using a 1kHz audio test signal.

Along with the modulator functions, an Antenna Booster/Splitter function is included.

These modulator versions are completely pin-to-pin and software compatible and all versions have the following features.

- No external varicaps diodes/inductors or tuned components
- Channel 21–69 UHF operation
- VHF range possible by internal dividers (30MHz to 450MHz)
- Integrated on-chip programmable UHF oscillator
- Extremely low external component count
- High-speed read and write I^2C-bus compatible (800kHz)
- Fixed video modulation depth (80% in PAL and 90% in SECAM)
- Peak White Clip disabled using the bus
- Programmable picture/sound carrier ratio (12dB and 16dB)
- Integrated on-chip programmable sound subcarrier oscillator (4.5MHz to 6.5MHz)—No external varicaps
- On-chip video test pattern generator with sound test signal (1kHz)
- Low-power programmable modulator standby mode (booster active)
- Transient output inhibit during PLL Lock-up at Power-ON
- Logical Output Port controlled by bus
- Integrated Antenna Booster/Splitter (40MHz to 860MHz)
- Custom masked versions with unique start-up settings possible (no I^2C bus programming required)
- Extremely robust ESD protection, minimum 4kV, typical 6kV

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2 Device Overview

Figure 2 shows a simplified block diagram of the MC44BC373/4 device.

The MC44BC373/374 device contains four main sections:

1. A high-speed I^2C-compatible bus section.
2. A PLL section — Synthesizes the UHF/VHF output channel frequency (from an integrated UHF oscillator, divided for VHF output).
3. A modulator section — Accepts audio and video inputs and then uses those inputs to modulate the UHF/VHF carrier.
4. An Antenna Booster/Splitter — Amplifies and splits the antenna signal into two signals:
   a) The modulated signal is added to the amplified antenna signal on the TVOUT pin.
   a)

The following items are programmable using the high-speed I^2C compatible bus:

- Channel frequency
- Sound frequency
- Sound/picture carrier ratio

An on-chip video test pattern generator with an audio test signal is included.

The MC44BC373 operates as a multi-standard modulator and can handle the following systems using the same external circuit components:

- B/G
- I
- D/K
- H
- L
- M/N

The high frequency BiCMOS technology permits integration of the following functions:

- Antenna Booster/Splitter
- UHF tank circuit and certain filtering

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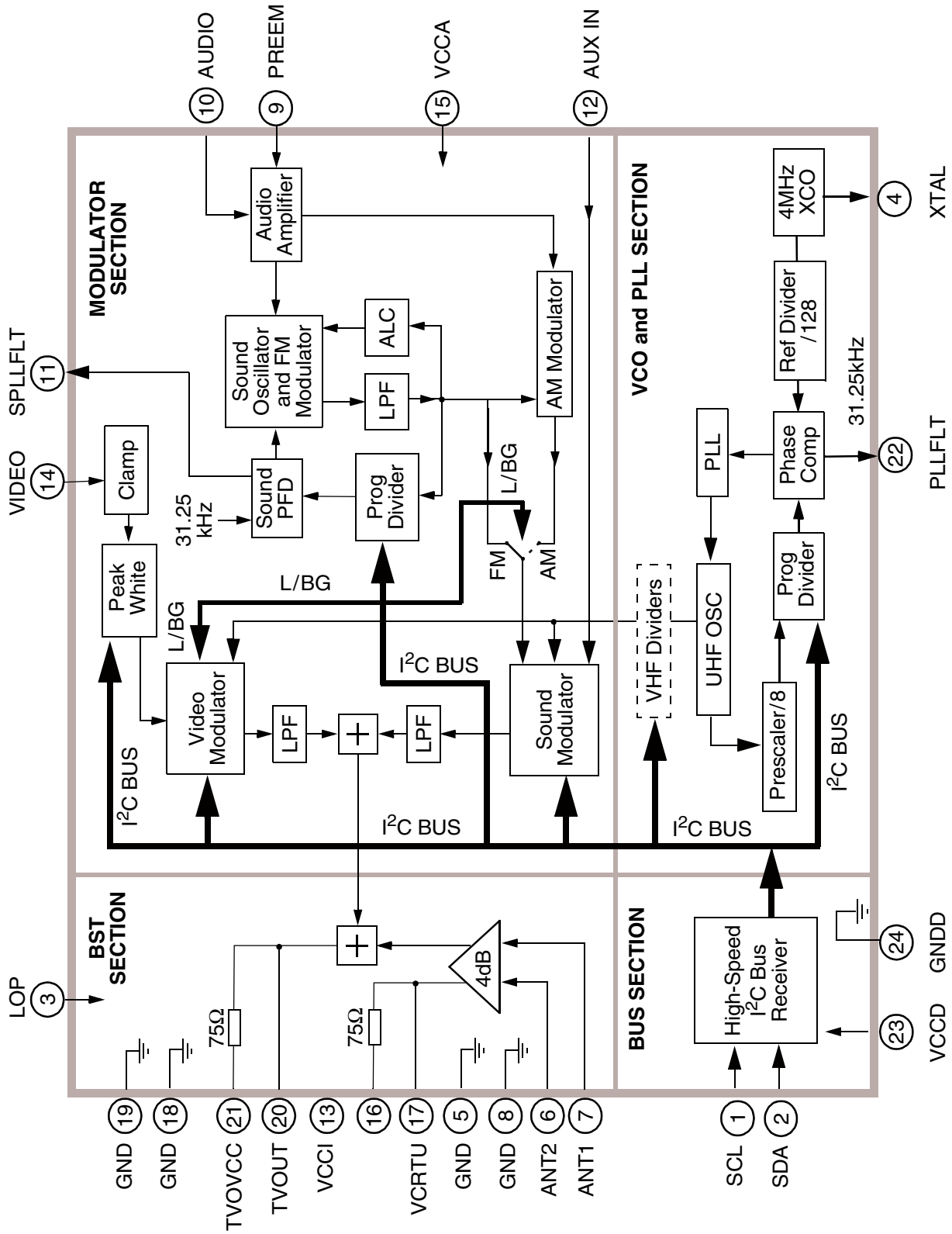

Figure 2. Simplified Block Diagram—MC44BC373/374

3 Maximum Ratings

Sym	Parameter	Value	Unit
Vcc1	Supply Voltage	6	V
Tamin	Minimum Operating Ambient Temperature	–10	°C
Tamax	Maximum Operating Ambient Temperature	75	°C
Tstgmin	Minimum Storage Temperature	–65	°C
Tstgmax	Maximum Storage Temperature	150	°C

This device contains protection circuitry to guard against damage due to high static voltage or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, input and output voltages should be constrained to the ranges indicated in the Recommended Operating Conditions.

Maximum ratings are those values beyond which damage to the device may occur. For functional operation, voltage should be restricted to the Recommended Operating Condition.

4 Electrostatic Discharge

Sym	Parameter	Min	Typ	Unit
ESD	HBM (Human Body Model)—MIL-STD-883C, Method 3015-7	4000	6000	V

5 Electrical Characteristics

- A = 100% Tested
- B = 100% Correlation tested
- C = Characterized on samples
- D = Design parameter

5.1 Specification Conditions

Unless otherwise stated: V_{cc} = 5.0 V, Ambient Temperature = 25°C, Video Input $1V_{p-p}$, 10-step grayscale. RF inputs/outputs into 75 Ohm load. SPECIFICATIONS ONLY VALID FOR ENVELOPE DEMODULATION.

Parameter	Min	Typ	Max	Unit	Notes	Type
Operating supply voltage range	4.5	5.0	5.5	V		B
Total supply current	65	75	88		All sections active	A
Total standby mode supply current	26	34	40	mA	OSC, SO, ATT=1 Bus Section active	A
Test pattern sync pulse width	3	4.7	6.5	µS		B
Sound comparator charge pump current During locking When locked	 7 0.7	 10 1	 12 1.5	 µA µA		 A A
RF comparator charge pump current	60	100	150	µA		A
Crystal oscillator stability-negative resistance	1	—	—	KΩ		D
Logic Output Port Saturation voltage at I=2mA Leakage current	 — —	 160 —	 300 1	 mV µA		 A A

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6 I²C Bit Mapping

WRITE MODE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK
CA-CHIP ADDRESS	1	1	0	0	1	0	1	0	ACK
C1-High Order Bits	1	AUX	SO	LOP	PS	X3	X2	SYSL	ACK
C0-Low Order Bits	PWC	OSC	ATT	SFD1	SFD0	TB1	X5	X4	ACK
FM-High Order Bits	0	TPEN	N11	N10	N9	N8	N7	N6	ACK
FL-Low Order Bits	N5	N4	N3	N2	N1	N0	X1	X0	ACK

READ MODE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK
CHIP ADDRESS	1	1	0	0	1	0	1	1	ACK
R-Status Byte	—	—	—	—	—	Y2	Y1	OOR	—

Bit Name	Description
PWC	Peak White Clip enable/disable.
OSC	UHF oscillator ON/OFF.
ATT	Modulator output attenuated-sound and video modulators ON/OFF.
SFD0, 1	Sound subcarrier frequency control bits.
TB1	Test mode bit—bus format compatible with MC44353.
AUX	Auxiliary sound input enable/disable.
SO	Sound Oscillator ON/OFF.
LOP	Logic Output Port.
PS	Picture-to-Sound carrier ratio.
SYSL	System L enable—selects AM sound and positive video modulation (MC44BC373/ only).
TPEN	Test pattern enable—picture and sound.
X5…X0	Test mode bits—All bits are 0 for normal operation (see Test Mode tables, page 7 & page 8).
N0…N11	UHF frequency programming bits, in steps of 250kHz.
OOR	RF oscillator out-of-frequency range information.
Y1, Y2	RF oscillator operating range information.

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7 I²C Programming

Sound

SFD1	SFD0	Sound Subcarrier Freq (MHz)
0	0	4.5
0	1	5.5
1	0	6.0
1	1	6.5

PS	Picture-to-Sound Ratio (dB)
0	12
1	16

SO	Sound Oscillator
0	Sound oscillator ON (normal mode).
1	Sound oscillation disabled (oscillator and PLL section bias turned OFF).

AUX	Auxiliary Audio Input
0	AUX input disabled (normal mode).
1	AUX input enabled.

Video

SYSL	System L and B/G Selection MC44BC373 only
0	System B/G enabled, System L disabled (FM sound and negative video modulation).
1	System L enabled, System B/G disabled (AM sound and positive video modulation).

PWC	Peak White Clip
0	Peak White Clip ON (System B/G).
1	Peak White Clip OFF (System L).

TPEN	Test Pattern Signal
0	Test pattern signal OFF (normal operation).

WRITE MODE: Test Mode 1 and VHF Range

X2	X1	X0	State	Description
0	0	0	1.a	Normal operation.
0	0	1	1.b	RF frequency divided for low frequency testing or VHF range: RF/2
0	1	0	1.c	RF/4
0	1	1	1.d	RF/8
1	0	0	1.e	RF/16
1	0	1	1.f	DC drive applied to modulators: non-inverted video at TVOUT.
1	1	0	1.g	DC drive applied to modulators: inverted video at TVOUT.
1	1	1	1.h	Transient output inhibit disabled.

UHF

OSC	UHF Oscillator
0	Normal operation.
1	UHF oscillator disabled (oscillator and PLL sections bias turned OFF).

ATT	Modulator Output Attenuation
0	Normal operation.
1	Modulator output attenuation (sound and video modulators sections bias turned OFF).

Standby Mode

OSC	SO	ATT	Combination of 3-bits
1	1	1	Modulator standby mode (sound and UHF oscillator, sound and video modulator section bias turned OFF, and I²C bus section standby mode)—BST is active.

MC44353/4/5 Compatibility

TB1	Description
0	Normal mode (fully programmable).
1	Limited programmability and compatibility with MC44353.

Logic Output Port

LOP	Description
0	Pin 3 is low voltage.
1	Pin 3 is high impedance.

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WRITE MODE: Test Mode 2

X5	X4	X3	State	Description
0	0	0	2.a	Normal operation.
0	0	1	2.b	Test pattern generator DC verification (Test pattern DC test mode available).
0	1	0	2.c	Programmable divider test (UHF programmable divider on PLLFILT pin and sound programmable divider on SPLLFIL pin).
0	1	1	2.d	Reference divider test (UHF reference divider on PLLFILT pin).
1	0	0	2.e	UHF phase comparator, upper source on PLLFILT pin. Sound phase comparator 10μA upper source on SPLLFIL (only valid during Transient Output Inhibit).
1	0	1	2.f	UHF phase comparator, lower source on PLLFILT pin. Sound phase comparator 10μA lower source on SPLLFIL (only valid during Transient Output Inhibit).
1	1	0	2.g	Sound phase comparator 1μA upper source on SPLLFIL (not valid during Transient Output Inhibit).
1	1	1	2.h	Sound phase comparator 1μA lower source on SPLLFIL (not valid during Transient Output Inhibit).

READ MODE

OOR	Description
0	Normal operation, VCO in range.
1	VCO out-of-range.

Y1	Description
0	VCO out-of-range, frequency too low, only valid if OOR=1.
1	VCO out-of-range, frequency too high, only valid if OOR=1.

Y2	Description
0	High VCO is active.
1	Low VCO is active.

8 Modulator High Frequency Characteristics

Unless otherwise stated: V_{cc}=5.0V, Ambient Temperature=25°C, Video Input $1V_{p-p}$, 10-step grayscale. RF inputs/outputs into 75Ohm load. SPECIFICATIONS VALID ONLY FOR ENVELOPE DEMODULATION.

Parameter	Test Conditions	Min	Typ	Max	Unit	Type
TVOUT output level	Output signal from modulator section. See Figure 3.	73	74.5	77	dBµV	B
UHF oscillator frequency	—	460	—	880	MHz	A
VHF range	From UHF oscillator internally divided.	45	—	460	MHz	B
TVOUT output attenuation	During transient output inhibit, or when ATT bit is set to 1. See Figure 3.	50	60	—	dBc	B
Sound subcarrier harmonics (Fp+n∗Fs)	Reference picture carrier.	—	–63	–58	dBc	C
Second harmonic of chroma subcarrier	Using red EBU bar.	–65	—	—	dBc	C
Chroma/Sound intermodulation: Fp+(Fsnd–Fchr)	Using red EBU bar.	–65	—	—	dBc	C
Fo (picture carrier) harmonics	2nd harmonic: CH21 3rd harmonic: CH21 Other channels: See Figure 3. See NOTE 1.	30 20	35 26	— —	dBc	C
Out band (picture carrier) spurious	1/2∗Fo–1/4∗Fo–3/2∗Fo–3/4∗Fo From 40MHz to 1GHz.	—	0	10	dBµV	C
In band spurious (Fo 5MHz)	No video sound modulation.	—	—	60	dBc	C
NOTE 1: Picture carrier harmonics are highly dependant on printed circuit board layout and decoupling capacitors.						

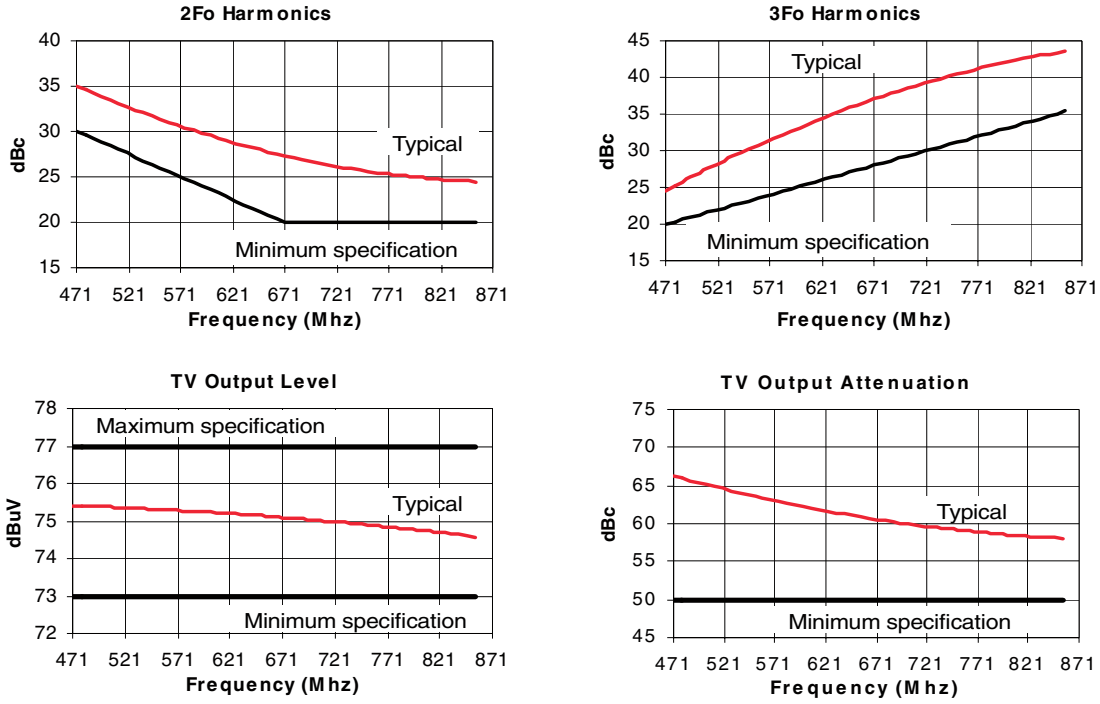

Figure 3. Typical Performance—Modulator High Frequency

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9 Video Characteristics

Unless otherwise stated: V_{cc} = 5.0 V, Ambient Temperature = 25 °C, Video Input 1 V_{p-p}, 10-step grayscale. RF inputs/outputs into 75 Ohm load. SPECIFICATIONS VALID ONLY FOR ENVELOPE DEMODULATION.

Parameter	Test Conditions	Min	Typ	Max	Unit	Type
Video bandwidth	Reference 0 dB at 100 kHz, measured at 5 MHz.	–1.5	–0.8	—	dB	C
Video input level	75 Ohm load.	—	—	1.5	Vcvbs	D
Video input current	—	—	0.2	1	µA	A
Video input impedance	—	500	—	—	KΩ	A
Peak White Clip	PWC bit set to 1, see PWC section.	110	114	118	%	A
Video S/N	See Figure 4.	50	53	—	dB	C
Differential Phase	See Figure 4.	–5	—	5	deg	C
Differential Gain	On line CCIR 310, worst of first 4 out of 5 steps. See Figure 4.	–5	—	5	%	C
Luma/Sync ratio	Input ratio 7.0 : 3.0	6.8/3.2	—	7.2/2.8	—	B
PAL video modulation depth	—	75	81	88	%	B
SECAM video modulation depth	—	88	93	99	%	B

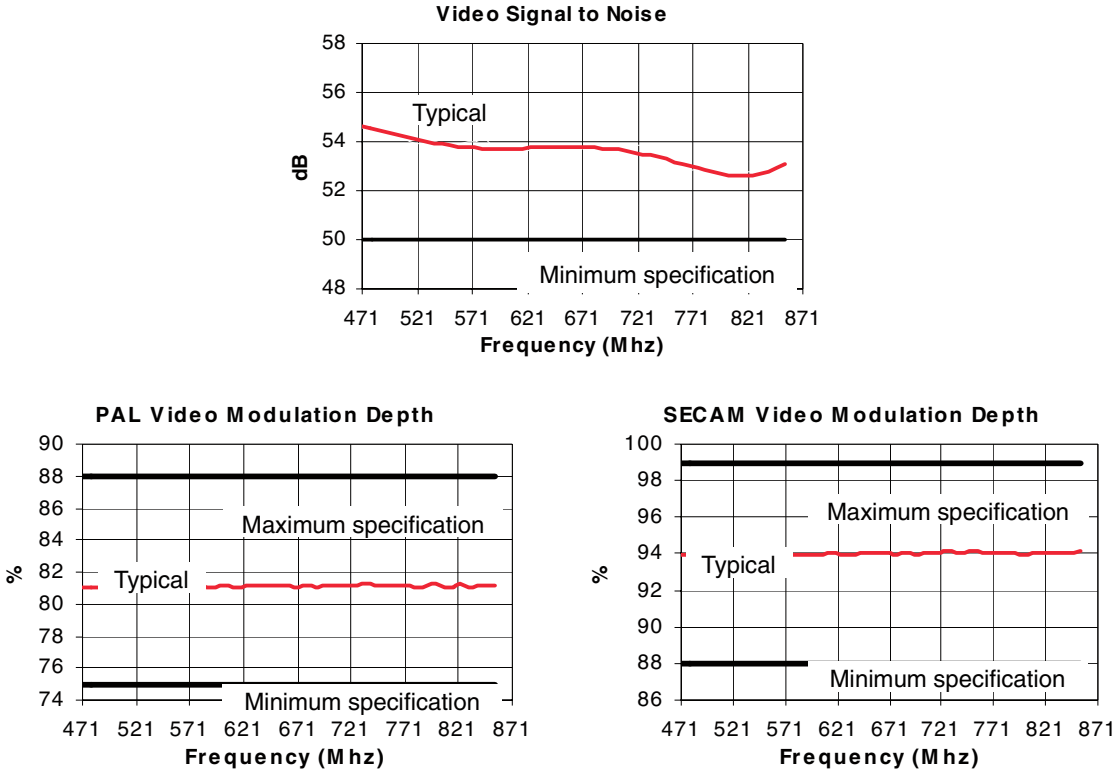

Figure 4. Typical Performance—Video

10 Audio Characteristics

Unless otherwise stated: V_{cc} = 5.0 V, Ambient Temperature = 25 °C, Video Input 1 V_{p-p}, 10-step grayscale. RF inputs/outputs into 75 Ohm load. SPECIFICATIONS VALID ONLY FOR ENVELOPE DEMODULATION.

Parameter	Test Conditions	Min	Typ	Max	Unit	Type
Picture-to-Sound ratio	PS bit set to 0. PS bit set to 1.	13 9	16 12	19 15	dB	B
Audio modulation depth	Using specific pre-emphasis circuit, audio input level = 205 mVrms – audio frequency = 1 kHz					
	AM modulation: SECAM Fs = 6.5 MHz	65	80	95	%	B
	FM modulation: Fs = 5.5, 6 or 6.5 MHz 100% modulation = ±50 kHz FM deviation	65	80	95	%	B
	FM modulation: NTSC Fs = 4.5 MHz 100% modulation = ±25 kHz FM deviation	65	80	95	%	B
Audio input resistance	—	45	53	61	KΩ	A
Audio Frequency response	Reference 0 dB at 1 kHz, using specified pre-emphasis circuit, measure from 50 Hz to 15 kHz.	–2.5	—	+2	dB	C
Audio Distortion FM (THD only)	At 1 kHz, 100% modulation (±50 kHz). No video.	—	0.4	2	%	C
Audio Distortion AM (THD only)	At 1 kHz, 100% modulation. No video.	—	1.5	2.5	%	D
Audio S/N with Sync Buzz FM	Video input EBU color bar 75%. Weighting filter CCIR 468-2.	48	53	—	dB	C
Audio S/N with Sync Buzz AM	Reference 1 kHz, 85% modulation. Video input EBU color bar 75%. Audio BW from 40 Hz to 15 kHz. Weighting filter CCIR 468-2.	45	50	—	dB	D

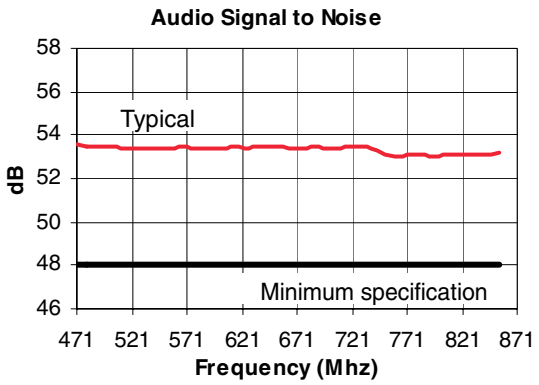

Figure 5. Typical performance—Audio

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11 Antenna Booster/Splitter Characteristics

Unless otherwise stated: V_{cc} = 5.0 V, Ambient Temperature = 25 °C, RF inputs/outputs into 75 Ohm load. All specifications use a BALUN at ANT1 & 2 inputs, assuming 0.8 dB losses MAX from 40 MHz to 860 MHz.

Parameter	Test Conditions	Min	Typ	Max	Unit	Type
Frequency range	—	40	—	860	MHz	C
Gain	ANT1, 2 to VCRTU. ANT1, 2 to TVOUT.	— —	4 4	— —	dB dB	B B
Gain flatness	40 to 860 MHz.	−1.5		+1.5	dB	C
Noise figure	ANT1, 2 to VCRTU and TVOUT. Modulator in standby mode.	5.5	7.5	9.5	dB	C
Noise figure	ANT1, 2 to VCRTU and TVOUT. Modulator in normal mode (ON).	6.5	8.5	10.5	dB	C
VSWR	All pins, BST bias ON. At TVout and VCRTU pins, BST bias OFF.	—	1.5	2.5	—	B
	At TVin pins, BST bias OFF.	—	2.5	3	—	B
Intermodulation (IMD)	Input level=90 dBuV. See IMD measurement section. F1+F2 IMD 2F1−F2, 2F2+F1, F1−F2 IMD	— —	55 60	47 50	dBc dBc	C C
Isolations	From TVOUT or VCR to ANT1, 2 TVOUT/VCRTU	48 30	60 45	— —	dBc dBc	C C

11.1 Typical Performance—Gain and Isolation

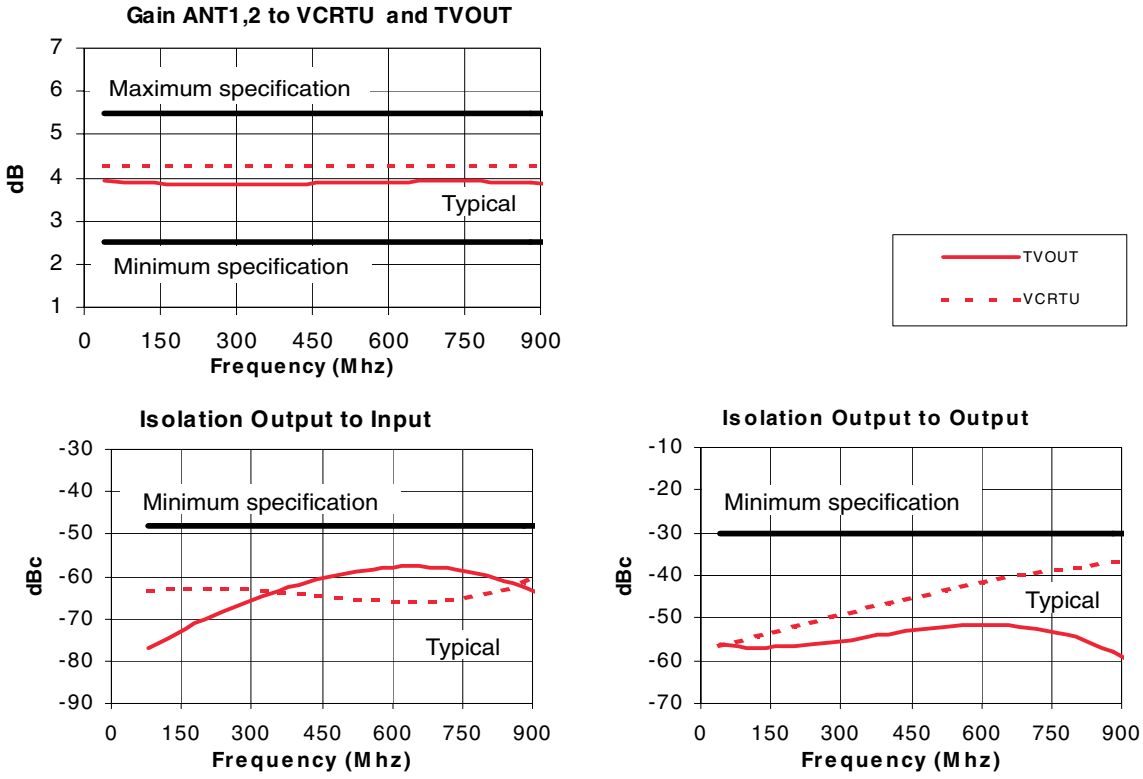

Figure 6. Typical Performance—Gain and Isolation

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11.2 Typical Performance—Noise Figure

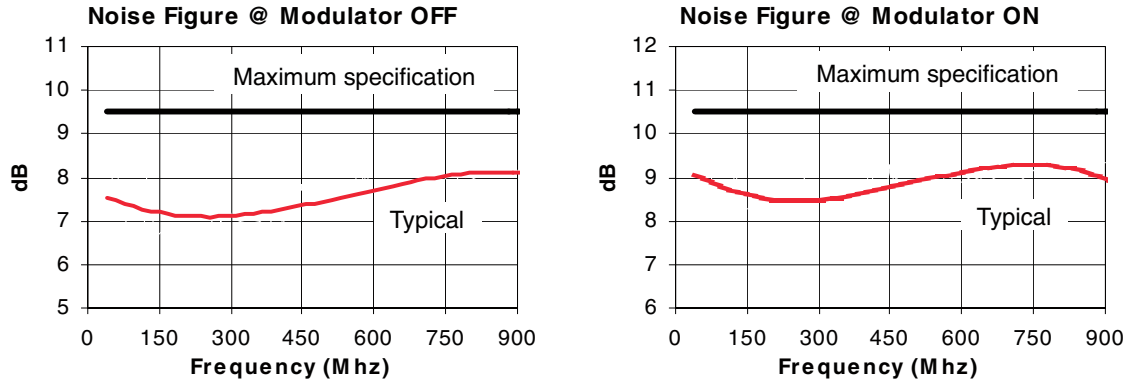

Figure 7. Typical Performance—Noise Figure

11.3 Intermodulation (IMD) Measurement

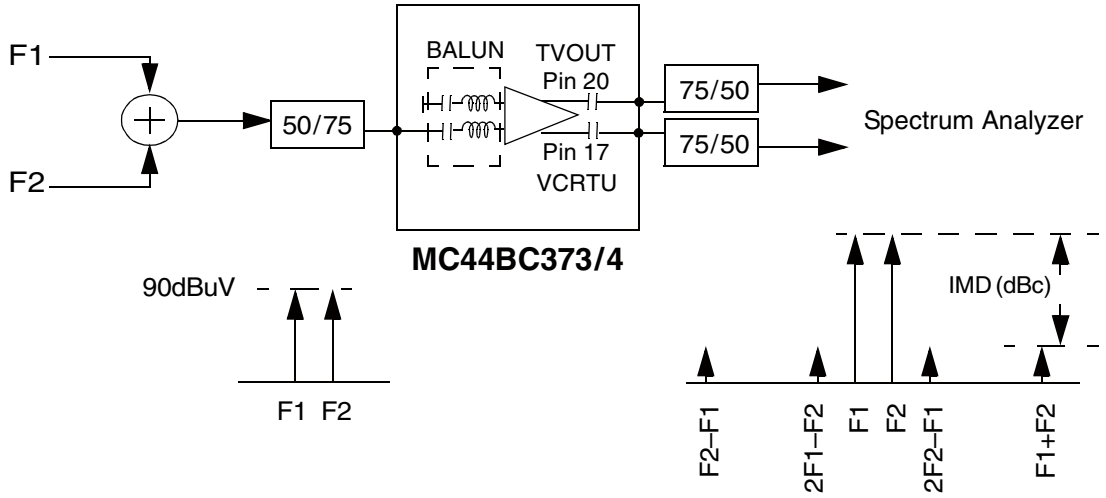

Figure 8. Intermodulation (IMD) Measurement

Intermodulation (IMD) frequencies are all frequency combinations coming from the two input carriers F1 and F2: F2−F1, 2∗F1−F2, 2∗F2−F1 and F1+F2, fall in the 40MHz–900MHz range.

F1 and F2 input levels are set to 90dBuV at the input of the BALUN. F1 and F2 frequency generator levels (50W internal load) take into account a 50 to 75Ohm load difference (1.8dB), plus losses in the 3dB coupler and the 50 to 75Ohm transformer.

Intermodulation measurement is the difference (in dBc) between the F1 or F2 level at the Output (VCRTU or TVOUT) and the frequency combinations level, for the following cases:

F1=50MHz and F2=60MHz	F1=100MHz and F2=110MHz	F1=200MHz and F2=210MHz
F1=300MHz and F2=310MHz	F1=400MHz and F2=410MHz	F1=500MHz and F2=510MHz
F1=600MHz and F2=610MHz	F1=700MHz and F2=710MHz	F1=800MHz and F2=810MHz

Intermodulation specification is the IMD measurement's worst case.

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12 Modulator Operation

12.1 Power-ON Settings

At power-ON, the MC44BC373 and MC44BC374 configuration is as follows:

WRITE MODE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK
C1—High Order Bits	1	0	0	0	0	0	0	0	ACK
C0—Low Order Bits	0	0	0	0	1	0	0	0	ACK
FM—High Order Bits	0	0	N11	N10	N9	N8	N7	N6	ACK
FL—Low Order Bits	N5	N4	N3	N2	N1	N0	0	0	ACK

Note: 1. N0 to N11 are set to have the UHF oscillator on channel 36 (591.25MHz).
Note: 2. Peak White Clip is ON.
Note: 3. Sound frequency is 5.5MHz.
Note: 4. Sound auxiliary input is disabled.
Note: 5. Logic Output Port is low voltage.
Note: 6. Picture-to-sound ratio is 12dB.

The settings indicated can be customized in the special masked version.

12.2 Power Supply

The five device Vcc pins (13, 15, 16, 21, 23) must be applied at the same time to ensure all internal blocks are correctly biased. All other pins must not be biased before Vcc is applied to the device. The printed circuit board layout of the Vcc supplies must be designed to ensure maximum isolation of the I/P to O/P and also between the two O/Ps.

12.3 Standby Mode

During standby mode, the modulator is switched to low power consumption; the sound oscillator, UHF oscillator, video and sound modulator sections bias are internally turned OFF.

The I^2C bus and booster sections remain active.

The modulator can be programmed in standby mode using a combination of three bits:

1. OSC=1
2. SO=1
3. ATT=1

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12.4 Test Bit TB1

This test bit allows an initial evaluation of MC44BC373 and MC44BC374 using software developed for MC443535:

- TB1= 0 — All MC44BC373/374 functions available—normal mode.
- TB1= 1 — Limited software compatibility with MC44353; MC44BC373/374 functions not available.

WRITE MODE[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK
CA-CHIP ADDRESS	1	1	0	0	1	0	1	0	ACK
C1-High Order Bits	1		—	—	PS	—	—	SYSL	ACK
C0-Low Order Bits	—	—	—	SFD1	SFD0	1	0	0	ACK
FM-High Order Bits	0	TPEN	N11	N10	N9	N8	N7	N6	ACK
FL-Low Order Bits	N5	N4	N3	N2	N1	N0	—	—	ACK

Note: 1. Case TB1=1, compatible with MC44353

Note: 2. All "—" are don't care bits.

Note: 3. PS bit replaces PSD2 bit in MC44353 bus format:
PS = 0 is for picture-to-sound ratio = 12dB,
PS = 1 is for picture-to-sound ratio = 16dB

Note: 4. SFD1 and SFD0 bits have the same definition for both bus formats (MC44353 and MC44BC373/374) and lets a sound frequency between 4.5MHz, 5MHz, 5.5MHz, and 6.5MHz be selected.

Note: 5. SYSL bit has same definition for bus formats MC44353 and MC44BC373/374; either system L or B/G is selectable.

Note: 6. All MC44BC373/374 functions are set to their default values.

12.5 System L or B/G Selection

SYSL bit internally switches the following functions:

- SYSL = 0; enables B/G system
  - — Video modulation polarity—Negative
  - — Video modulation depth—80% Typical (See Video Characteristics on page 10.)
  - — Sound modulation type—FM
- SYSL = 1; enables L system
  - — Video modulation polarity—Positive
  - — Video modulation depth—90% Typical (See Video Characteristics on page 10.)
  - — Sound modulation type—AM

12.6 Transient Output Inhibit

To minimize the risk of interference to other channels while the UHF PLL is acquiring a lock on the desired frequency, the Sound and Video modulators are turned OFF for each of the following two cases:

1. Power-ON from zero (i.e., all Vcc is switched from 0V to 5V).
2. UHF oscillator power-ON from OFF state (i.e., OSC bit is switched from 1 to 0)

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There is a time-out of 263ms until the output is enabled. This allows the UHF PLL settle to its programmed frequency. During the 263ms time-out, the sound PLL current source is set to 10µA typical, to speed up the locking time. After the 263ms time-out, the current source is switched to 1µA.

CAUTION:

Use care when selecting loop filter components, to ensure the loop transient does not exceed the specified delay.

For test purposes, it is possible to disable the 263ms delay using Test Mode1–State1.h.

12.7 Logic Output Port (LOP)

The LOP pin controls any logic function. The primary applications are to control an external attenuator or an external switch between the antenna input and TV output. When an external switch is controlled, the Booster function is not used.

The following figure shows a typical attenuator application with PIN diode. The LOP pin switches the PIN attenuator depending on the signal strength of the Antenna Input, thereby reducing the risks of Intermodulation in certain areas. The LOP may also be used as an OFF position bypass switch or for other logic functions in the application.

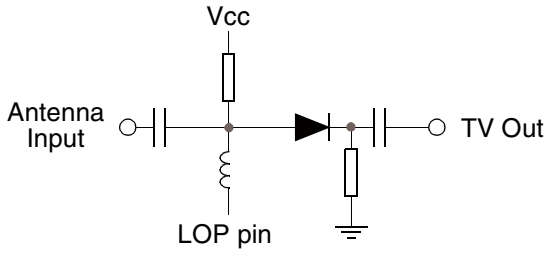

Figure 9. Attenuator Application with PIN Diode

12.8 Video Section—Peak White Clip

The modulator requires the following:

- A composite video input with “negative going” sync pulses
- A nominal level of 1Vp-p

This signal is AC-coupled to the video input where the sync tip level is clamped. The video signal is then passed to a Peak White Clip (PWC) circuit. The PWC circuit function sets to soft-clip the top of the video waveform, if the “sync tip amplitude” to “peak white clip” goes too high. This method avoids carrier over-modulation by the video. Clipping can be disabled by software.

12.9 Sound Section

The multivibrator oscillator is fully integrated and does not require external components. An internal low pass filter and matched structure provide a very low harmonics level.

The sound modulator system consists of an FM modulator incorporating the sound subcarrier oscillator, and an AM modulator. The audio input signal is AC coupled into the amplifier which then drives the two types of modulators.

The audio pre-emphasis circuit is a high-pass filter with an external capacitor and an internal resistor (100kOhms). The recommended capacitor value (470pF) is for BG standard. (50µS time constant.)

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The auxiliary audio input adds a sound subcarrier to the main carrier. The input can be a modulated NICAM carrier or a second sound subcarrier for a stereo system. Pin 12 is directly connected to the sound modulator input and the picture-to-sound ratio (P/S Ratio) depends on the auxiliary audio input level. (P/S ratio is 20dB for 35mVrms typical.)

12.10 Test Pattern Generator

A simple test pattern is generated on the IC which can be switched in under bus control to permit a TV receiver to easily tune in to the modulator output. The pattern consists of two white vertical bars on a black background and a 976Hz audio test signal.

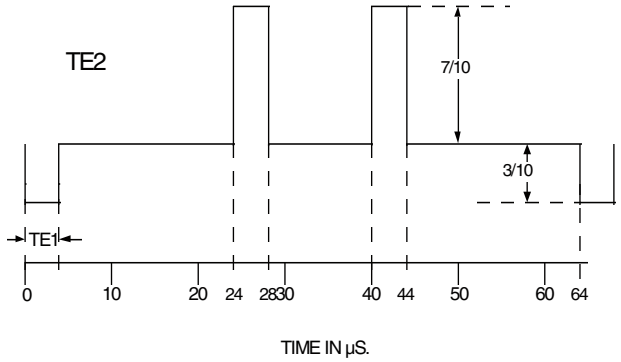

Figure 10. Test Pattern Generator—(Time in Seconds)

12.11 PLL Section

The reference divider is a fixed divide-by-128, resulting in a reference frequency of 31.25KHz with a 4.0MHz crystal. The 31.25KHz reference frequency is used for both UHF and Sound PLLs.

The prescaler is a fixed divide by 8 and is permanently engaged.

The programmable divider's division ratio is controlled by the state of control bits N0 to N11. The divider ratio N for a desired frequency F (in MHz) is provided by the following formulas:

$$N = \frac{F}{8} \times \frac{128}{4}$$

with:

$$N = 2048 \times N11 + 1024 \times N10 + \ldots\ldots + 4 \times N2 + 2 \times N1 + N0$$

12.12 UHF Oscillator—VHF Range

The UHF oscillator is fully integrated and does not require any external components. For low frequency testing or VHF range operation (test mode 1, states 1.b to 1.c), the UHF oscillator can be internally divided by 2, 4, 8, or 16.

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13 High-Speed I2C Compatible Bus

13.1 Specification Conditions

Unless otherwise specified, the Vcc1=5.0V and the ambient temperature (TA) =25°C.

Electrical Characteristics	Min	Typ	Max	Unit	Type
SDA/SCL output current at 0V	—	—	10	µA	A
SDA/SCL low input level	—	—	1.5	V	B
SDA/SCL high input level	3.0	—	—	V	B
SDA/SCL input current for input level from 0.4V to 0.3Vcc	−5	—	5	µA	C
SDA/SCL input level	0	—	Vcc+0,3	V	D
SDA/SCL capacitance	—	—	10	pF	C
ACK low output level (sinking 3mA)	—	0,3	1	V	A
ACK low output level (sinking 15mA)	—	—	1.5	V	C

Timing Characteristics	Min	Typ	Max	Unit	Type
Bus clock frequency	0	—	800	kHz	C
Bus free time between stop and start	200	—	—	ns	C
Setup time for start condition	500	—	—	ns	C
Hold time for start condition	500	—	—	ns	C
Data setup time	0	—	—	ns	C
Data hold time	0	—	—	ns	C
Setup time for stop condition	500	—	—	ns	C
Hold time for stop condition	500	—	—	ns	C
Acknowledge propagation delay	—	—	300	ns	C
SDA fall time at 3ma sink I and 130pF load	—	—	50	ns	C
SDA fall time at 3ma sink I and 400pF load	—	—	80	ns	C
SDA rise time SCL fall/rise time	— —	— —	300 300	ns ns	C C
Pulse width of spikes suppressed by the input filter	—	—	50	ns	C

13.2 Timing Definitions

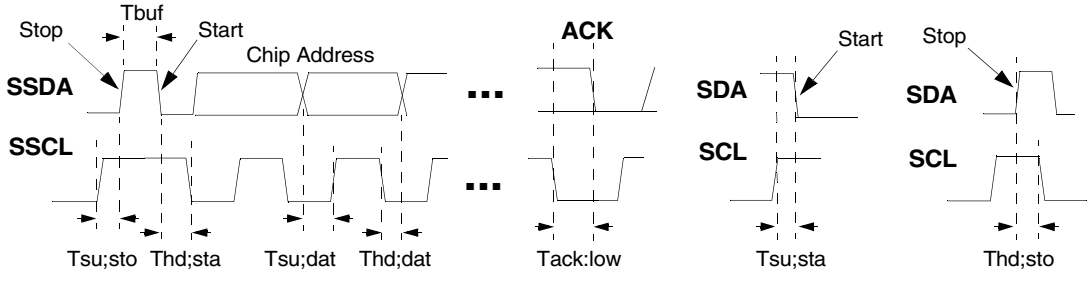

Figure 11. SSDA/SSCL Timing

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13.3 Levels Definition

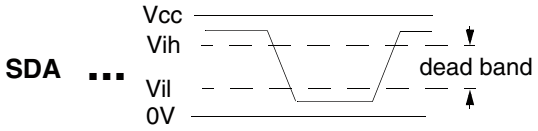

Figure 12. SDA Levels

13.4 High-Speed I²C Compatible Bus Format

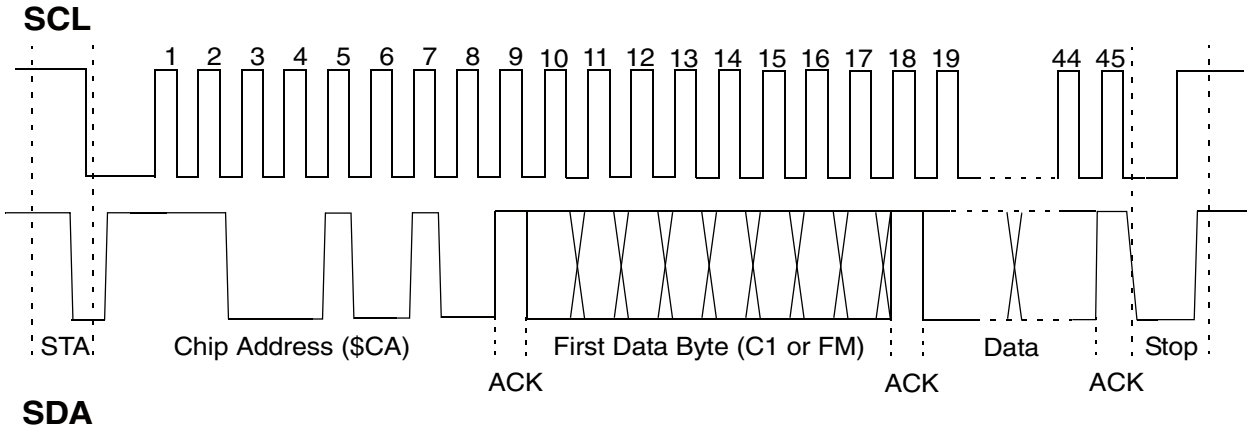

Figure 13. SCL and SDA Bus Timing

13.5 I²C Write Mode Format and Bus Receiver

The bus receiver operates the I²C compatible data format. The chip address (I²C bus) is:

1 1 0 0 1 0 1 0 (ACK) = $CA (hex) in write mode

In write mode, each ninth data bit (bits 9, 18, 27, 36, and 45) is an acknowledge bit (ACK) during which the MCU sends a logic 1 and the Modulator circuit answers on the data line by pulling it low. Besides the chip address, the circuit needs two or four data bytes for operation. The following data byte sequences are the permitted incoming information:

Example 1	STA	CA	C1	C0	STO		
Example 2	STA	CA	FM	FL	STO		
Example 3	STA	CA	C1	C0	FM	FL	STO
Example 4	STA	CA	FM	FL	C1	C0	STO

With:

STA = Start condition
CA = Chip Address
FM = Frequency information, high order bits
FL = Frequency information, low order bits
C1 = Control information, high order bits
CO = Control information, low order bits
STO = Stop condition

After the chip address, two or four data bytes may be received.

- If three (3) data bytes are received, the third one is ignored.
- If five (5) or more data bytes are received, the fifth and following ones are ignored, and the last ACK pulse is sent at the end of the fourth data byte.

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The first and third data bytes contain a function bit which lets the IC distinguish between frequency information and control information. If the function bit is a logic 1, the two following bytes contain control information. The first data byte after the chip address may be byte CO or byte FM. The two bytes of frequency information are preceded by a logic 0.

13.6 I²C Read Mode Format

The chip address (I^2C) is:

1 1 0 0 1 0 1 1 (ACK) = $CB (hex) in read mode

The incoming information consists of the read mode chip address byte. The device then answers with an ACK followed by one byte containing three bits of status information. No acknowledge is answered by the modulator after this byte.

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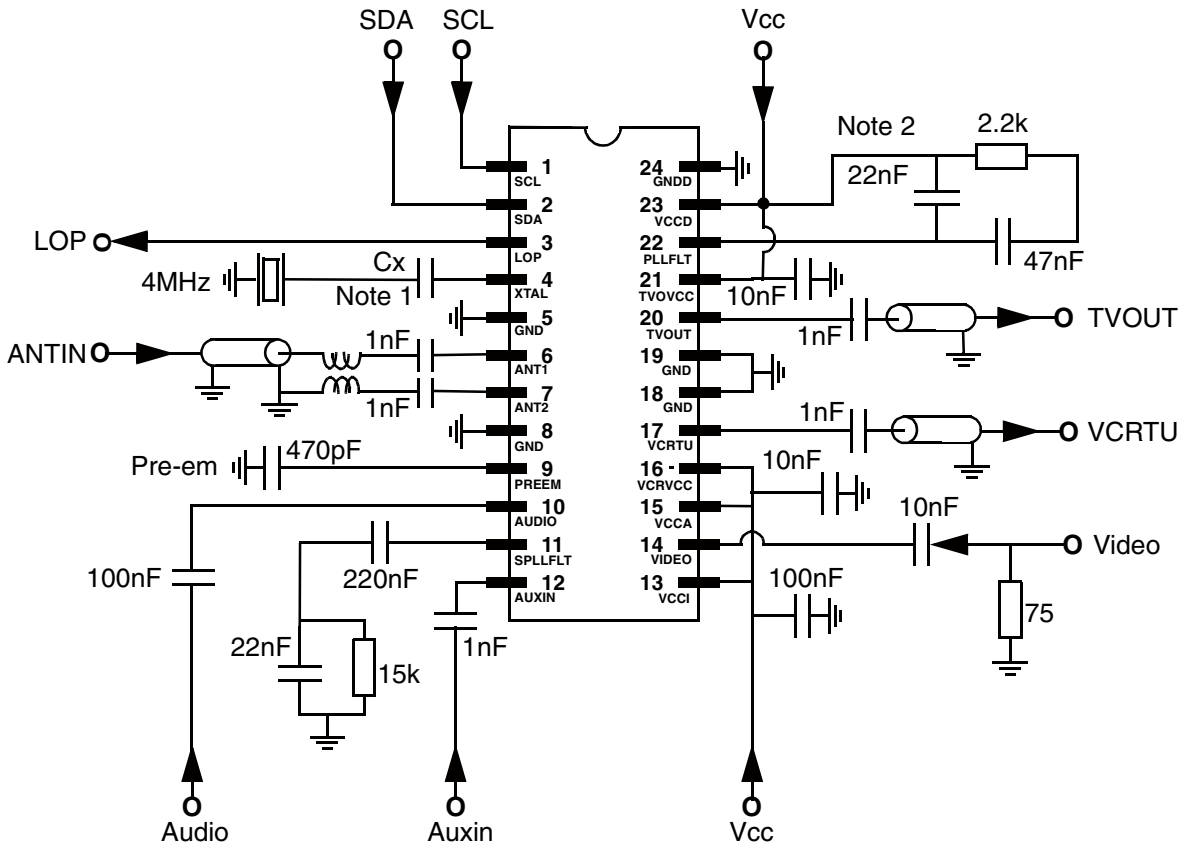
14 Application and Case Diagrams

Proposed BiCMOS Modulator and Booster/Splitter Application

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.



Note 1: Cx value depends on crystal characteristics; Cx = 27pF on Motorola application board.
Note 2: Loop filter components must be as close as possible to pins 22 and 23.

Figure 14. Proposed BiCMOS Modulator and Booster/Splitter Application

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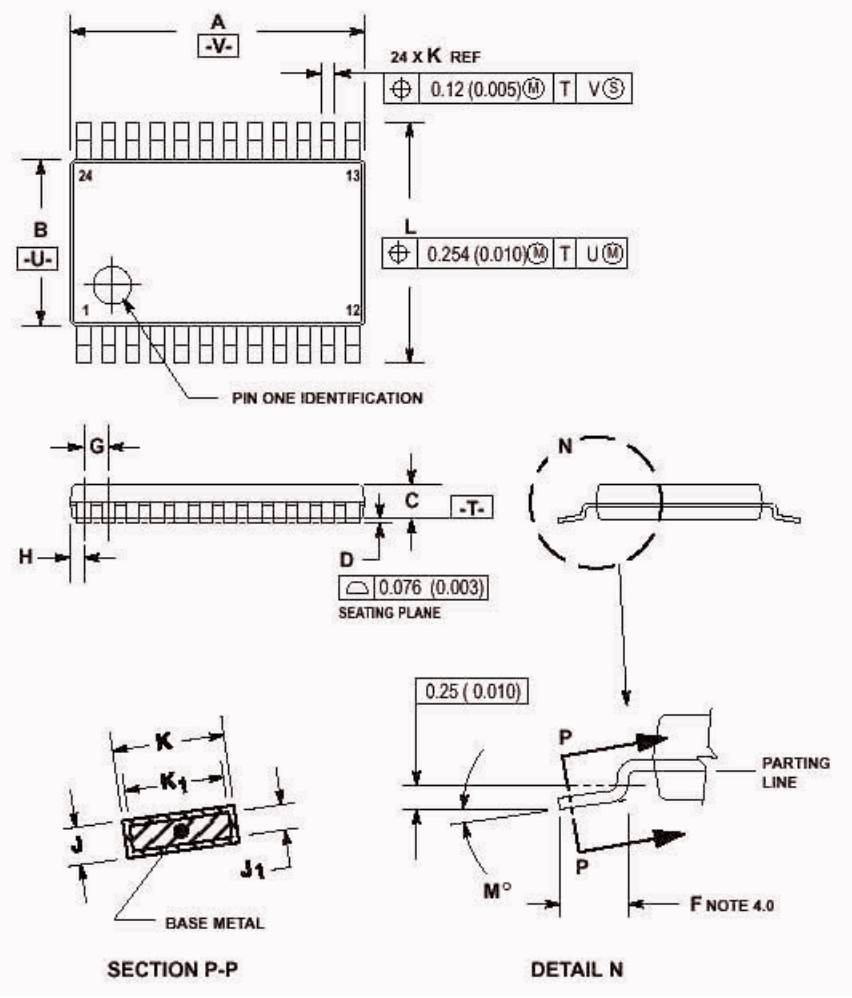

CASE 940H-02 ISSUE A

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	7.70	7.90	0.303	0.311
B	4.30	4.48	0.169	0.176
C	—	0.95	—	0.037
D	0.05	0.15	0.002	0.006
F	0.51	0.71	0.020	0.028
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.18	0.003	0.007
J1	0.09	0.13	0.003	0.005
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.25	6.50	0.246	0.256
M	0°	8°	0°	8°

Note: 1. Dimensioning and Tolerancing per ANSI Y14.5M, 1982.

Note: 2. Controlling dimension: Millimeters.

Note: 3. Dimensions A and B do not include mold flash or protrusions and are measured at the parting line. Mold flash or protrusions shall not exceed 0.15 (0.006) per side.

Note: 4. Dimension is the length of terminal for soldering to a substrate.

Note: 5. Terminal positions are shown for reference only.

Note: 6. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 (0.003) total in excess of the lead width dimension at maximum material condition. Dambar can not be located on the lower radius or the foot. Minimum space between protrusions and adjacent lead to be 0.14 (0.006).

Figure 15. TSSOP24 Package

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NOTES

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