

# Quad Analog Switch/ Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

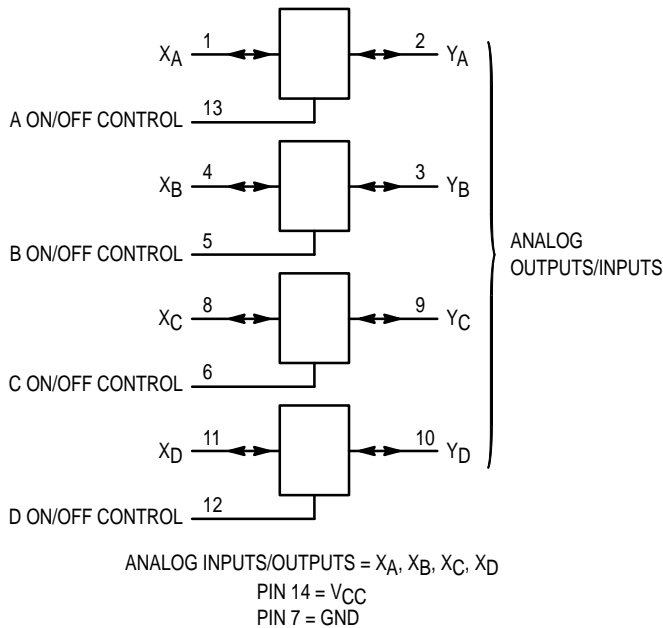
The MC54/74HC4016 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from  $V_{CC}$  to GND).

The HC4016 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances ( $R_{ON}$ ) are much more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

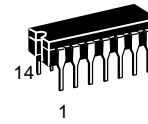
This device is identical in both function and pinout to the HC4066. The ON/OFF Control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316. For analog switches with lower  $R_{ON}$  characteristics, use the HC4066.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Analog Input Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 32 FETs or 8 Equivalent Gates

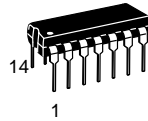
### LOGIC DIAGRAM



## MC54/74HC4016



**J SUFFIX**  
CERAMIC PACKAGE  
CASE 632-08



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06

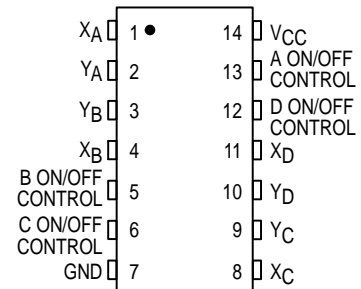


**D SUFFIX**  
SOIC PACKAGE  
CASE 751A-03

### ORDERING INFORMATION

MC54HCXXXXJ	Ceramic
MC74HCXXXXN	Plastic
MC74HCXXXXD	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND)	- 0.5 to + 14.0	V
V <sub>IS</sub>	Analog Input Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>in</sub>	Digital Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
Ceramic DIP: - 10 mW/°C from 100° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V	
V <sub>IS</sub>	Analog Input Voltage (Referenced to GND)	GND	V <sub>CC</sub>	V	
V <sub>in</sub>	Digital Input Voltage (Referenced to GND)	GND	V <sub>CC</sub>	V	
V <sub>IO</sub> *	Static or Dynamic Voltage Across Switch	—	1.2	V	
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 9.0 V V <sub>CC</sub> = 12.0 V	0 0 0 0	1000 500 400 250	ns

\* For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

**DC ELECTRICAL CHARACTERISTICS** Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Voltage ON/OFF Control Inputs	R <sub>on</sub> = per spec	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			9.0	6.3	6.3	6.3	
			12.0	8.4	8.4	8.4	
V <sub>IL</sub>	Maximum Low-Level Voltage ON/OFF Control Inputs	R <sub>on</sub> = per spec	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			9.0	1.8	1.8	1.8	
			12.0	2.4	2.4	2.4	
I <sub>in</sub>	Maximum Input Leakage Current, ON/OFF Control Inputs	V <sub>in</sub> = V <sub>CC</sub> or GND	12.0	±0.1	±1.0	±1.0	µA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND V <sub>IO</sub> = 0 V	6.0	2	20	40	µA
			12.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**DC ELECTRICAL CHARACTERISTICS** Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
R <sub>on</sub>	Maximum "ON" Resistance	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to GND I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0†	—	—	—	Ω
			4.5	320	400	480	
			9.0	170	215	255	
			12.0	170	215	255	
		V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Endpoints) I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0	—	—	—	
			4.5	180	225	270	
			9.0	135	170	205	
			12.0	135	170	205	
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - GND) I <sub>S</sub> ≤ 2.0 mA	2.0	—	—	—	Ω
			4.5	30	35	40	
			9.0	20	25	30	
			12.0	20	25	30	
I <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> V <sub>IO</sub> = V <sub>CC</sub> or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I <sub>on</sub>	Maximum On-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V<sub>CC</sub> - GND) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** (C<sub>L</sub> = 50 pF, ON/OFF Control Inputs: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit	
			- 55 to 25°C	≤ 85°C	≤ 125°C		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0	50	65	75	ns	
		4.5	10	13	15		
		9.0	10	13	15		
		12.0	10	13	15		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	150	190	225	ns	
		4.5	30	38	45		
		9.0	30	38	45		
		12.0	30	38	45		
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	125	160	185	ns	
		4.5	25	32	37		
		9.0	25	32	37		
		12.0	25	32	37		
C	Maximum Capacitance	ON/OFF Control Input	—	10	10	10	pF
		Control Input = GND	—	35	35	35	
		Analog I/O Feedthrough	—	1.0	1.0	1.0	

## NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Switch)* (Figure 13)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
		15	pF

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**ADDITIONAL APPLICATION CHARACTERISTICS** (Voltages Referenced to GND unless noted)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f <sub>in</sub> = 1 MHz Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub> Increase f <sub>in</sub> Frequency Until dB Meter Reads - 3 dB R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off-Channel Feedthrough Isolation (Figure 6)	f <sub>in</sub> ≡ Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	- 50 - 50 - 50 - 40 - 40 - 40	dB
—	Feedthrough Noise, Control to Switch (Figure 7)	V <sub>in</sub> ≤ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns) Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	60 130 200 30 65 100	mV <sub>PP</sub>
—	Crosstalk Between Any Two Switches (Figure 12)	f <sub>in</sub> ≡ Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	- 70 - 70 - 70 - 80 - 80 - 80	dB
THD	Total Harmonic Distortion (Figure 14)	f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF THD = THD <sub>Measured</sub> - THD <sub>Source</sub> V <sub>IS</sub> = 4.0 V <sub>PP</sub> sine wave V <sub>IS</sub> = 8.0 V <sub>PP</sub> sine wave V <sub>IS</sub> = 11.0 V <sub>PP</sub> sine wave	4.5 9.0 12.0	0.10 0.06 0.04	%

\* Guaranteed limits not tested. Determined by design and verified by qualification.

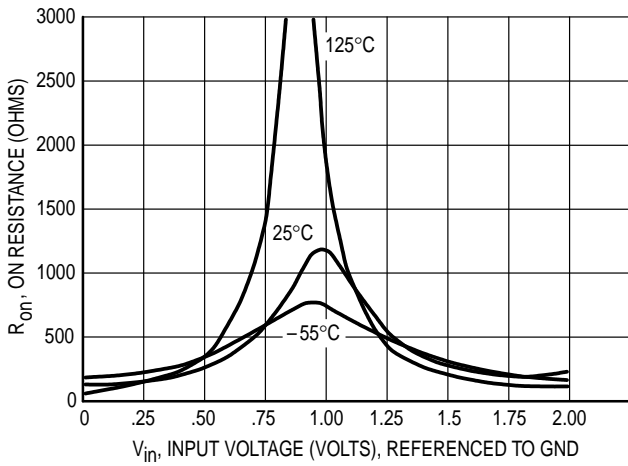


Figure 1a. Typical On Resistance,  $V_{CC} = 2.0 \text{ V}$

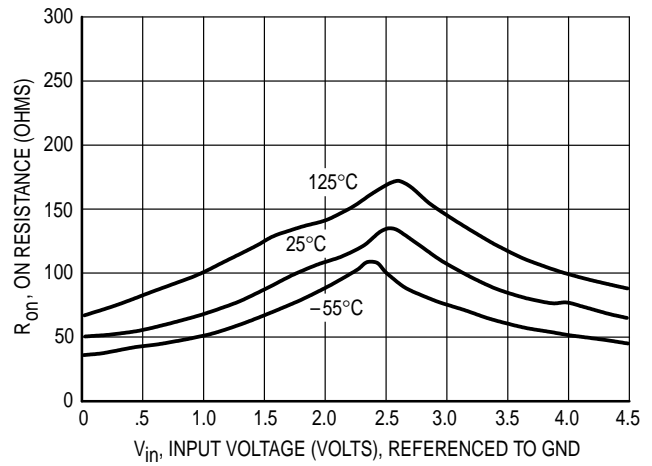


Figure 1b. Typical On Resistance,  $V_{CC} = 4.5 \text{ V}$

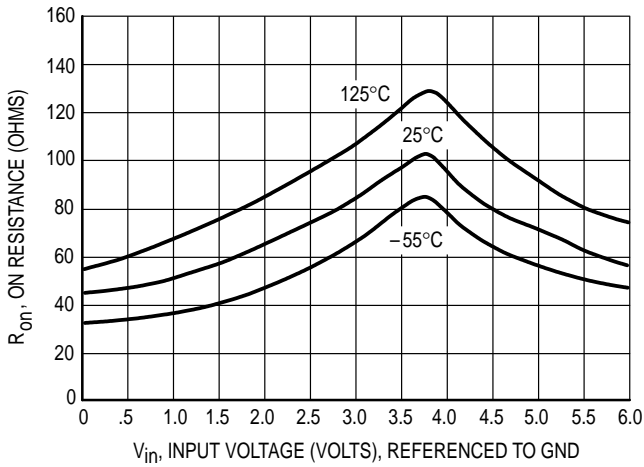


Figure 1c. Typical On Resistance,  $V_{CC} = 6.0 \text{ V}$

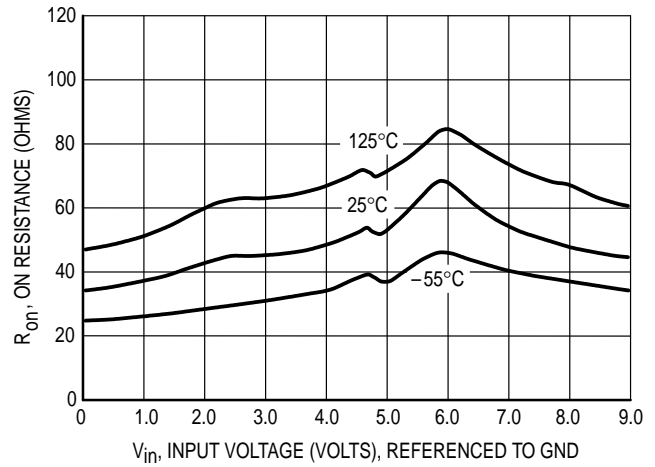


Figure 1d. Typical On Resistance,  $V_{CC} = 9.0 \text{ V}$

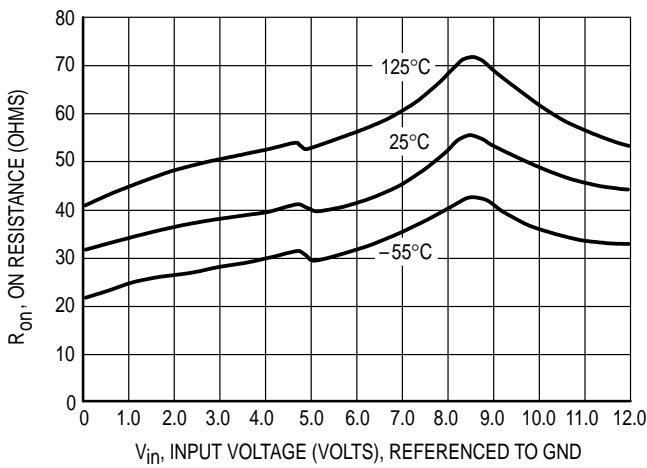


Figure 1e. Typical On Resistance,  $V_{CC} = 12.0 \text{ V}$

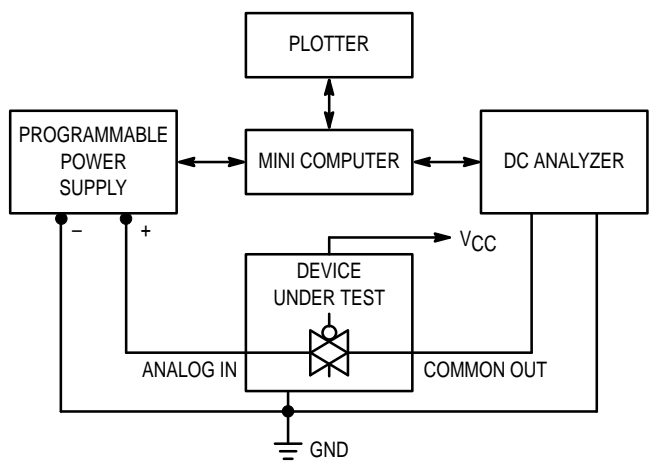


Figure 2. On Resistance Test Set-Up

MC54/74HC4016

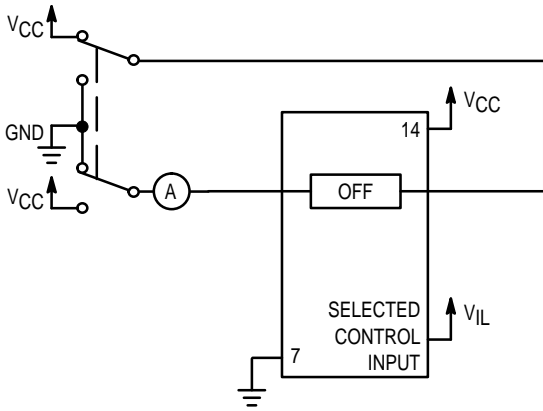


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

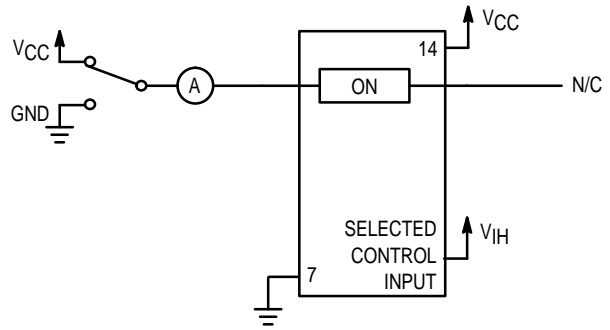
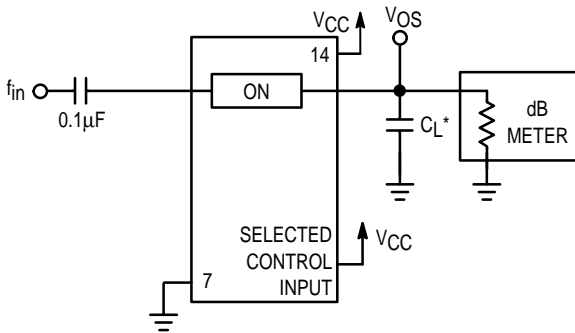
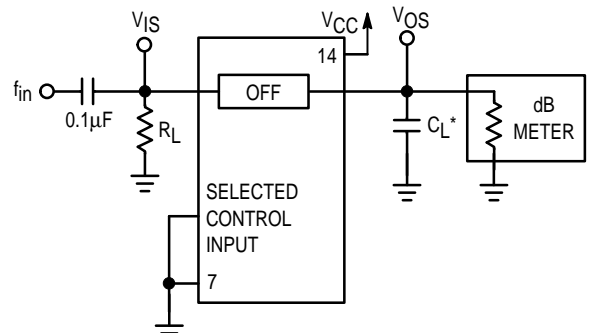


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



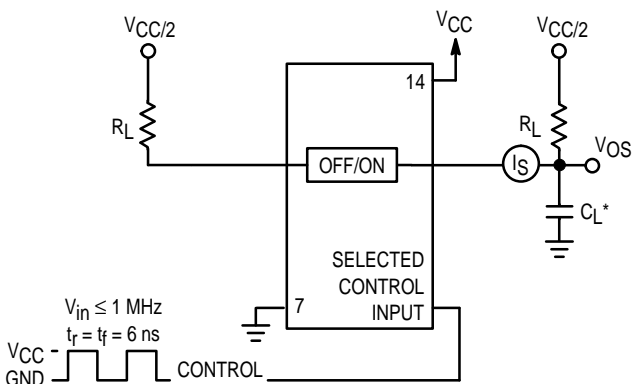
\*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth Test Set-Up



\*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

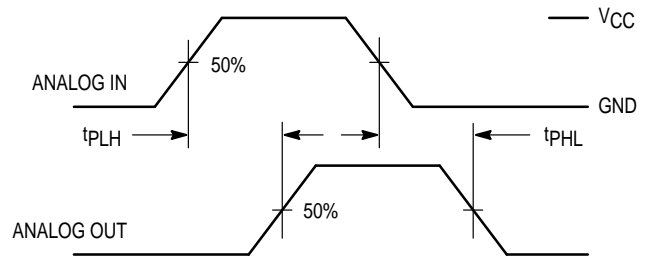
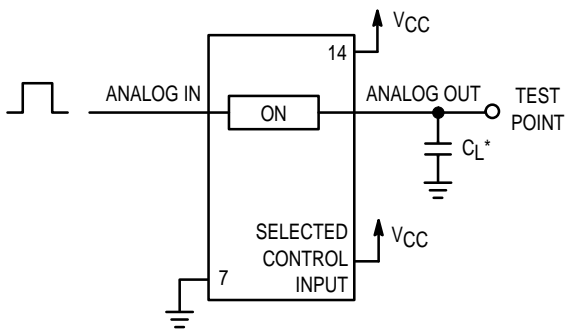


Figure 8. Propagation Delays, Analog In to Analog Out



\*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

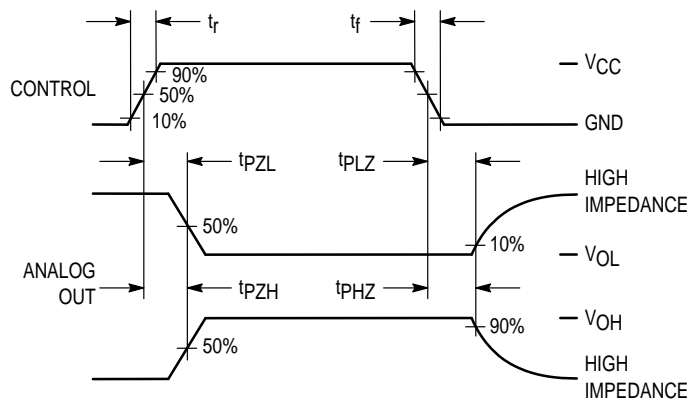
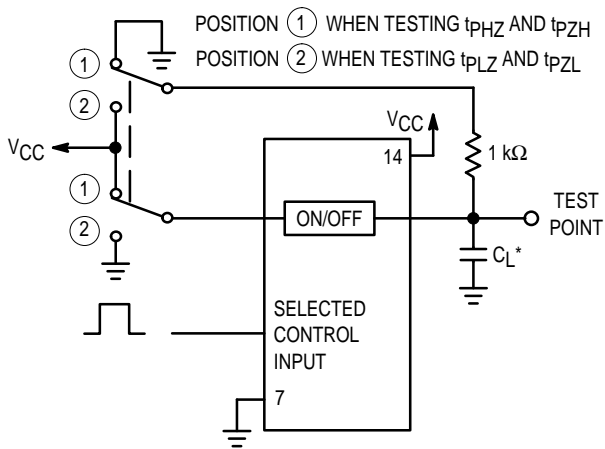
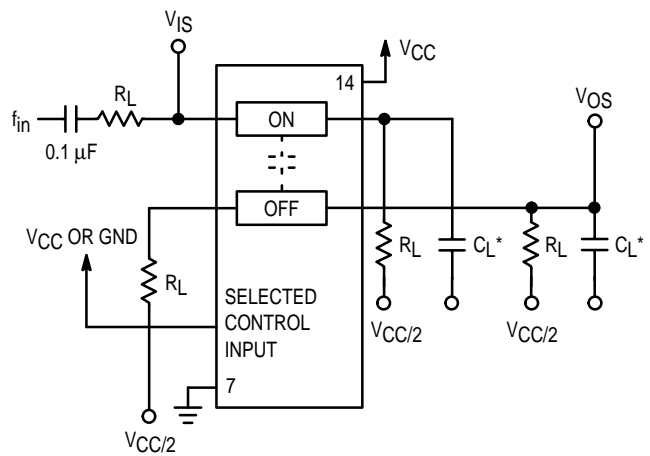


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



\*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



\*Includes all probe and jig capacitance

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

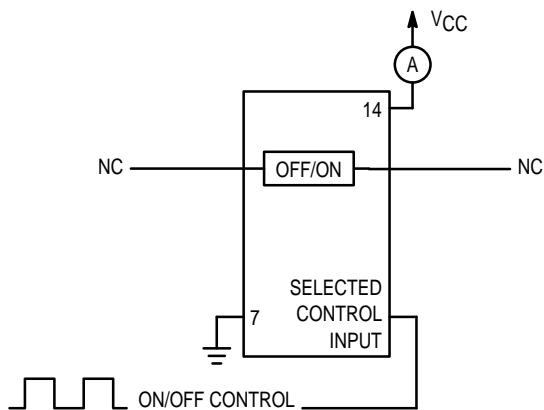
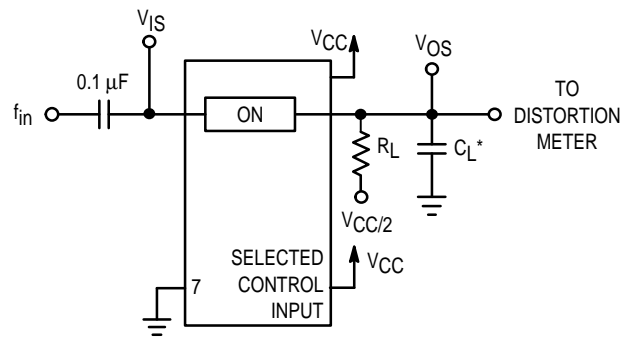


Figure 13. Power Dissipation Capacitance Test Set-Up



\*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

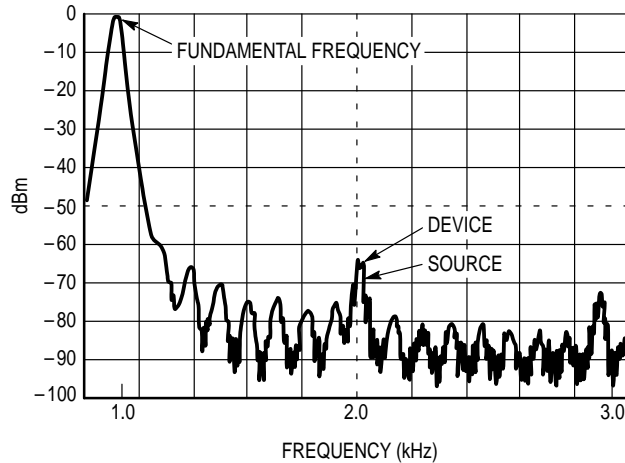


Figure 15. Plot, Harmonic Distortion

**APPLICATION INFORMATION**

The ON/OFF Control pins should be at  $V_{CC}$  or GND logic levels,  $V_{CC}$  being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and GND. The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below GND. In the example

below, the difference between  $V_{CC}$  and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above  $V_{CC}$  and/or below GND are anticipated on the analog channels, external diodes ( $D_x$ ) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the  $D_x$  diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear-out mechanism.

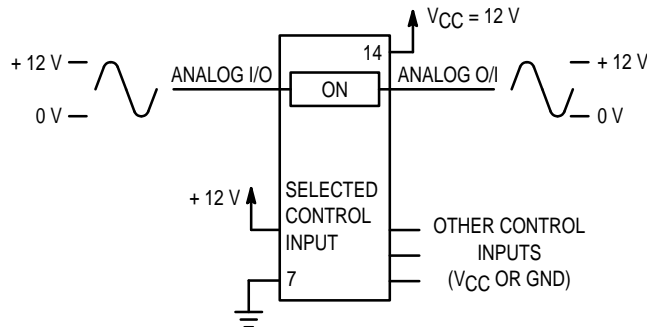


Figure 16. 12 V Application

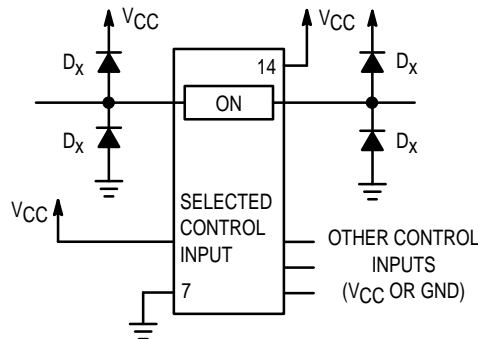


Figure 17. Transient Suppressor Application

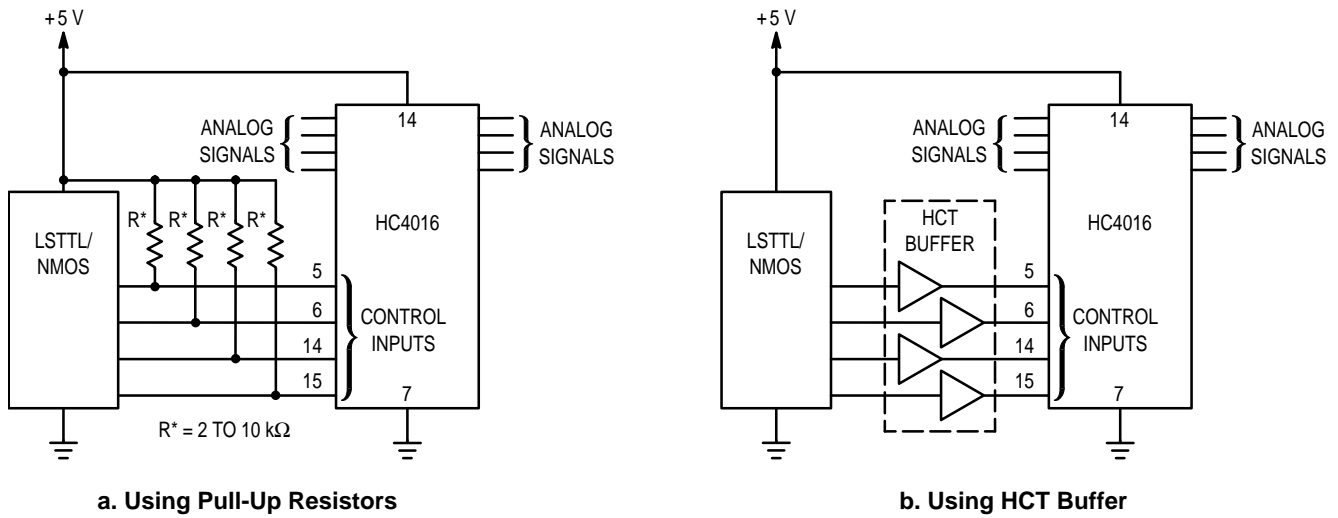


Figure 18. LSTTL/NMOS to HC4016 Interface

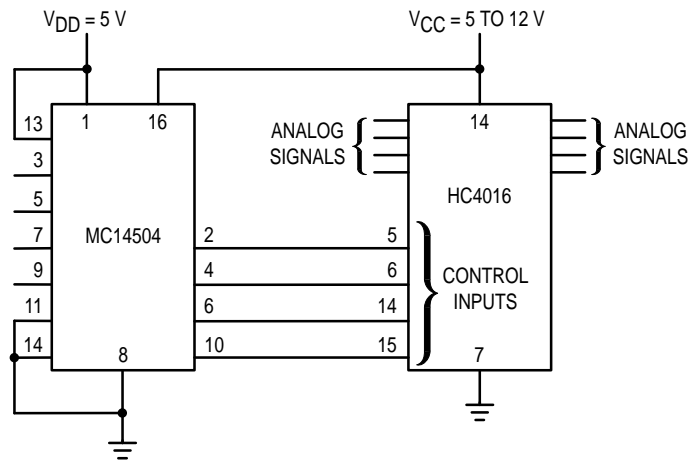
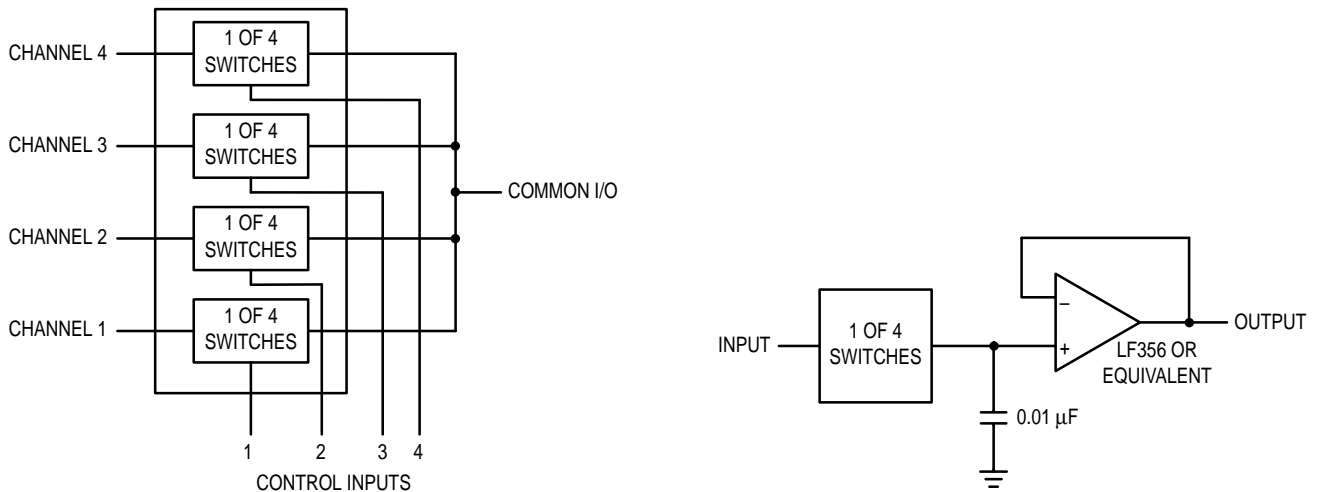
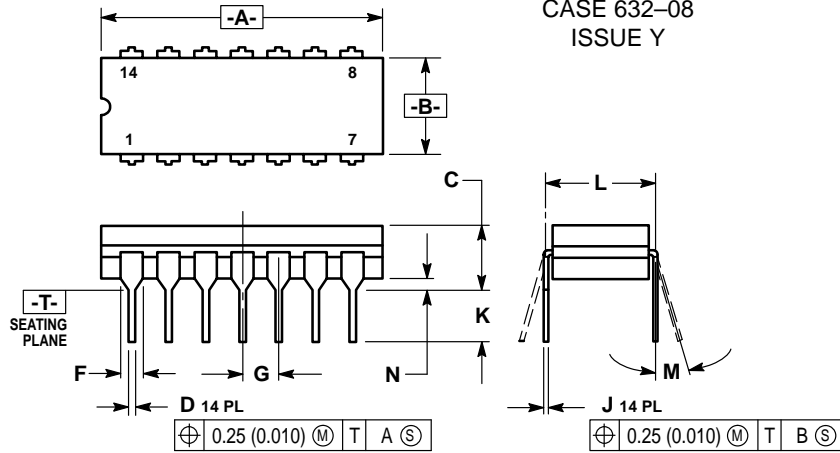


Figure 19. TTL/NMOS-to-CMOS Level Converter  
Analog Signal Peak-to-Peak Greater than 5 V  
(Also see HC4316)



OUTLINE DIMENSIONS

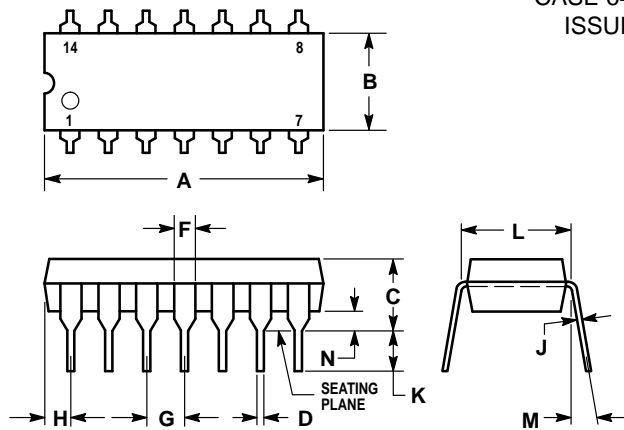
**J SUFFIX**  
**CERAMIC DIP PACKAGE**  
**CASE 632-08**  
**ISSUE Y**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

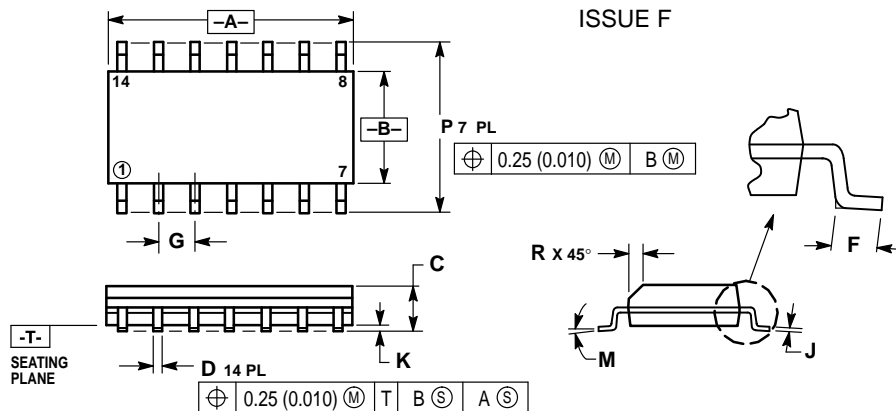
**N SUFFIX**  
**PLASTIC DIP PACKAGE**  
**CASE 646-06**  
**ISSUE L**



- NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  4. ROUNDED CORNERS OPTIONAL.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751A-03**  
**ISSUE F**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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