MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68010

Technical Summary

3 16-/32-Bit Virtual Memory Microprocessor

This document contains an MC68010 summary and a detailed set of parametrics. For detailed information on the MC68010, refer to the M68000UM/AD, *M68000 8-/16-/32-Bit Microprocessor User's Manual*.

The MC68010 is a member of the M68000 Family of advanced microprocessors. Utilizing VLSI technology, the MC68010 is a fully implemented 16-bit microprocessor with 32-bit registers, a rich basic instruction set, and versatile addressing modes.

The following resources are available to the MC68010 user:

- 17 32-Bit Data and Address Registers
- 16-Mbyte Direct Addressing Range
- Virtual Memory/Machine Support
- 57 Powerful Instruction Types
- High-Performance Looping Instructions
- Operations on Five Main Data Types
- Memory-Mapped I/O
- 14 Addressing Modes

This document contains information on a new product. Specifications and information herein are subject to change without notice.

INTRODUCTION

The MC68010 is fully user object-code compatible with the earlier members of the M68000 Family and has added features of virtual memory support and enhanced instruction execution timing. The MC68010 is pin-for-pin compatible with the MC68000.

The MC68010 possesses an asynchronous bus structure with a 24-bit address bus and a 16-bit data bus.

As shown in the user and supervisor programming models (see Figures 1 and 2), the MC68010 offers 17, 32-bit, general-purpose registers, a 32-bit program counter, a 16-bit status register, a 32-bit vector base register, and two 3-bit alternate function code registers. The first eight registers (D0–D7) are used as data registers for byte (8-bit), word (16-bit), and long-word (32-bit) operations. The second set of seven registers (A0–A6) and the stack pointers (SSP and USP) may be used as software stack pointers and base address registers. In addition, the address registers may be used for word and long-word operations. All 17 registers may be used as index registers.

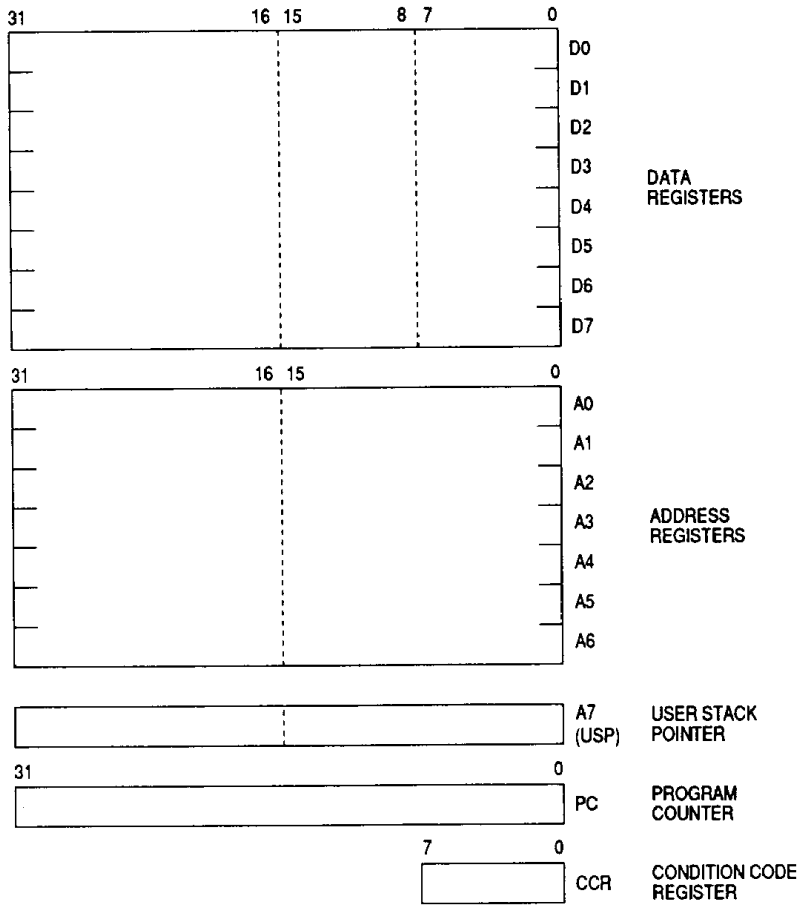


Figure 1. User Programming Model

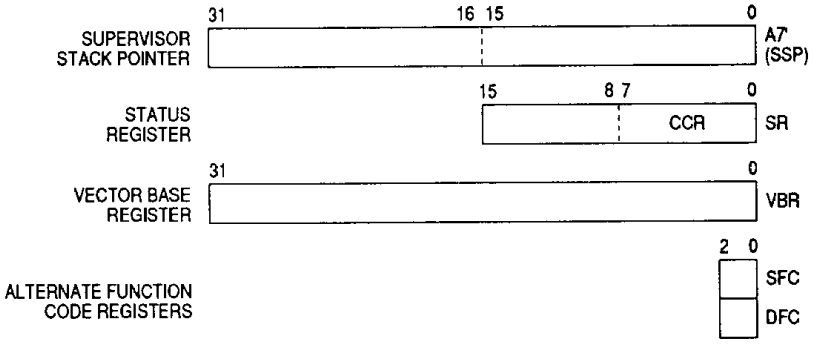


Figure 2. Supervisor Programming Model Supplement

The status register (SR) (see Figure 3) contains the interrupt mask (eight levels available) as well as the condition codes: extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

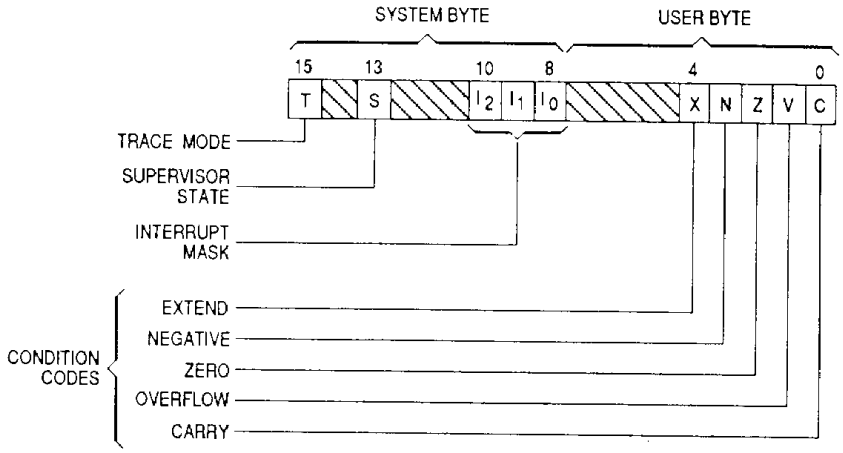


Figure 3. Status Register

The vector base register (VBR) is used to determine the location of the exception vector table in memory to support multiple vector tables. The alternate function code registers allow the supervisor to access user data space or emulate CPU space cycles.

DATA TYPES AND ADDRESSING MODES

Five basic data types are supported:

1. Bits
2. BCD Digits (4 Bits)
3. Bytes (8 Bits)
4. Words (16 Bits)
5. Long Words (32 Bits)

In addition, operations on other data types, such as memory addresses, status word data, etc., are provided in the instruction set.

Most instructions can use any of the 14 addressing modes listed in Table 1. These addressing modes consist of six basic types:

1. Register Direct
2. Register Indirect
3. Absolute
4. Program Counter Relative
5. Immediate
6. Implied

Included in the register indirect addressing modes is the capability to perform postincrementing, predecrementing, offsetting, and indexing. The program counter relative mode can also be modified via indexing and offsetting.

Table 1. Addressing Modes

Addressing Modes	Syntax
Register Direct Addressing	
Data Register Direct	Dn
Address Register Direct	An
Absolute Data Addressing	
Absolute Short	xxx.W
Absolute Long	xxx.L
Program Counter Relative Addressing	
Relative with Offset	d_{16}(PC)
Relative with Index Offset	d_8(PC,Xn)
Register Indirect Addressing	
Register Indirect	(An)
Postincrement Register Indirect	(An)+
Predecrement Register Indirect	−(An)
Register Indirect with Offset	d_{16}(An)
Indexed Register Indirect with Offset	d_8(An,Xn)
Immediate Data Addressing	
Immediate	#xxx
Quick Immediate	#1r#8
Implied Addressing	
Implied Register	SR/USP/SP/PC

NOTES:
Dn = Data Register
An = Address Register
Xn = Address of Data Register Used as Index Register
SR = Status Register
PC = Program Counter
SP = Stack Pointer
USP = User Stack Pointer
( ) = Effective Address
d_8 = 8-Bit Offset (Displacement)
d_{16} = 16-Bit Offset (Displacement)
#xxx = Immediate Data

INSTRUCTION SET OVERVIEW

The MC68010 instruction set is listed in Table 2. Some additional instructions that are variations or subsets of these instructions are listed in Table 3. Special emphasis is given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words, and most instructions can use any of the 14 addressing modes. By combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, quick arithmetic operations, BCD arithmetic, and expanded operations (through traps). Also, 33 instructions may be used in the loop mode with certain addressing modes and the DBcc instruction to provide 230 high-performance string and block manipulations and extended arithmetic operations.

Table 2. Instruction Set Summary

Mnemonic	Description
ABCD*	Add Decimal with Extend
ADD*	Add
AND*	Logical AND
ASL*	Arithmetic Shift Left
ASR*	Arithmetic Shift Right
Bcc	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register against Bounds
CLR*	Clear Operand
CMP*	Compare
DBcc	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR*	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL*	Logical Shift Left
LSR*	Logical Shift Right
MOVE*	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD*	Negate Decimal with Extend
NEG*	Negate
NOP	No Operation
NOT*	Ones Complement
OR*	Logical OR
PEA	Push Effective Address
RESET	Reset External Devices
ROL*	Rotate Left without Extend
ROR*	Rotate Right without Extend
ROXL*	Rotate Left with Extend
ROXR*	Rotate Right with Extend
RTD	Return and Deallocate
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD*	Subtract Decimal with Extend
Scc	Set Conditional
STOP	Stop
SUB*	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST*	Test
UNLK	Unlink

*Loopable Instructions

Table 3. Variations of Instruction Types

Instruction Type	Variation	Description
ADD	ADD*	Add
	ADDA*	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX*	Add with Extend
AND	AND*	Logical AND
	ANDI	AND Immediate
	ANDI to CCR	AND Immediate to Condition Codes
	ANDI to SR	AND Immediate to Status Register
CMP	CMP*	Compare
	CMPA*	Compare Address
	CMPM*	Compare Memory
	CMPI	Compare Immediate
EOR	EOR*	Exclusive OR
	EORI	Exclusive OR Immediate
	EORI to CCR	Exclusive OR Immediate to Condition Codes
	EORI to SR	Exclusive OR Immediate to Status Register
MOVE	MOVE*	Move Source to Destination
	MOVEA*	Move Address
	MOVEC	Move Control Register
	MOVEM	Move Multiple Registers
	MOVEP	Move Peripheral Data
	MOVEQ	Move Quick
	MOVES	Move Alternate Address Space
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE from CCR	Move from Condition Codes
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	NEG*	Negate
	NEGX*	Negate with Extend
OR	OR*	Logical OR
	ORI	OR Immediate
	ORI to CCR	OR Immediate to Condition Codes
	ORI to SR	OR Immediate to Status Register
SUB	SUB*	Subtract
	SUBA*	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX*	Subtract with Extend

*Loopable Instructions

VIRTUAL MEMORY/MACHINE CONCEPTS

In most systems using the MC68010 as the central processor, only a fraction of the 16-Mbyte addressing space will actually contain physical memory. However, by using virtual memory techniques, the system can be made to appear to the user to have 16-Mbytes of physical memory available. These techniques have been used for several years in large mainframe computers and more recently in minicomputers and now, with the MC68010, can be fully supported in microprocessor-based systems.

In a virtual memory system, a user program can be written as though it has a large amount of memory available to it when only a small amount of memory is physically present in the system. In a similar fashion, a system can be designed which allows user programs to access other types of devices that are not physically present in the system. With proper software emulation, a physical system can be made to appear to a user program as any other computer system, and the program may be given full access to all resources of that emulated system. Such an emulated system is called a virtual machine.

The MC68010 supports these modes through its instruction continuation mechanism. When an address error or bus error is encountered, the MC68010 will place its internal state on the supervisor stack. The appropriate exception handler is erased and, upon completion, causes the MC68010 to reload its internal state and resume execution.

Loop mode takes advantage of the fact that the MC68010 can contain three elements of the instruction stream internally. When these elements are 1) a loopable instruction, 2) the DBcc instruction, and 3) a branch displacement to the loopable instruction, the MC68010 will enter the loop mode in which no instruction accesses are made; only data accesses are performed. This allows extremely fast data transfers as well as providing the bus access made by the MC68010.

SIGNAL DESCRIPTION

The input and output signals are functionally grouped in Figure 4 and are described in the following paragraphs.

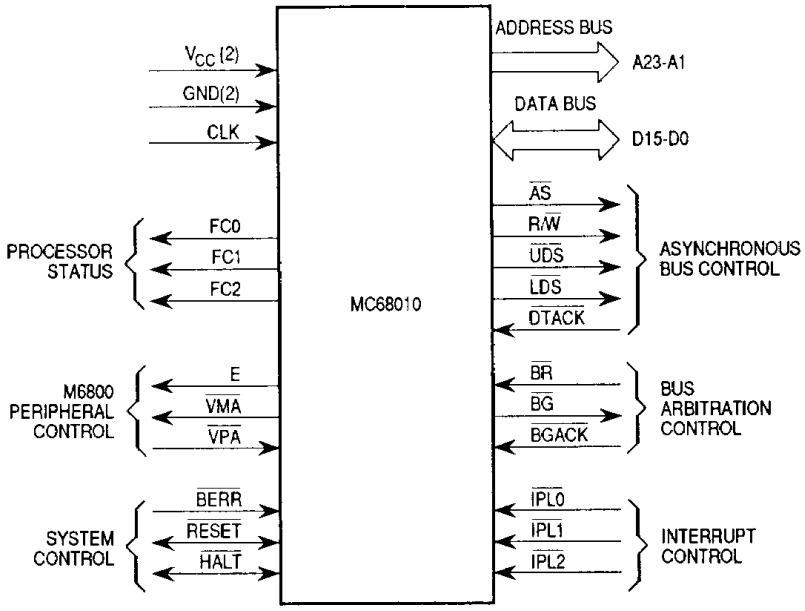


Figure 4. Functional Signal Groups

ADDRESS BUS (A1–A23)

This 23-bit, unidirectional, three-state bus is capable of addressing 16 Mbytes of data. It provides the address for bus operation during all cycles except CPU space cycles.

DATA BUS (D0–D15)

This 16-bit, bidirectional, three-state bus is the general-purpose data path. It can transmit and accept data in either word or byte length.

ASYNCHRONOUS BUS CONTROL

Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge.

Address Strobe ($\overline{AS}$)

This signal indicates a valid address on the address bus.

Read/Write (R/$\overline{W}$)

This signal defines the data bus transfer as a read or write cycle. R/$\overline{W}$ also works in conjunction with the data strobe as explained in the following paragraph.

Upper and Lower Data Strobe ($\overline{UDS}$, $\overline{LDS}$)

These signals control the flow of data on the data bus, as listed in Table 4. When R/$\overline{W}$ is high, the processor will read from the data bus as indicated. When R/$\overline{W}$ is low, the processor will write to the data bus as shown in Table 4.

Table 4. Data Strobe Control of Data Bus

$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D8–D15	D0–D7
1	1	—	No Valid Data	No Valid Data
0	0	1	Valid Data Bits 8–15	Valid Data Bits 0–7
1	0	1	No Valid Data	Valid Data Bits 0–7
0	1	1	Valid Data Bits 8–15	No Valid Data
0	0	0	Valid Data Bits 8–15	Valid Data Bits 0–7
1	0	0	Valid Data Bits 0–7	Valid Data Bits 0–7
0	1	0	Valid Data Bits 8–15	Valid Data Bits 8–15*

*These conditions are a result of current implementation and may not appear on future devices.

Data Transfer Acknowledge ($\overline{DTACK}$)

This input indicates that the data transfer is complete. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle is terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

BUS ARBITRATION CONTROL

Bus request, bus grant, and bus grant acknowledge form a bus arbitration circuit to determine which device will be the bus master.

Bus Request ($\overline{BR}$)

This input is wire-ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

Bus Grant ($\overline{BG}$)

This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge ($\overline{BGACK}$)

This input indicates that some other device has become the bus master. This signal should not be asserted until the following four conditions are met:

1. A bus grant has been received.
2. Address strobe is inactive, which indicates that the microprocessor is not using the bus.
3. Data transfer acknowledge is inactive, which indicates that neither memory nor peripherals are using the bus.
4. Bus grant acknowledge is inactive, which indicates that no other device is still claiming bus mastership.

INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$)

These pins indicate the encoded priority level of the device requesting an interrupt. Level 7 is the highest priority; level 0 indicates that no interrupts are requested. Level 7 cannot be masked. The least significant bit is $\overline{IPL0}$ and the most significant bit is $\overline{IPL2}$. These lines must remain stable until the processor signals interrupt acknowledge (FC0–FC2 are all high, A16–A19 are all high) to ensure that the interrupt is recognized.

SYSTEM CONTROL

The three system control inputs are used to reset or halt the processor and to indicate to the processor that bus errors have occurred.

Bus Error ($\overline{\text{BERR}}$)

This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. Nonresponding devices
2. Interrupt vector number acquisition failure
3. Illegal access request as determined by a memory management unit
4. Other application-dependent errors

The bus error signal interacts with the halt signal to determine if the current bus cycle should be re-executed or if exception processing should be performed.

Reset ($\overline{\text{RESET}}$)

This bidirectional signal resets (starts a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of a RESET instruction) causes all external devices to be reset, and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ signals applied simultaneously.

Halt ($\overline{\text{HALT}}$)

When this bidirectional signal is driven by an external device, it causes the processor to stop at the completion of the current bus cycle. When the processor is halted using this input, all control signals are inactive, and all three-state lines are put in their high-impedance state.

When the processor stops executing instructions, such as in a double bus fault condition, the $\overline{\text{HALT}}$ line is driven by the processor to indicate to external devices that the processor has stopped.

M6800 PERIPHERAL CONTROL

These control signals are used to interface synchronous M6800 peripheral devices with the asynchronous MC68010.

Enable (E)

This signal is the standard enable signal common to all M6800-type peripheral devices. The period for this output is 10 MC68010 clock periods (six clocks low, four clocks high). Enable is generated by an internal ring counter which may come up in any state (i.e., at power-on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

Valid Peripheral Address ($\overline{\text{VPA}}$)

This input indicates that the device addressed is an M68000 Family device and that data transfer should be synchronized with E. This input also indicates that the processor should use automatic vectoring for an interrupt.

Valid Memory Address ($\overline{\text{VMA}}$)

This output is used to indicate to M6800 peripheral devices that a valid address exists on the address bus and the processor is synchronized to E. This signal only responds to a $\overline{\text{VPA}}$ input, which indicates that the peripheral is an M68000 Family device.

PROCESSOR STATUS (FC0, FC1, FC2)

These function code outputs indicate the state (user or supervisor) and the address space of the bus cycle currently being executed (see Table 5). The information indicated by the function code outputs is valid whenever $\overline{\text{AS}}$ is active.

Table 5. Function Code Outputs

Function Code Output			Address Space
FC2	FC1	FC0	
0	0	0	Undefined, Reserved*
0	0	1	User Data
0	1	0	User Program
0	1	1	Undefined, Reserved*
1	0	0	Undefined, Reserved*
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	CPU

*Address space 3 is reserved for user definition; 0 and 4 are reserved for future use by Motorola.

CLOCK (CLK)

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time, and the clock signal must conform to minimum and maximum pulse-width times.

V_{CC} and GND

Power is supplied to the processor using these two signals.

SIGNAL SUMMARY

Table 6 is a summary of all the signals discussed in the previous paragraphs.

Table 6. Signal Summary

Signal Name	Mnemonic	Input/Output	Active State	Hi-Z	
				On $\overline{HALT}$	On $\overline{BGACK}$
Address Bus	A1–A23	Output	High	Yes	Yes
Data Bus	D0–D15	Input/Output	High	Yes	Yes
Address Strobe	$\overline{AS}$	Output	Low	No	Yes
Read/Write	R/$\overline{W}$	Output	Read—High Write—Low	No No	Yes Yes
Upper and Lower Data Strobe	$\overline{UDS}$, $\overline{LDS}$	Output	Low	No	Yes
Data Transfer Acknowledge	$\overline{DTACK}$	Input	Low	—	—
Bus Request	$\overline{BR}$	Input	Low	—	—
Bus Grant	$\overline{BG}$	Output	Low	No	No
Bus Grant Acknowledge	$\overline{BGACK}$	Input	Low	—	—
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	Input	Low	—	—
Bus Error	$\overline{BERR}$	Input	Low	—	—
Reset	$\overline{RESET}$	Input/Output	Low	No*	No*
Halt	$\overline{HALT}$	Input/Output	Low	No*	No*
Enable	E	Output	High	No	No
Valid Memory Address	$\overline{VMA}$	Output	Low	No	Yes
Valid Peripheral Address	$\overline{VPA}$	Input	Low	—	—
Function Code Output	FC0, FC1, FC2	Output	High	No	Yes
Clock	CLK	Input	High	—	—
Power Input	V_{CC}	Input	—	—	—
Ground	GND	Input	—	—	—

*Open Drain

DATA TRANSFER OPERATIONS

Transfer of data between devices involves the following leads:

1. Address bus A1–A23
2. Data bus D0–D15
3. Control signals

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the MC68010 for interlocked multiprocessor communications.

READ CYCLE

During a read cycle, the processor receives data from the memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when A0 equals zero, the upper data strobe is issued. When A0 equals one, the lower data strobe is issued. When the data is received, the processor correctly positions it internally. If $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, or $\overline{\text{VPA}}$ is not asserted for the required setup time before the falling edge of state 4, a wait cycle will be inserted in the bus cycle, and $\overline{\text{DTACK}}$ will be sampled again on the falling edge of each wait cycle. The MC68010 will continue to insert wait cycles until $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, or $\overline{\text{VPA}}$ is recognized.

WRITE CYCLE

During a write cycle, the processor sends data to either the memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when A0 equals zero, the upper data strobe is issued. When A0 equals one, the lower data strobe is issued. If $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, or $\overline{\text{VPA}}$ is not asserted for the required setup time before the falling edge of state 4, a

wait cycle will be inserted in the bus cycle, and $\overline{DTACK}$ will be sampled again on the falling edge of each wait cycle. The MC68010 will continue to insert wait cycles until $\overline{DTACK}$, $\overline{BERR}$, or $\overline{VPA}$ is recognized.

READ-MODIFY-WRITE CYCLE

The read-modify-write cycle performs a read, modifies the data in the arithmetic logic unit, and writes the data back to the same address. In the MC68010, this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. TAS is the only instruction that uses the read-modify-write cycles; since TAS only operates on bytes, all read-modify-write cycles are byte operations.

CPU SPACE CYCLE

During a CPU space cycle, the MC68010 reads a peripheral-device vector number or indicates a breakpoint instruction. If the cycle is to read a vector number, it is referred to as an interrupt acknowledge cycle. A CPU space cycle is indicated when the function codes are all high. The address bus then defines what type of CPU space cycle is being executed. The MC68010 defines two types of CPU space cycles, the interrupt acknowledge cycle and the breakpoint cycle.

The interrupt acknowledge cycle on an M68000 Family compatible processor is defined as a CPU space cycle with the most significant address lines high; on the MC68010, this cycle means that A4–A23 will be high. The level of the interrupt being acknowledged is encoded on address lines A1–A3. An interrupt acknowledge cycle is terminated in the same manner as a normal read cycle. The processor expects a peripheral device to respond to an interrupt acknowledge cycle with a vector number that will be used to transfer control to an interrupt handler routine.

The breakpoint read cycle is executed by the MC68010 in response to a breakpoint illegal instruction. A breakpoint cycle on the MC68010 is defined as a CPU space cycle with all of the address lines low. The processor does not accept or send any data during this cycle. The breakpoint cycle may be terminated by $\overline{DTACK}$, $\overline{BERR}$, or $\overline{VPA}$.

PROCESSING STATES

The MC68010 is always in one of three processing states: normal, exception, or halted.

NORMAL PROCESSING

The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands and to store results. A special case of the normal state is the stopped state which the processor enters when a stop instruction is executed. In this state, no further references are made.

EXCEPTION PROCESSING

The exception processing state is associated with interrupts, trap instructions, tracing, and other exception conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, a bus error, or a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

HALTED PROCESSING

The halted processing state is an indication of catastrophic hardware failure. For example, if, during the exception processing of a bus error, another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

INTERFACE WITH M6800 PERIPHERALS

Motorola's extensive line of M6800 peripherals are directly compatible with the MC68010. Some devices that are particularly useful are as follows:

MC6821 Peripheral Interface Adapter
MC6840 Programmable Timer Module
MC6843 Floppy Disk Controller
MC6845 CRT Controller
MC6850 Asynchronous Communications Interface Adapter
MC6854 Advanced Data Link Controller

To interface the synchronous M6800 peripherals with the asynchronous MC68010, the processor modifies its bus cycle to meet the M6800 cycle requirements whenever an M6800 device address is detected. This modification is possible since both processors use memory-mapped I/O.

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC68010 MC68010C	T_A	T_L to T_H 0 to 70 −40 to 85	°C
Storage Temperature	T_{stg}	−55 to 150	°C

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, normal precautions should be taken to avoid application of voltages higher than maximum-rated voltages to these high-impedance circuits. Tying unused inputs to the appropriate logic voltage level (e.g., either GND or V_{CC}) enhances reliability of operation.

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Symbol	Value	Rating
Thermal Resistance (Still Air)	θ_{JA}		θ_{JC}		°C/W
Ceramic, Type L/LC		30		15*	
Ceramic, Type R/RC		33		15	
Plastic, Type P		30		15*	
Plastic, Type FN		45		25*	

*Estimated

POWER CONSIDERATIONS

The average die-junction temperature T_J in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K/(T_J + 273\ °C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The curve shown in Figure 5 provides the graphic solution to these equations for the specified power dissipation of 1.5 watts over the ambient temperature range of −55 °C to +125 °C using a maximum θ_{JA} of 45 °C/W. Ambient temperature is that of the still air surrounding the device. Lower values of θ_{JA} cause the curve to shift downward slightly; for instance, for θ_{JA} of 40 °/W, the curve is just below 1.4 watts at 25 °C.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (θ_{JC}) and from the case to the outside ambient air θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by heat sinks, ambient air cooling, thermal convection, and other thermal management techniques. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation 1 results in a lower semiconductor junction temperature.

Table 7 summarizes maximum power dissipation and average junction temperature for the curve drawn in Figure 5, using the minimum and maximum values of ambient temperature for different packages and substituting θ_{JC} for θ_{JA} (assuming good thermal management). Table 8 provides the maximum power dissipation and average junction temperature for the MC68010 assuming that no thermal management is applied (i.e., still air).

NOTE

Since the power dissipation curve shown in Figure 5 is negatively sloped, power dissipation declines as ambient temperature increases. Therefore, maximum power dissipation occurs at the lowest rated ambient temperature where *power dissipation is lowest.*

Values for thermal resistance presented in this manual, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, *Thermal Resistance Measurement Method for MC68XXX Microcomponent Devices*, and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

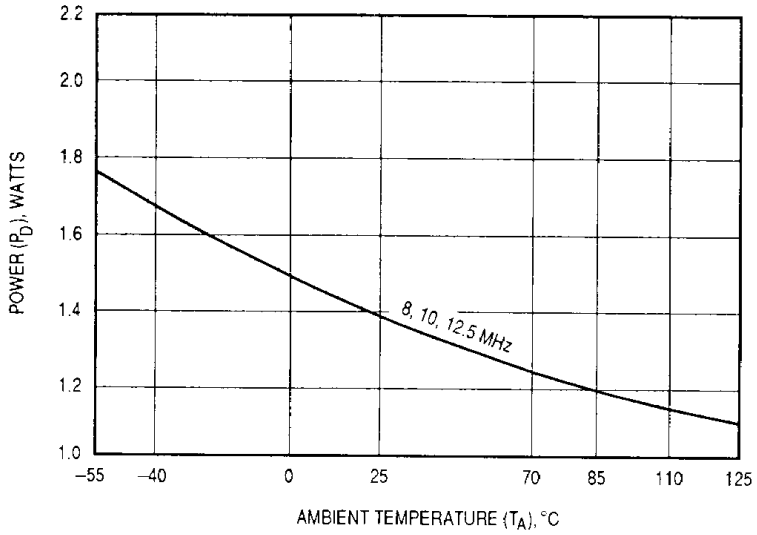


Figure 5. Power Dissipation (P_D vs Ambient Temperature (T_A)

Table 7. Power Dissipation and Junction Temperature vs Temperature ($\theta_{JC} = \theta_{JA}$)

Package	T_A Range	θ_{JC} (°C/W)	P_D (W) @ T_A Min	T_J (°C) @ T_A Min	P_D (W) @ T_A Max	T_J (°C) @ T_A Max
L/LC	0°C to 70°C –40°C to +85°C	15 15	1.5 1.7	22.5 –14.5	1.2 1.2	88 103
P	0°C to 70°C	15	1.5	22.5	1.2	88
R/RC	0°C to 70°C –40°C to +85°C	15 15	1.5 1.7	22.5 –14.5	1.2 1.2	88 103
FN	0°C to 70°C	25	1.5	37.5	1.2	100

Table 8. Power Dissipation and Junction Temperature vs Temperature ($\theta_{JA} \neq \theta_{JC}$)

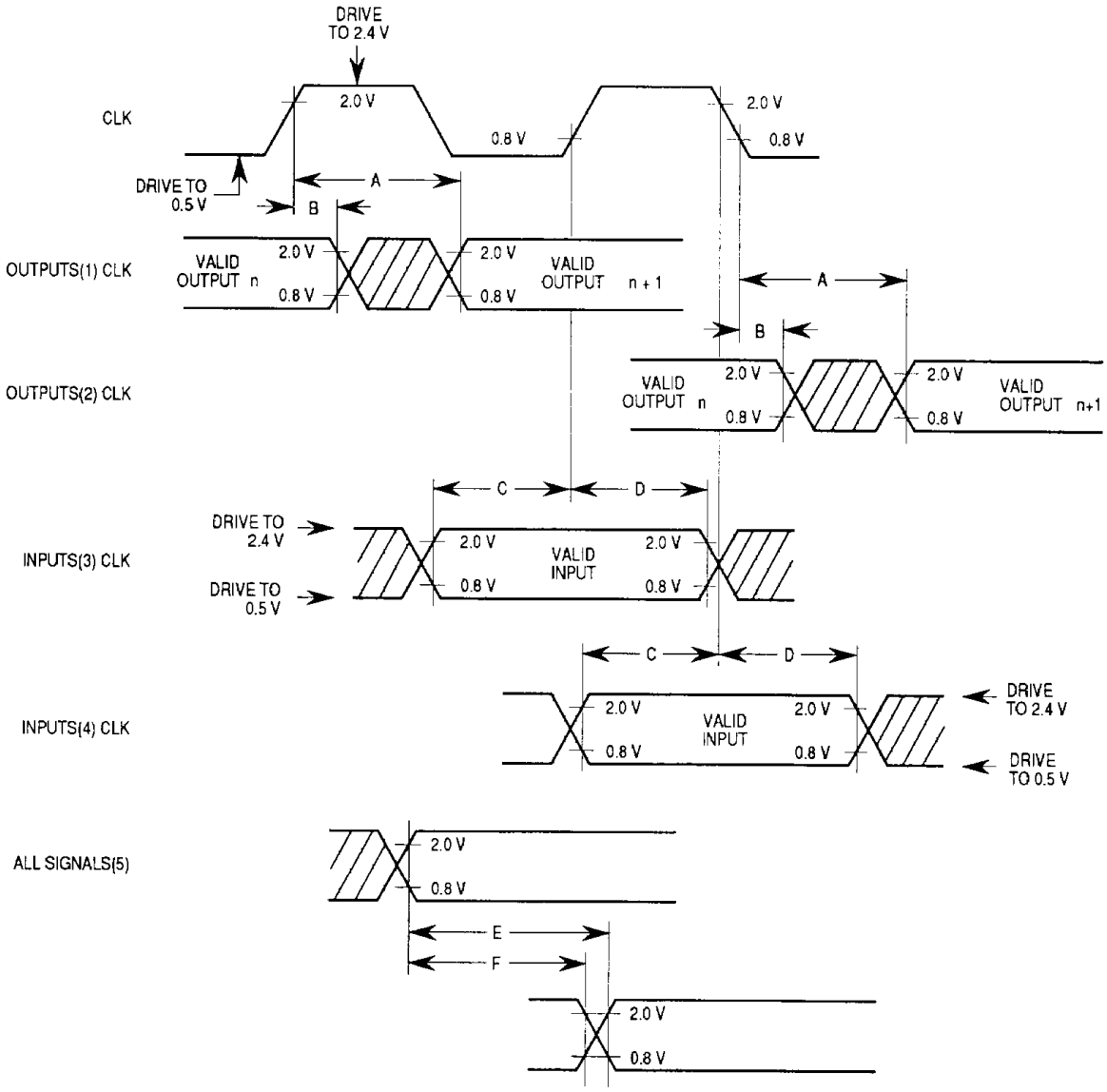
Package	T_A Range	θ_{JA} (°C/W)	P_D (W) @ T_A Min	T_J (°C) @ T_A Min	P_D (W) @ T_A Max	T_J (°C) @ T_A Max
L/LC	0°C to 70°C –40°C to +85°C	30 30	1.5 1.7	45 11	1.2 1.2	106 121
P	0°C to 70°C	30	1.5	45	1.2	106
R/RC	0°C to 70°C 40°C to –85°C	33 33	1.5 1.7	49.5 16.1	1.2 1.2	109.6 124.6
FN	0°C to 70°C	40	1.5	60	1.2	118

AC ELECTRICAL SPECIFICATIONS DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 6. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in this figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown in Figure 6. Inputs are specified with minimum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications is also shown.

Note that the testing levels used to verify conformance to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 6. Drive Levels and Test Points for AC Specifications

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H)

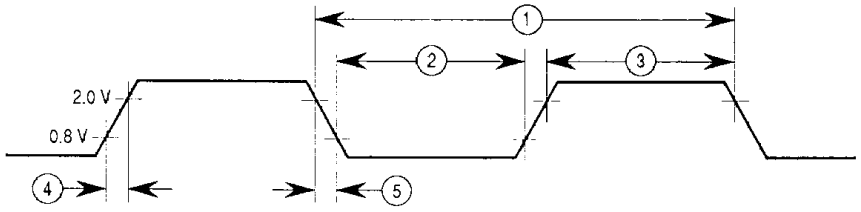
Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	GND − 0.3	0.8	V
Input Leakage Current @ 5.25 V	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$–$\overline{IPL2}$, $\overline{VPA}$ $\overline{HALT}$, $\overline{RESET}$	I_{IN}	— —	2.5 20	μA
Three-State (Off State) Input Current @ 2.4V/0.4 V	$\overline{AS}$, A1–A23, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	—	20	μA
Output High Voltage (I_{OH} = −400 μA) (I_{OH} = −400 μA)	E* E, $\overline{AS}$, A1–A23, $\overline{BG}$, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OH}	V_{CC} − 0.75 2.4	— 2.4	V
Output Low Voltage (I_{OL} = 1.6 mA) (I_{OL} = 3.2 mA) (I_{OL} = 5.0 mA) (I_{OL} = 5.3 mA)	 $\overline{HALT}$ A1–A23, $\overline{BG}$, FC0–FC2 $\overline{RESET}$ E, $\overline{AS}$, D0–D15, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OL}	 — — — —	 0.5 0.5 0.5 0.5	V
Power Dissipation (see **POWER CONSIDERATIONS**)		P_D***	—	—	W
Capacitance (V_{in} = 0 V, T_A = 25°C, Frequency = 1 MHz)**		C_{in}	—	20.0	pF
Load Capacitance	$\overline{HALT}$ All Others	C_L	— —	70 130	pF

*With external pullup resistor of 1.1 Ω.
**Capacitance is periodically sampled rather than 100% tested.
***During normal operation, instantaneous V_{CC} current requirements may be as high as 1.5 A.

AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (see Figure 7)

Num.	Characteristic	Symbol	8 MHz*		10 MHz*		12.5 MHz*		Unit
			Min	Max	Min	Mat	Min	Max	
	Frequency of Operation	f	4	8	4	10	4	12.5	MHz
1	Clock Period	t_{cyc}	125	250	100	250	80	250	ns
2,3	Clock Pulse Measured from 1.5 V to 1.5 V	t_{CL}, t_{CH}	55	125	45	125	35	125	ns
4,5	Clock Rise and Fall Times	t_{Cr}, t_{Cf}	—	10	—	10	—	5	ns

*These specifications represent an improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68010 and are valid only for product bearing date codes of 8827 and later.



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 V and 2.0 V.

Figure 7. Clock Input Timing Diagram

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 8 and 9)

Num.	Characteristic	Symbol	8 MHz*		10 MHz*		12.5 MHz*		Unit
			Min	Max	Min	Mat	Min	Max	
6	Clock Low to Address Valid	t_{CLAV}	—	62	—	50	—	50	ns
6A	Clock High to FC Valid	t_{CHFCV}	—	62	—	50	—	45	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	80	—	70	—	60	ns
8	Clock High to Address, FC Invalid (Minimum)	t_{CHAFI}	0	—	0	—	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted	t_{CHSL}	3	60	3	50	3	40	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read) $\overline{AS}$ Asserted (Write)	t_{AVSL}	30	—	20	—	15	—	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read) $\overline{AS}$ Asserted (Write)	t_{FCVSL}	90	—	70	—	60	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	t_{CLSH}	—	62	—	50	—	40	ns
13[2]	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid	t_{SHAFI}	40	—	30	—	20	—	ns
14[2]	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SL}	270	—	195	—	160	—	ns
14A[2]	$\overline{DS}$ Width Asserted (Write)	t_{DSL}	140	—	95	—	80	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width Negated	t_{SH}	150	—	105	—	65	—	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	80	—	70	—	60	ns
17[2]	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	t_{SHRH}	40	—	30	—	20	—	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	t_{CHRH}	0	55	0	45	0	40	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	t_{CHRL}	0	55	0	45	0	40	ns
20A[2, 6]	$\overline{AS}$ Asserted to R/$\overline{W}$ Valid (Write)	t_{ASRV}	—	10	—	10	—	10	ns
21[2]	Address Valid to R/$\overline{W}$ Low (Write)	t_{AVRL}	20	—	0	—	0	—	ns
21A[2]	FC Valid to R/$\overline{W}$ Low (Write)	t_{FCVRL}	60	—	50	—	30	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	t_{RLSL}	80	—	50	—	30	—	ns
23	Clock Low to Data-Out Valid (Write)	t_{CLDO}	—	62	—	50	—	50	ns
25[2]	$\overline{AS}$, $\overline{DS}$ Negated to Data-Out Invalid (Write)	t_{SHDOI}	40	—	30	—	20	—	ns
26[2]	Data-Out Valid to $\overline{DS}$ Asserted (Write)	t_{DOSL}	40	—	30	—	20	—	ns
27[5]	Data-In Valid to Clock Low (Setup Time of Read)	t_{DICL}	10	—	10	—	10	—	ns
27A[5]	Late $\overline{BERR}$ Asserted to Clock Low (Setup Time)	t_{BELCL}	45	—	45	—	45	—	ns
28[2]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold)	t_{SHDAH}	0	240	0	190	0	150	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	0	—	0	—	ns
29A	$\overline{AS}$, $\overline{DS}$ Negated to Data In High Impedance	t_{SHDZ}	—	187	—	150	—	120	ns
30	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{BERR}$ Negated	t_{SHBEH}	0	—	0	—	0	—	ns
31[2, 5]	$\overline{DTACK}$ Asserted to Data-In Valid (Setup Time)	t_{DALDI}	—	90	—	65	—	50	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	$t_{RHr,f}$	0	200	0	200	0	200	ns
33	Clock High to $\overline{BG}$ Asserted	t_{CHGL}	—	62	—	50	—	40	ns
34	Clock High to $\overline{BG}$ Negated	t_{CHGH}	—	62	—	50	—	40	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[7]	$\overline{BR}$ Negated to $\overline{BG}$ Negated	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GALGH}	1.5	3.5	1.5	3.5	1.5	3.5	Clks

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

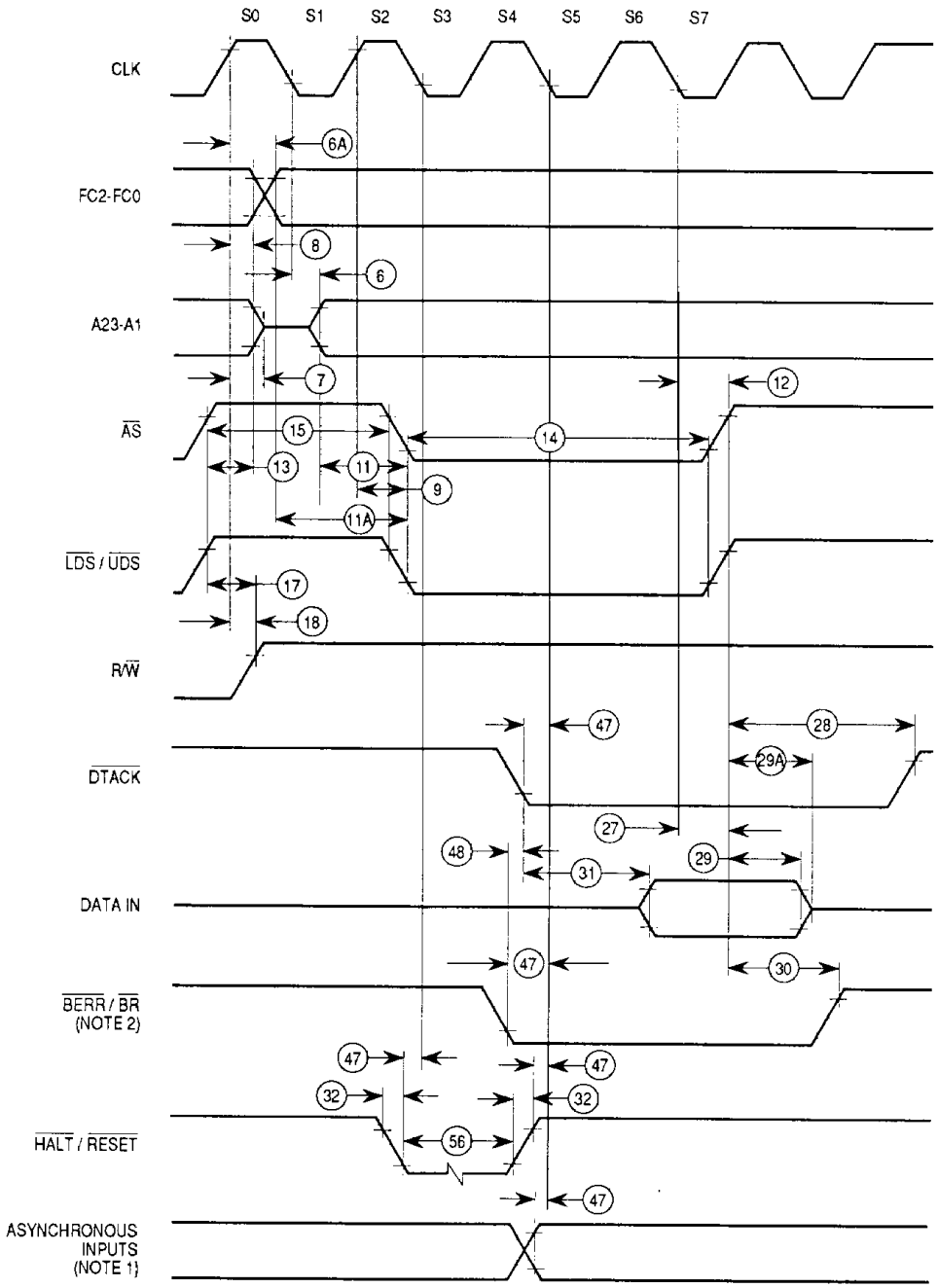
(Continued)

Num.	Characteristic	Symbol	8 MHz*		10 MHz*		12.5 MHz*		Unit
			Min	Max	Min	Mat	Min	Max	
37A[8]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	t_{GALBRH}	20	1.5 Clks	20	1.5 Clks	20	1.5 Clks	ns
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	t_{GLZ}	—	80	—	70	—	60	ns
39	$\overline{BG}$ Width Negated	t_{GH}	1.5	—	1.5	—	1.5	—	Clks
40	Clock Low to $\overline{VMA}$ Asserted	t_{CLVML}	—	70	—	70	—	70	ns
41	Clock Low to E Transition	t_{CLET}	—	55	—	45	—	35	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	15	—	15	—	15	ns
43	$\overline{VMA}$ Asserted to E High	t_{VMLEH}	200	—	150	—	90	—	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{VPA}$ Negated	t_{SHVPH}	0	120	0	90	0	70	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	t_{ELCAI}	30	—	10	—	10	—	ns
46	$\overline{BGACK}$ Width Low	t_{GAL}	1.5	—	1.5	—	1.5	—	Clks
47[5]	Asynchronous Input Setup Time	t_{ASI}	10	—	10	—	10	—	ns
48[2,3,5]	$\overline{DTACK}$ Asserted to $\overline{BERR}$ Asserted	t_{DALBEL}	—	80	—	55	—	35	ns
49[9]	$\overline{AS}$, $\overline{DS}$, Negated to E Low	t_{SHEL}	−70	70	−55	55	−45	45	ns
50	E Width High	t_{EH}	450	—	350	—	280	—	ns
51	E Width Low	t_{EL}	700	—	550	—	440	—	ns
53	Data-Out Hold from Clock High	t_{CHDOI}	0	—	0	—	0	—	ns
54	E Low to Data-Out Invalid	t_{ELDOI}	30	—	20	—	15	—	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RLDBD}	30	—	20	—	10	—	ns
56[4]	$\overline{HALT}$ $\overline{RESET}$ Pulse Width	t_{HRPW}	10	—	10	—	10	—	Clks
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{GASD}	1.5	—	1.5	—	1.5	—	Clks
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven	t_{GAFD}	1	—	1	—	1	—	Clks
58[7]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{RHSD}	1.5	—	1.5	—	1.5	—	Clks
58A[7]	$\overline{BR}$ Negated to FC, $\overline{VMA}$ Driven	t_{RHFD}	1	—	1	—	1	—	Clks

*These specifications represent an improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68010 and are valid only for product bearing date codes of 8827 and later.

NOTES:

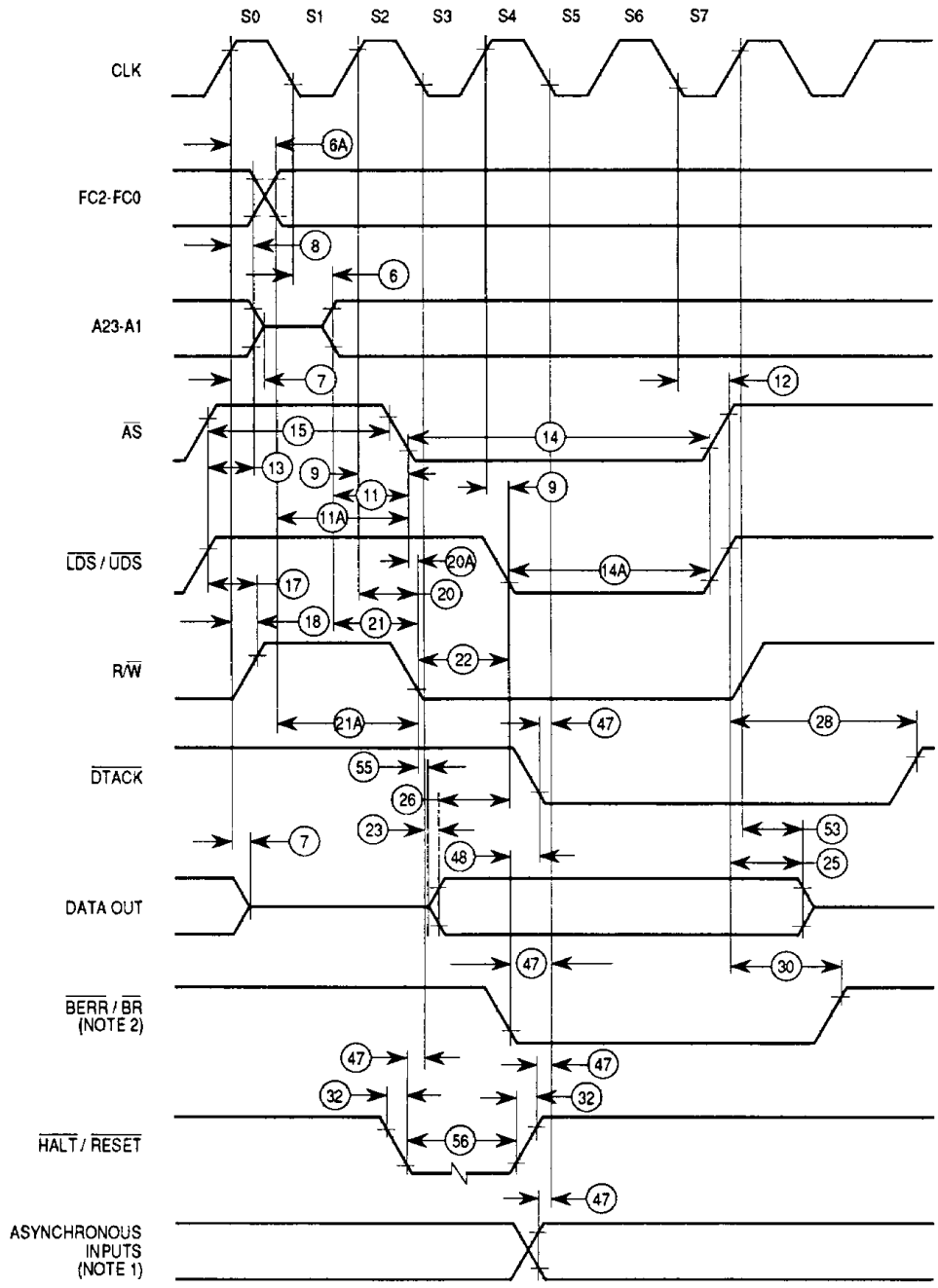
1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. Actual value depends on clock period.
3. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (#47).
4. For power-up, the MC68010 must be held in the $\overline{RESET}$ state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the processor.
5. If the asynchronous input setup time (#47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$ asserted to data setup time (#31) and $\overline{DTACK}$ asserted to $\overline{BERR}$ asserted setup time (#48) requirements can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle, and $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ asserted to clock-low setup time (#27A) for the following clock cycle.
6. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 5 ns from the values given in these columns.
7. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.
9. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{xDS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of E.



NOTES:

1. Setup time for the asynchronous inputs $\overline{IPL2}$-$\overline{IPL0}$ and $\overline{VPA}$ (#47) guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ need fall at this time only to ensure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

Figure 8. Read Cycle Timing Diagram



NOTES:

1. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.
2. Because of loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (specification #20A).

Figure 9. Write Cycle Timing Diagram

AC ELECTRICAL SPECIFICATIONS — PERIPHERAL CYCLES TO M6800

(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H, see Figures 10 and 11)

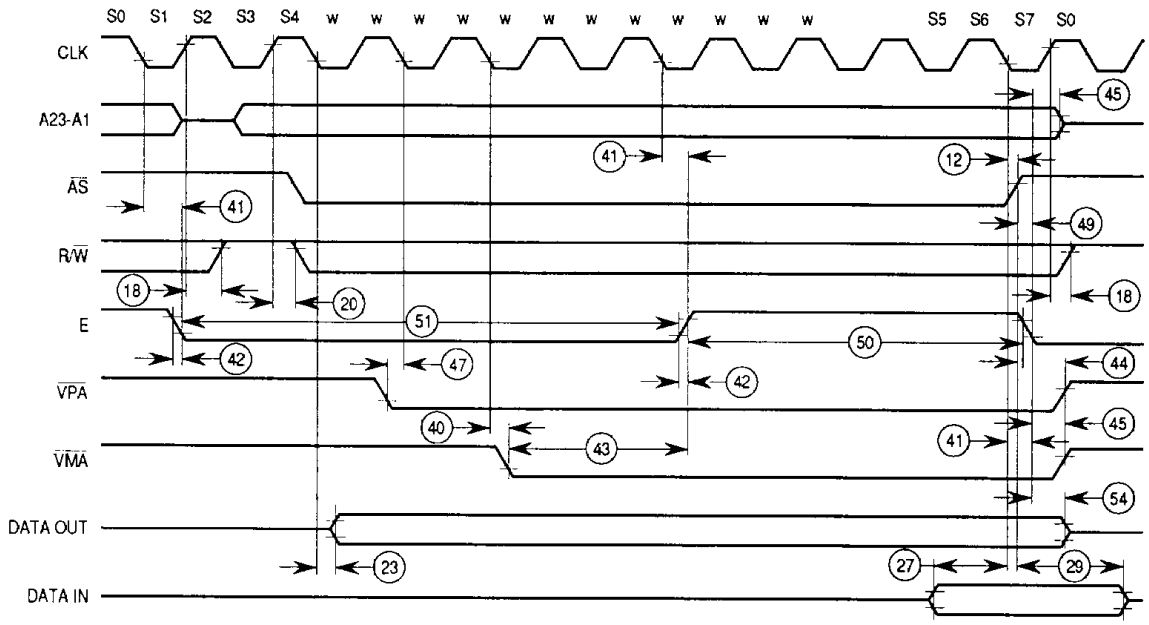
Num.	Characteristic	Symbol	8 MHz*		10 MHz*		12.5 MHz*		Unit
			Min	Max	Min	Max	Min	Max	
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	t_{CLSH}	—	62	—	50	—	40	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	t_{CHRH}	0	55	0	45	0	40	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	t_{CHRL}	0	55	0	45	0	40	ns
23	Clock Low to Data-Out Valid (Write)	t_{CLDO}	—	62	—	50	—	50	ns
27	Data-In Valid to Clock Low (Setup Time of Read)	t_{DICL}	10	—	10	—	10	—	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	0	—	0	—	ns
40	Clock Low to $\overline{VMA}$ Asserted	t_{CLVML}	—	70	—	70	—	70	ns
41	Clock Low to E Transition	t_{CLET}	—	55	—	45	—	35	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	15	—	15	—	15	ns
43	$\overline{VMA}$ Asserted to E High	t_{VMLEH}	200	—	150	—	90	—	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{VPA}$ Negated	t_{SHVPH}	0	120	0	90	0	70	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	t_{ELCAI}	30	—	10	—	10	—	ns
47	Asynchronous Input Setup Time	t_{ASI}	10	—	10	—	10	—	ns
49[2]	$\overline{AS}$, $\overline{DS}$, Negated to E Low	t_{SHEL}	−70	70	−55	55	−45	45	ns
50	E Width High	t_{EH}	450	—	350	—	280	—	ns
51	E Width Low	t_{EL}	700	—	550	—	440	—	ns
54	E Low to Data-Out Invalid	t_{ELDOI}	30	—	20	—	15	—	ns

*These specifications represent an improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68010 and are valid only for product bearing date codes of 8827 and later.

NOTES:

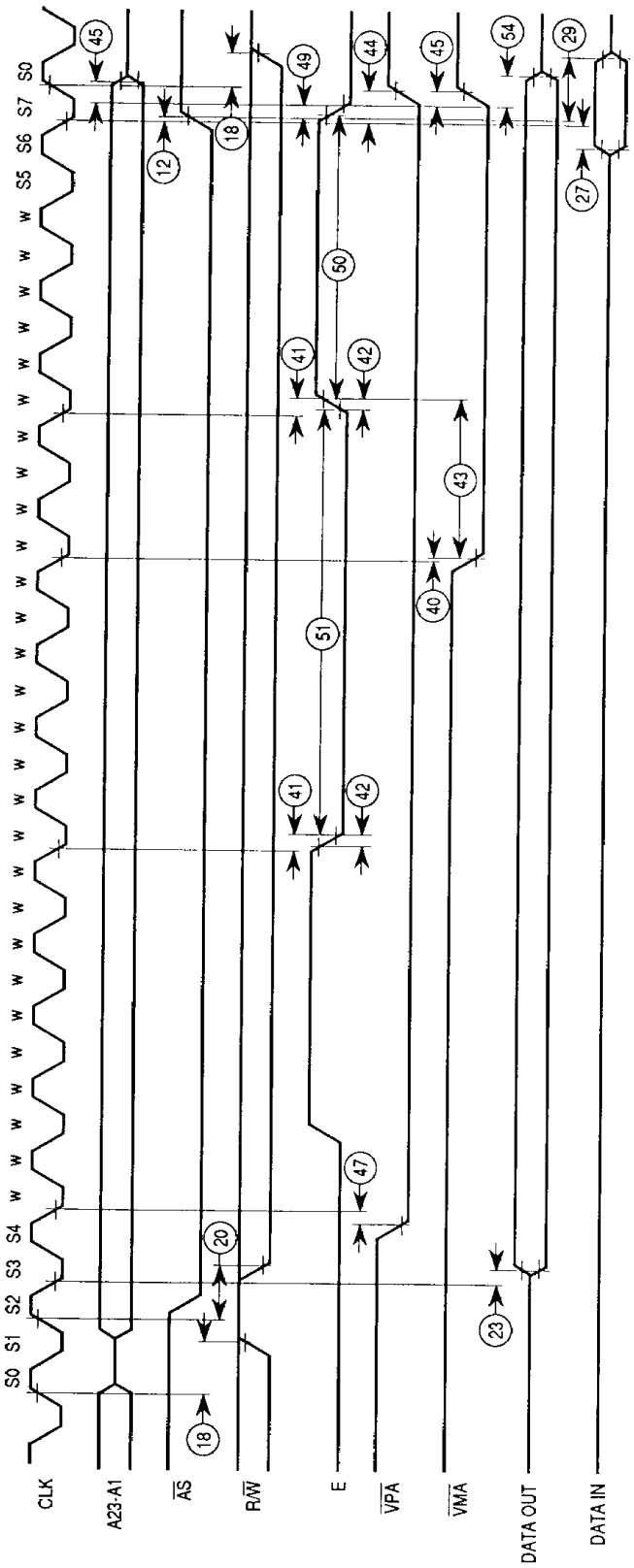
1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of E.

3



NOTE: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the best case possibly attainable.

Figure 10. MC68010 to M6800 Peripheral Timing Diagram (Best Case)



NOTE: This timing diagram is included for those who wish to design their own circuit to generate VMA. It shows the worst case possibly attainable.

Figure 11. MC68010 to M6800 Peripheral Timing Diagram (Worst Case)

3

AC ELECTRICAL SPECIFICATIONS — BUS ARBITRATION

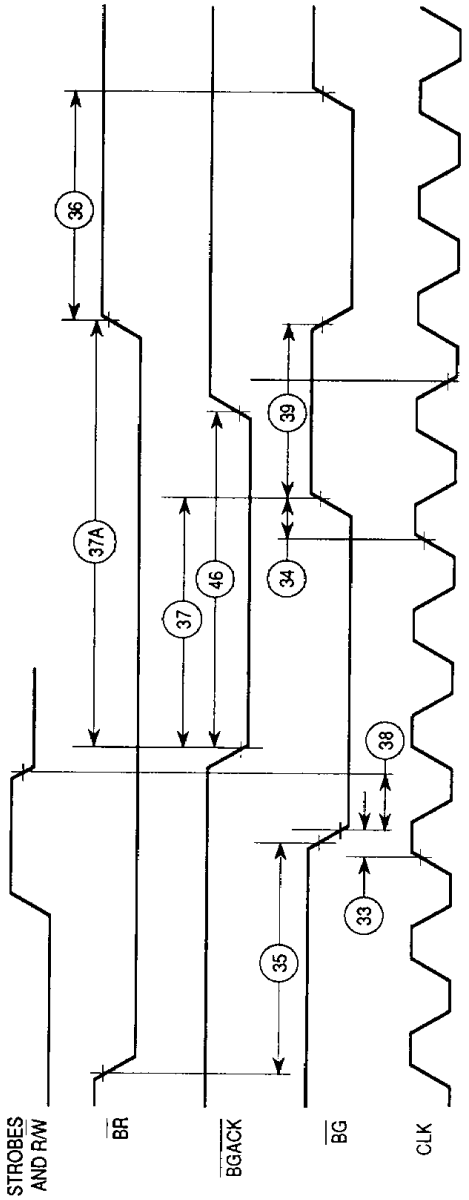
(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 12–15)

Num.	Characteristic	Symbol	8 MHz*		10 MHz*		12.5 MHz*		Unit
			Min	Max	Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	80	—	70	—	60	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	80	—	70	—	60	ns
33	Clock High to $\overline{BG}$ Asserted	t_{CHGL}	—	62	—	50	—	40	ns
34	Clock High to $\overline{BG}$ Negated	t_{CHGH}	—	62	—	50	—	40	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[1]	$\overline{BR}$ Negated to $\overline{BG}$ Negated	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GALGH}	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37A[2]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	t_{GALBRH}	20	1.5 Clks	20	1.5 Clks	20	1.5 Clks	ns
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	t_{GLZ}	—	80	—	70	—	60	ns
39	$\overline{BG}$ Width Negated	t_{GH}	1.5	—	1.5	—	1.5	—	Clks
46	$\overline{BGACK}$ Width Low	t_{GAL}	1.5	—	1.5	—	1.5	—	Clks
47	Asynchronous Input Setup Time	t_{ASI}	10	—	10	—	10	—	ns
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{GASD}	1.5	—	1.5	—	1.5	—	Clks
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven	t_{GAFD}	1	—	1	—	1	—	Clks
58[1]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{RHSD}	1.5	—	1.5	—	1.5	—	Clks
58A[1]	BR Negated to FC, $\overline{VMA}$ Driven	t_{RHFD}	1	—	1	—	1	—	Clks

*These specifications represent an improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68010 and are valid only for product bearing date codes of 8827 and later.

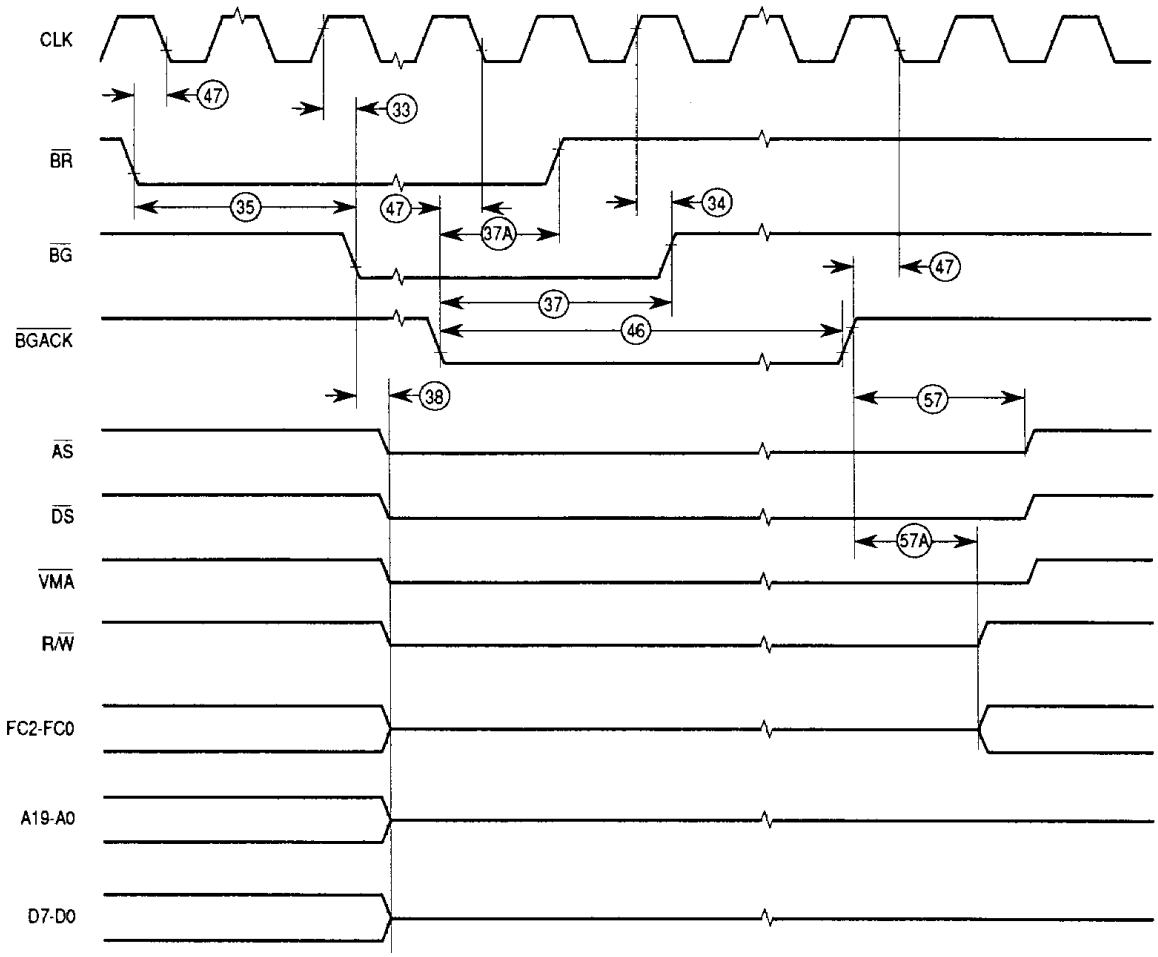
NOTES:

1. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
2. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.



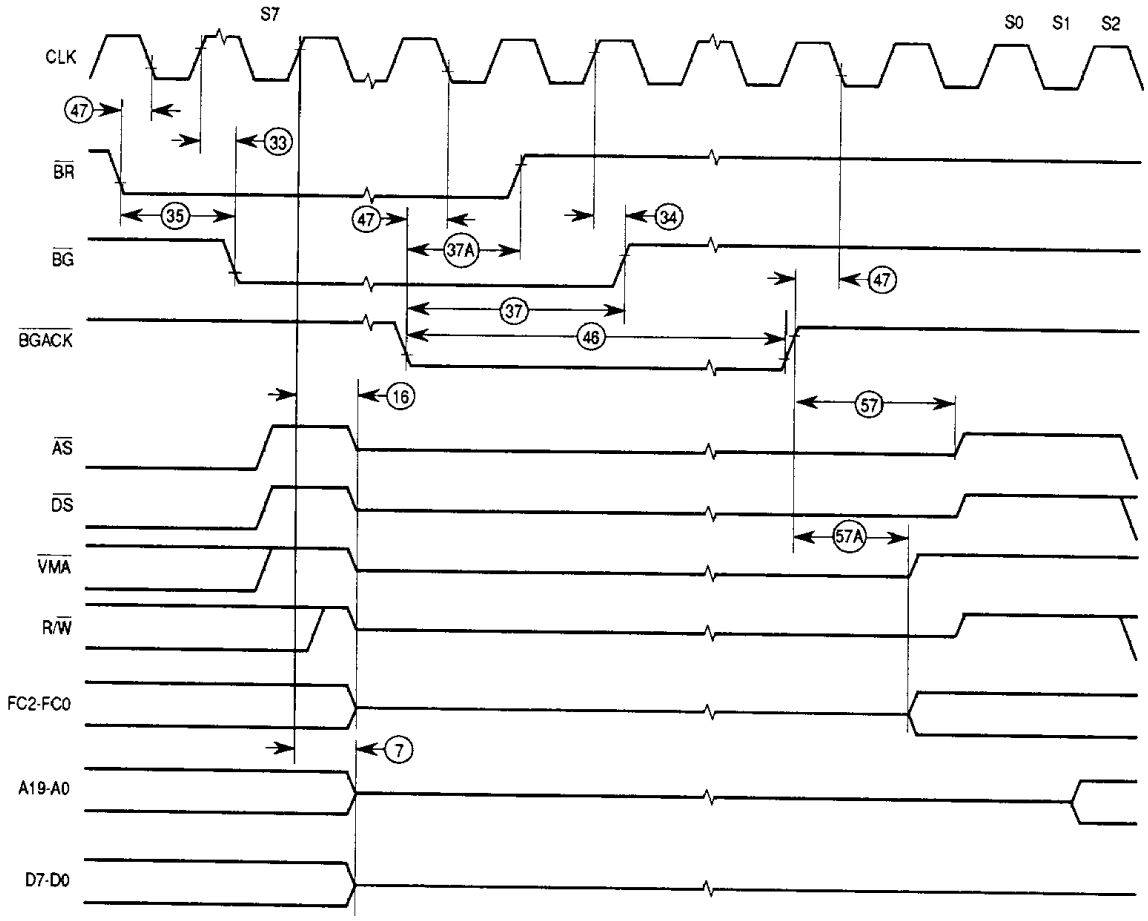
NOTE: Setup time to the clock (#47) for the asynchronous inputs BERR, BGACK, BR, DTACK, IPL2-IPL0, and VPA guarantees their recognition at the next falling edge of the clock.

Figure 12. Bus Arbitration Timing



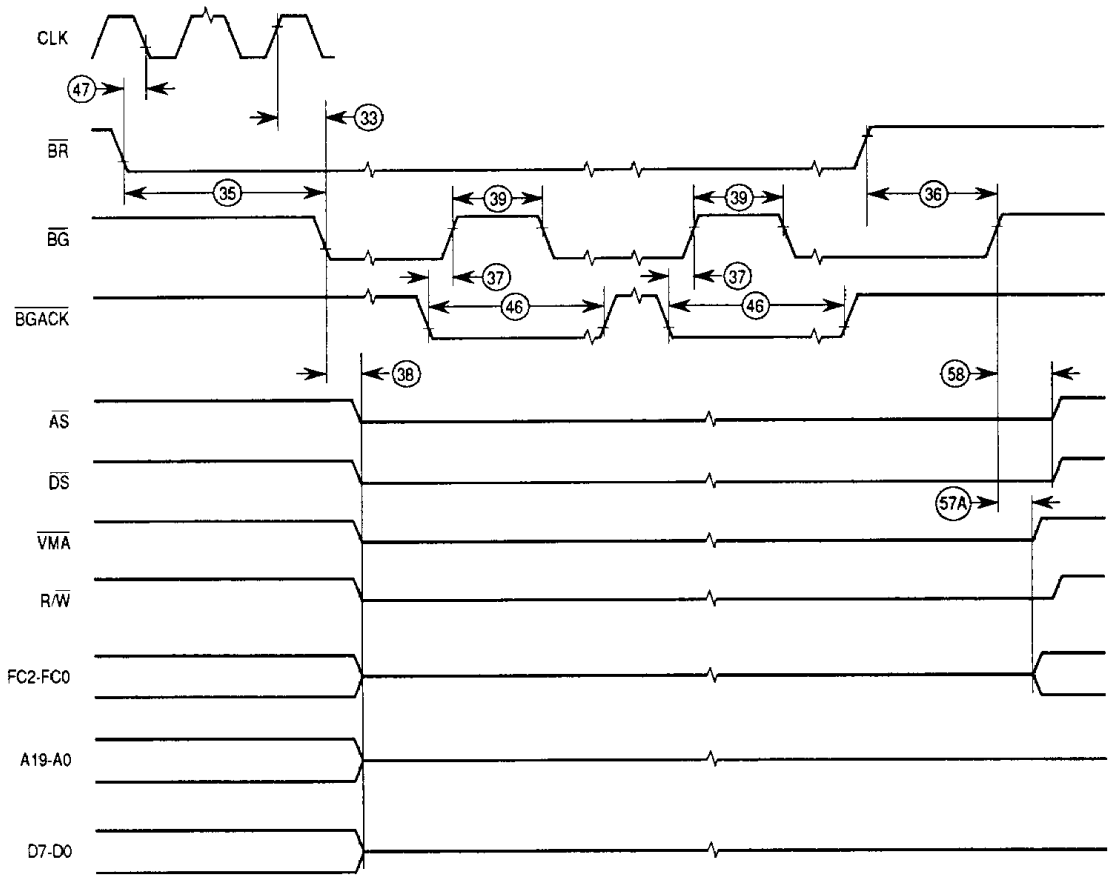
NOTE: Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 V, logic low = 0.8 V.

Figure 13. Bus Arbitration Timing — Idle Bus Case



NOTE: Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 V, logic low = 0.8 V.

Figure 14. Bus Arbitration Timing — Active Bus Case

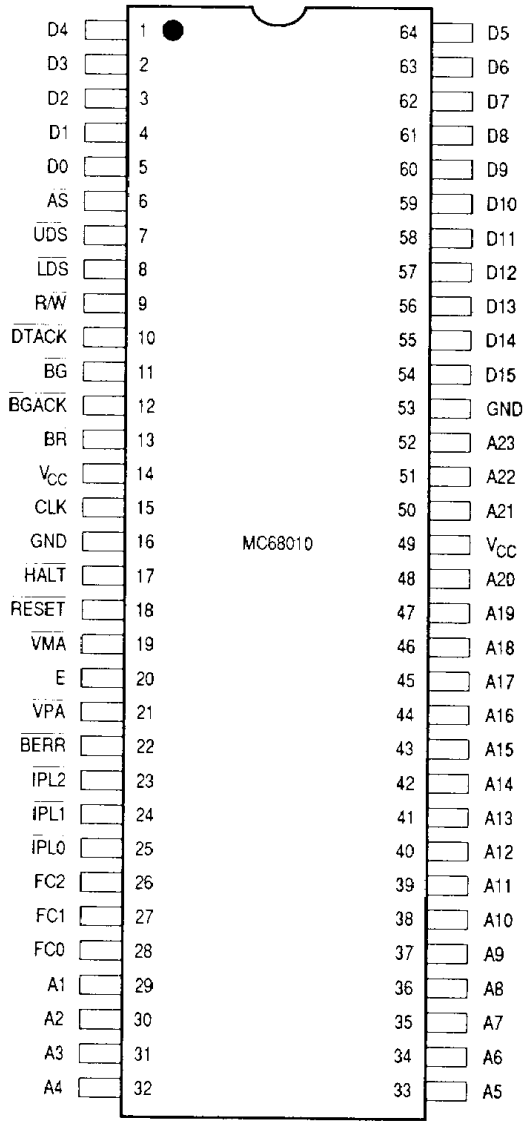


NOTE: Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 V, logic low = 0.8 V.

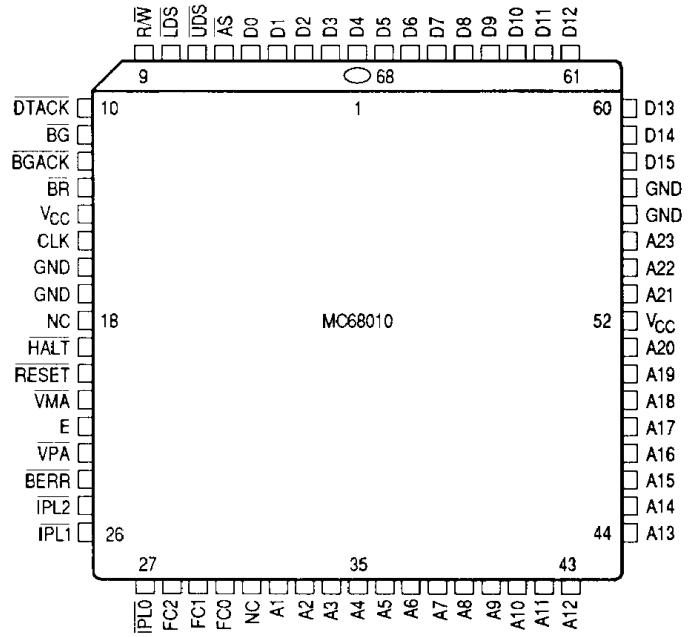
Figure 15. Bus Arbitration Timing — Multiple Bus Requests

PIN ASSIGNMENTS

64-LEAD DUAL-IN-LINE PACKAGE



68-LEAD QUAD PACKAGE



68-LEAD PIN GRID ARRAY