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MC68330
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Technical Summary
Integrated CPU32 Processor

The MC68330 is one of Motorola's CPU32-based M68300 Family of high-performance 32-bit integrated processors. The MC68330 combines on a single integrated circuit an enhanced M68000-compatible processor with a variety of circuits typically used to integrate a processor into the overall computer system. Devoid of the selection of peripheral circuits found on most M68300 products, the MC68330 gives the designer access to the higher performance of the CPU32 with minimized external glue logic, while allowing the greatest freedom in selecting needed peripheral and custom circuits. The MC68330 is also ideal for applications needing 32-bit CISC processor performance from a lower cost 16-bit memory system.

The MC68330's high level of functional integration results in reductions in component count, power consumption, board space, and cost while yielding higher system reliability and shorter design time. In an idle state, the MC68330 requires only a trickle of current, making it ideal for battery-powered applications. The 3.3-V MC68330V is particularly attractive to applications on a very tight power budget. Complete code compatibility with the MC68000 affords the designer access to a broad base of established real-time kernels, operating systems, languages, applications, and development tools, many of which are oriented towards embedded control. Figure 1 shows a simplified block diagram of the MC68330.

The primary features of the MC68330 are as follows:

- High Functional Integration on a Single Piece of Silicon
- CPU32—MC68020-Derived 32-Bit Central Processor Unit
  - — Upward Object-Code Compatible with MC68000 and MC68010
  - — Additional 32-Bit MC68020 Instructions and Addressing Modes
  - — Unique Embedded Control Instructions
  - — Fast Two-Clock Register Instructions—10,045 Dhrystones/Second
- System Integration Module (SIM40) Incorporates Many Functions Typically Relegated to External PALs, TTL, and ASIC, such as:
  - — System Configuration
  - — System Protection
  - — Chip-Select and Wait-State Generation
  - — Clock Generation
  - — Dynamic Bus Sizing
  - — Up to 16 Discrete I/O Lines
  - — External Bus Interface
  - — Periodic Interrupt Timer
  - — Interrupt Response
  - — Bus Arbitration
  - — IEEE 1149.1 Boundary Scan (JTAG)
  - — Power-On Reset
- 32 Address Lines, 16 Data Lines

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

- Power Consumption Control
  - — Static HCMOS Technology Reduces Power in Normal Operation
  - — Low-Voltage Operation at 3.3 V ±0.3 V (MC68330V only)
  - — Programmable Clock Generator Throttles Frequency
  - — LPSTOP Provides an Idle State for Lowest Standby Current
- 0–16.78 MHz or 0–25.16 MHz Operation
- 132-Pin Plastic Quad Flat Pack (PQFP) or 128-Pin 14 × 20 mm PQFP

As a low-voltage part, the MC68330V can operate with a 3.3-V power supply. MC68330 is used throughout this document to refer to both the low-voltage and standard 5-V parts since both are functionally equivalent.

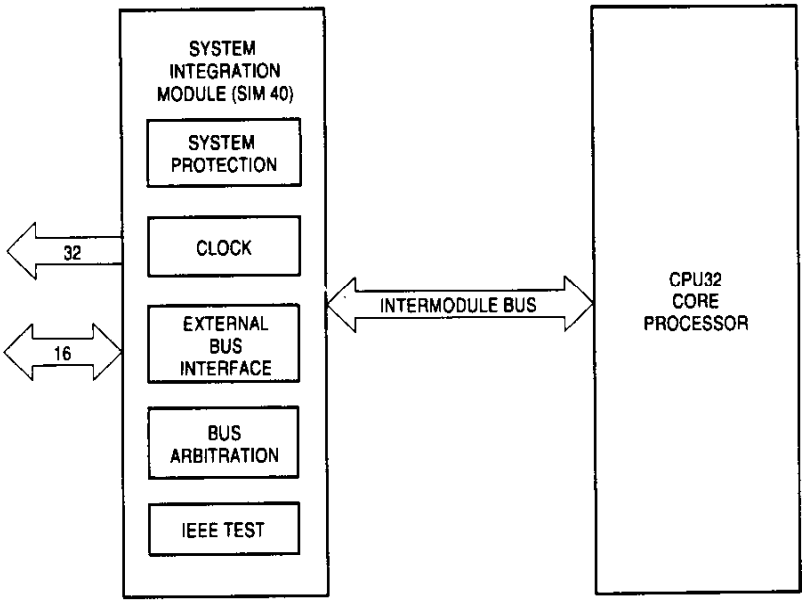


Figure 1. MC68330 Simplified Block Diagram

M68300 FAMILY

The MC68330 is one of a series of components in the Motorola M68300 family. Other members of the family include the MC68302, MC68331, MC68332, MC68F333, and MC68340.

ORGANIZATION

The M68300 family of integrated processors and controllers is built on an M68000 core processor, an on-chip bus, and a selection of intelligent peripherals appropriate for a set of applications. The CPU32 is a powerful central processor with nearly the performance of the MC68020. A system integration module (SIM40) incorporates the external bus interface and many of the smaller circuits that typically surround a microprocessor for address decoding, wait-state insertion, interrupt prioritization, clock generation, arbitration, watchdog timing, and power-on reset timing.

Each member of the M68300 family is distinguished by its selection of peripherals. Peripherals are chosen to address specific applications but are often useful in a wide variety of applications. The peripherals may be highly sophisticated timing or protocol engines that have their own processors, or they may be more traditional peripheral functions, such as UARTs and timers. Since each major function is designed in a standalone module, each module might be found in many different M68300 family parts. Driver software written for a module on one M68300 part can be used to run the same module that appears on another part.

ADVANTAGES

By incorporating so many major features into a single M68300 family chip, a system designer can realize significant savings in design time, power consumption, cost, board space, pin count, and programming. The equivalent functionality can easily require 20 separate components. Each component might have 16–64 pins, totaling over 350 connections. Most of these connections require interconnects or are duplications. Each connection is a candidate for a bad solder joint or misrouted trace. Each component is another part to qualify, purchase, inventory, and maintain. Each component requires a share of the printed circuit board. Each component draws power, which is often used to drive large buffers to get the signal to another chip. The cumulative power consumption of all the components must be available from the power supply. The signals between the CPU and a peripheral might not be compatible nor run from the same clock, requiring time delays or other special design considerations.

In an M68300 family component, the major functions and glue logic are all properly connected internally, timed with the same clock, fully tested, and uniformly documented. Power consumption stays well under a watt, and a special standby mode drops current well under a milliamp during idle periods. Only essential signals are brought out to pins. The primary package is the surface-mount plastic quad flat pack for the smallest possible footprint.

MC68330 SIGNALS

Figure 2 is a detailed diagram showing the components and signals.

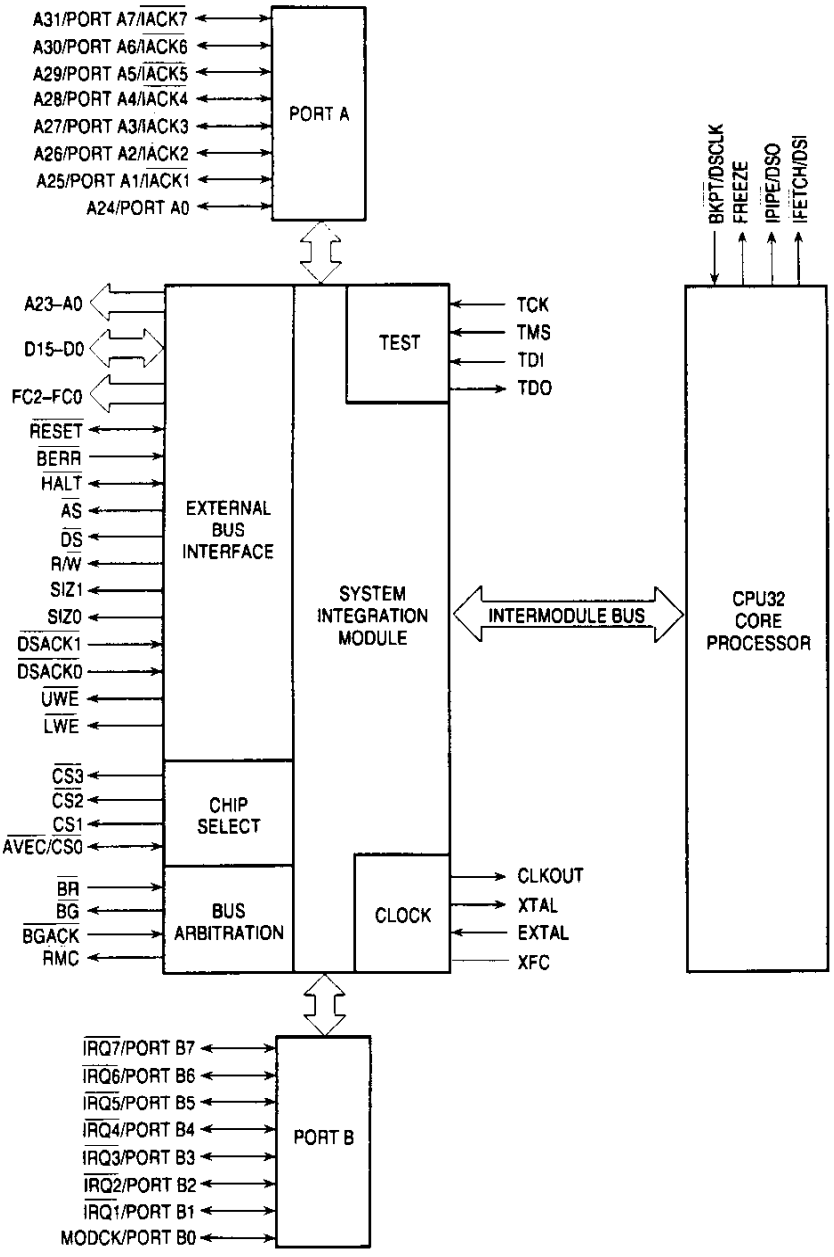


Figure 2. MC68330 Detailed Block Diagram

CENTRAL PROCESSOR UNIT

The CPU32 is a powerful central processor that supervises system functions, makes decisions, manipulates data, and directs I/O. A special debugging mode simplifies processor emulation during system debug.

CPU32

The CPU32 is an M68000 family processor specially designed for use as a 32-bit core processor and for operation over the intermodule bus (IMB). Designers used the MC68020 as a model and included advances of the later M68000 family processors, resulting in an instruction execution performance of 4 MIPS (VAX-equivalent) at 25.16 MHz.

The powerful and flexible M68000 architecture is the basis of the CPU32. MC68000 (including the MC68HC000 and the MC68EC000) and MC68010 user programs will run unmodified on the CPU32. The programmer can use any of the eight 32-bit data registers for fast manipulation of data and any of the eight 32-bit address registers for indexing data in memory. The CPU32 can operate on data types of single bits, binary-coded decimal (BCD) digits, and 8, 16, and 32 bits. Peripherals and data in memory can reside anywhere in the 4-Gbyte linear address space. A supervisor operating mode protects system-level resources from the more restricted user mode, allowing a true virtual environment to be developed.

Flexible instructions for data movement, arithmetic functions, logical operations, shifts and rotates, bit set and clear, conditional and unconditional program branches, and overall system control are supported, including a fast 32 × 32 multiply and 32-bit conditional branches. Instructions such as table lookup and interpolate and low-power stop (LPSTOP) support specific requirements of embedded control applications. Many addressing modes complement these instructions, including predecrement and postincrement, which allow simple stack and queue maintenance and scaled indexing for efficient table accesses. Data types and addressing modes are supported orthogonally by all data operations and with all appropriate addressing modes. Position-independent code is easily written.

The CPU32 is specially optimized to run with the MC68330's 16-bit data bus. Most instructions execute in one-half the number of clocks compared to the original MC68000, yielding an overall 1.6 times the performance of the same-speed MC68000 and measuring 10,045 Dhrystones/sec @ 25.16 MHz (6,742 Dhrystones/sec @ 16.78 MHz).

Like all M68000 family processors, the CPU32 recognizes interrupts of seven different priority levels and allows the peripheral to vector the processor to the desired service routine. Internal trap exceptions ensure proper instruction execution with good addresses and data, allow operating system intervention in special situations, and permit instruction tracing. Hardware signals can either terminate or rerun bad memory accesses before instructions process data incorrectly.

The CPU32 offers the programmer full 32-bit data processing performance with complete M68000 compatibility, yet with more compact code than is available with RISC processors. The CPU32 is identical in all CPU32-based M68300 family products.

BACKGROUND DEBUG MODE

A special operating mode is available in the CPU32 in which normal instruction execution is suspended while special on-chip microcode performs the functions of a debugger. Commands are received over a dedicated, high-speed, full-duplex serial interface. Commands allow the manual reading or writing of CPU32 registers, reading or writing of external memory locations, and diversion to user-specified patch code. This background debug mode permits a much simpler emulation environment while leaving the processor chip in the target system, running its own debugging operations.

ON-CHIP PERIPHERALS

To improve total system throughput and reduce part count, board size, and cost of system implementation, the M68300 family integrates on-chip peripheral modules and typical glue logic. On the MC68330, only the system integration module (SIM40) resides on chip with the CPU32.

The processor communicates with these modules over the on-chip intermodule bus (IMB). This backbone of the chip is similar to traditional external buses with address, data, clock, interrupt, arbitration, and handshake signals. Because bus masters (like the CPU32), peripherals, and the SIM40 can be on the chip, the IMB ensures that communication between these modules is fully synchronized and that arbitration and interrupts can be handled in parallel with data transfers, greatly improving system performance. Internal accesses across the IMB may be monitored from outside the chip, if desired.

Each module operates independently. No direct connections between peripheral modules are made inside the chip; however, external connections could, for instance, link a serial output to a DMA control line. Modules and their registers are relocatable and are accessed in the CPU32 memory map for easy access by general M68000 instructions. Each module may be assigned its own interrupt level, response vector, and arbitration priority. Since each module is a self-contained design and adheres to the IMB interface specifications, the modules may appear on other M68300 family products, retaining the investment in the software drivers for the module. The MC68330's SIM40 also appears on the MC68340.

SYSTEM INTEGRATION MODULE (SIM40)

The SIM40 provides the external bus interface for the CPU32. It also eliminates much of the glue logic that typically supports the microprocessor and its interface with the peripheral and memory system. The SIM40 provides programmable circuits to perform address decoding and chip selects, wait-state insertion, interrupt handling, clock generation, bus arbitration, watchdog timing, discrete I/O, and power-on reset timing. A boundary scan test capability is also provided.

EXTERNAL BUS INTERFACE

The external bus interface (EBI) handles the transfer of information between the internal CPU32 and memory, peripherals, or other processing elements in the external address space. Based on the MC68030 bus, the external bus provides up to 32 address lines and 16 data lines. Address extensions identify each bus cycle as supervisor or user privilege level and as instruction or data access. The data bus allows dynamic sizing for 8- or 16-bit bus accesses. Synchronous transfers for the CPU32 can be made in as little as two clock cycles. Asynchronous transfers allow the memory system to signal the CPU32 when the transfer is complete and to note the number of bits in the transfer. An external master can arbitrate for the bus using a three-line handshaking interface.

SYSTEM CONFIGURATION AND PROTECTION

The M68000 family of processors is designed with the concept of providing maximum system safeguards. System configuration and various monitors and timers are provided in the MC68330. Power-on reset circuitry is a part of the SIM40. A bus monitor ensures that the system does not lock up when there is no response to a memory access. The bus fault monitor can reset the processor when a catastrophic bus failure occurs. Spurious interrupts are detected and handled appropriately. A software watchdog can pull the processor out of an infinite loop. With the periodic interupt timer, an interrupt can be sent to the CPU32 with programmable regularity for DRAM refresh, time-of-day clock, task switching, etc.

CLOCK SYNTHESIZER

The clock synthesizer generates the clock signals used by all internal operations as well as a clock output used by external devices. The clock synthesizer can operate with an inexpensive 32768-Hz watch crystal or an external oscillator for reference, using an internal phase-locked loop and voltage-controlled oscillator. At any time, software can select clock frequencies from 131 kHz to 16.78 MHz or 25.16 MHz, favoring either low power consumption or high performance. Alternately, an external clock can directly drive the clock signal at the operating frequency. With its fully static HCMOS design, it is possible to completely stop the system clock without losing the contents of the internal registers.

CHIP-SELECT AND WAIT-STATE GENERATION

Four programmable chip selects provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals with up to 175-ns access times with a 25.16-MHz system clock (265 ns @ 16.78 MHz). Each chip select signal has an associated base address and an address mask that determine the addressing characteristics of that chip select. Address space and write protection can be selected for each. The block size can be selected from 256 bytes up to 4 Gbytes in increments of 2^n. Accesses can be preselected for either 8- or 16-bit transfers. Fast synchronous termination or up to three wait states can be programmed, whether or not the chip select signals are used. External handshakes can also signal the end of a bus transfer. A system can boot from reset out of 8-bit-wide memory, if desired.

INTERRUPT HANDLING

Seven input signals are provided to trigger an external interrupt, one for each of the seven priority levels supported. Seven separate outputs can indicate the priority level of the interrupt being serviced. An input can direct the processor to a default service routine, if desired. Interrupts at each priority level can be preprogrammed to go to the default service routine. For maximum flexibility, interrupts can be vectored to the correct service routine by the interrupting device.

DISCRETE I/O PINS

When not used for other functions, 16 pins can be programmed as discrete input or output lines.

IEEE 1149.1 TEST

To aid in system diagnostics, the MC68330 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability, often referred to as JTAG (Joint Test Action Group).

POWER CONSUMPTION MANAGEMENT

The MC68330 is very power efficient due to its advanced 0.8-μ HCMOS process technology and its static logic design. The resulting power consumption is typically 240 mW in full operation @ 16.78 MHz (370 mW @ 25.16 MHz)—far less than the comparable discrete component implementation the MC68330 can replace. For applications employing reduced voltage operation, selection of the MC68330V, which requires only a 3.3-V power supply, reduces current consumption by 40–60% in all modes of operation (as well as reducing noise emissions).

The MC68330 has many additional methods of dynamically controlling power consumption during operation. The frequency of operation can be lowered under software control to reduce current consumption when performance is less critical. Running a special LPSTOP instruction shuts down the active circuits in the CPU32 and SIM40 module, halting instruction execution. Power consumption in this standby mode is reduced to about 300 μW. Processing and power consumption can be resumed by resetting the part or by generating an interrupt, which can be done with the SIM40's periodic interrupt timer.

PHYSICAL

The MC68330 is available as 0–16.78 MHz and 0–25.16 MHz, 0°C to +70°C and -40°C to +85°C, and 5.0 V ±5% and 3.3 V ±0.3 supply voltages (reduced frequencies at 3.3 V). Multiple power and ground leads minimize ground bounce and ensure proper isolation of different sections of the chip, including the clock oscillator. Either 132 or 120 pins are used for signals and power. The MC68330 is available in a PQFP with 0.25-in or 0.5-mm lead spacing.

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C

The following ratings define a range of conditions in which the device will operate without being damaged. However, sections of the device may not operate normally while being exposed to the electrical extremes. This device contains circuitry to protect against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance	θ_{JA}		°C/W
132-Pin PQFP		42	
128-Pin PQFP		TBD	

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts—Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins—User Determined

For most applications, $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from Equation (3) by measuring P_D (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A.

AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

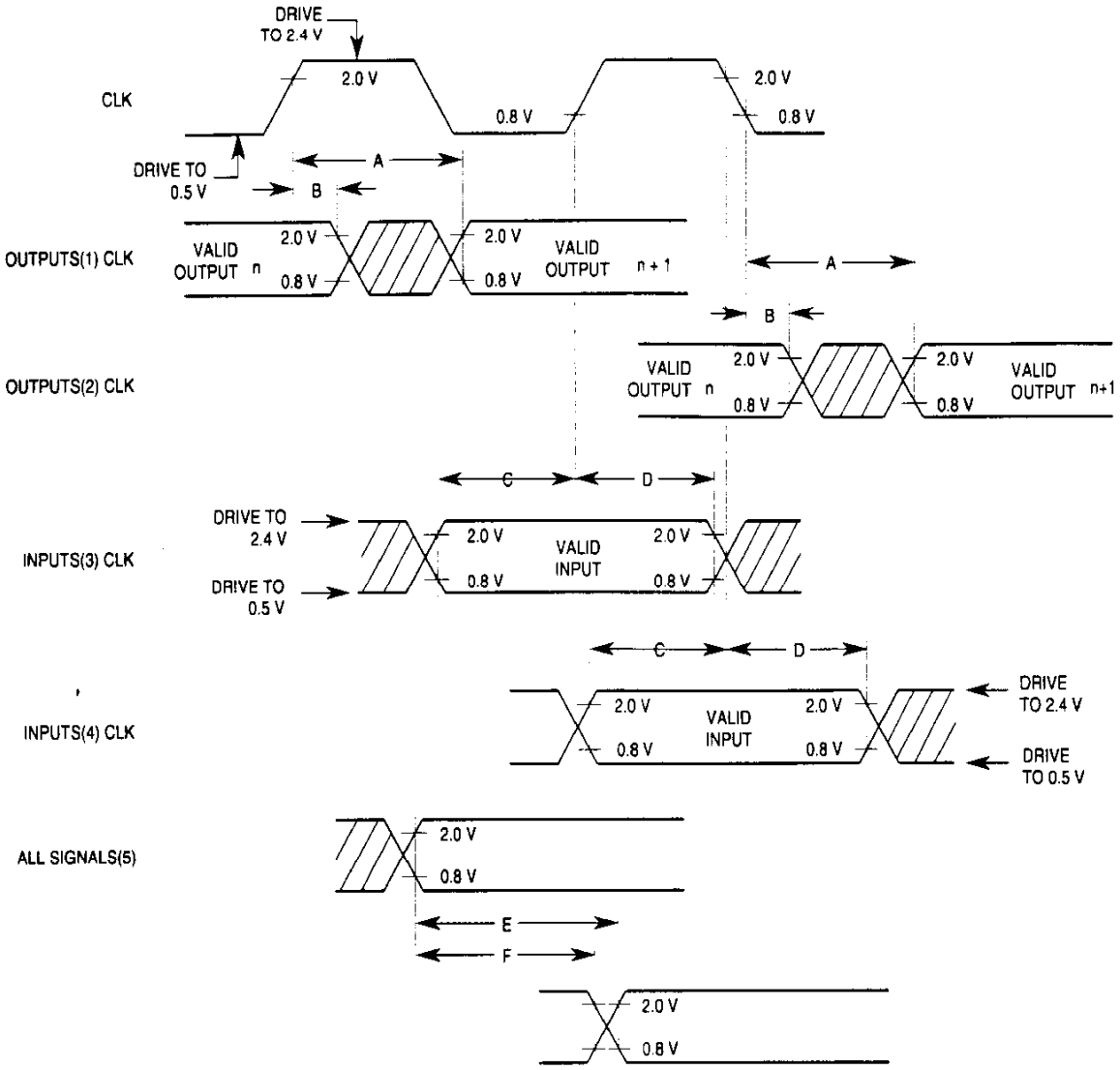
The measurement of the AC specifications is defined by the waveforms shown in Figure 3. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in the figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications is shown.

Note that the testing levels used to verify conformance to the AC specifications do not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.

The MC68330V low voltage parts can operate up to 8.39 MHz or 16.78 MHz with a 3.3 V ±0.3 V supply. Separate part numbers are used to distinguish the operation of the parts according to the supply voltage. MC68330 is used throughout the specifications to refer to the 16.78- or 25.16-MHz parts at 5.0 V ±5%. MC68330V is used throughout the specifications to refer to the 8.39- or 16.78-MHz parts at 3.3 V ±0.3 V.

NOTE

The electrical specifications for the MC68330 25.16 MHz at 5.0 V ±5% and the 3.3 V ±0.3 V specifications for both the 8.39- and 16.78-MHz parts are preliminary.



NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 3. Drive Levels and Test Points for AC Specifications

DC ELECTRICAL SPECIFICATIONS (See notes (a), (b), (c) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70°C; see numbered notes.)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage (Except Clock)	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	V
Clock Input High Voltage (EXTAL, X1)	V_{IHC}	0.7 * V_{CC}	V_{CC} + 0.3	V
Undershoot	—	—	–0.8	V
Input Leakage Current (All Input-Only Pins) V_{in} = V_{CC} or GND	I_{in}	–2.5	2.5	µA
Hi-Z(Off-State) Leakage Current (All Non-Crystal Outputs and I/O Pins—See Note 1) V_{in} = 0.5/2.4 V	I_{OZ}	–20	20	µA
Signal Low Input Current V_{IL} = 0.8 V TMS, TDI Signal High Input Curent V_{IH} = 2.0 V TMS, TDI	I_L I_H	–0.2 –0.2	–0.015 –0.015	mA mA
Output High Voltage (See Notes 1 and 2) I_{OH} = –0.8 mA, V_{CC} = 4.75 V (All Non-Crystal Outputs except $\overline{HALT}$, $\overline{RESET}$)	V_{OH}	2.4	—	V
Output Low Voltage (See Note 1) I_{OL} = 2.0 mA CLKOUT, FREEZE, $\overline{IPIPE}$, $\overline{IFETCH}$ I_{OL} = 3.2 mA A23–A0, D15–D0, FC2–FC0, SIZ1, SIZ0 I_{OL} = 5.3 mA All Other Output-Only and Group 2 I/O Pins I_{OL} = 15.3 mA $\overline{HALT}$, $\overline{RESET}$	V_{OL}	—	 0.5 0.5 0.5 0.5	V
Total Supply Current at 5 V ±5% @ 16.78 MHz RUN (see Note 3) STOP (VCO Off)	 I_{CC} S_{ICC}	—	 120 300	 mA µA
Power Dissipation at 5 V ±5% @ 16.78 MHz	P_D	—	630	mW
Total Supply Current at 3.3 V ±0.3 V @ 8.39 MHz RUN (see Note 4) STOP (VCO Off)	 I_{CC} S_{ICC}	—	 TBD TBD	 mA µA
Power Dissipation at 3.3 V ±0.3 V @ 8.39 MHz	P_D	—	TBD	mW
Input Capacitance (See Notes 1 and 5) All Input-Only Pins All I/O Pins	Cin	—	 10 20	pF
Load Capacitance (See Note 5)	C_L	—	100	pF

NOTES:

(a) The electrical specifications in this document for both the 8.39 and 16.78 MHz @ 3.3 V ±0.3 V are preliminary and apply only to the appropriate MC68330V low-voltage part.

(b) The 25.16 MHz @ 5.0 V ±5% electrical specifications are preliminary.

(c) For extended temperature parts T_A = –40 to +85°C. These specifications are preliminary.

1. Input-Only Pins: $\overline{BERR}$, $\overline{BGACK}$, $\overline{BKPT}$, $\overline{BR}$, $\overline{DSACK1}$, $\overline{DSACK0}$, EXTAL, TCK, TDI, TMS
   Output-Only Pins: A23–A0, $\overline{AS}$, $\overline{BG}$, CLKOUT, $\overline{CS3}$–$\overline{CS1}$, $\overline{DS}$, FC2–FC0, FREEZE, $\overline{IFETCH}$, $\overline{IPIPE}$, $\overline{LWE}$, $\overline{RMC}$, R/$\overline{W}$, SIZ1, SIZ0, TDO, $\overline{UWE}$
   Input/Output Pins:
   Group 1: D15–D0
   Group 2: A31–A24, $\overline{CS0}$, $\overline{IRQ7}$– $\overline{IRQ1}$, MODCK
   Group 3: $\overline{HALT}$, $\overline{RESET}$
2. V_{OH} specification for $\overline{HALT}$ and $\overline{RESET}$ is not applicable because they are open-drain pins.
3. Supply current measured with system clock frequency of 16.78 MHz @ 5.25 V.

4. Supply current measured with system clock frequency of 8.39 MHz @ 3.6 V.
5. Capacitance is periodically sampled rather than 100% tested.

AC ELECTRICAL SPECIFICATIONS CONTROL TIMING (See notes (a), (b), (c) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70°C; see numbered notes; see Figure 4.)

Num	Characteristic	Symbol	3.3 V 8.39 MHz		3.3 V or 5.0 V 16.78 MHz		5.0 V 25.16 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	System Frequency[1]	f_{sys}	dc	8.39	dc	16.78	dc	25.16	MHz
	Crystal Frequency	f_{XTAL}	25	50	25	50	25	50	kHz
	On-Chip VCO System Frequency	f_{sys}	0.13	8.39	0.13	16.78	0.13	25.16	MHz
	On-Chip VCO Frequency Range	f_{VCO}	0.1	16.78	0.1	33.5	0.1	50.3	MHz
	External Clock Operation	f_{sys}	0	8.39	0	16.78	0	25.16	MHz
	PLL Start-up Time[2]	t_{rc}	—	20	—	20	—	20	ms
	Limp Mode Clock Frequency[3] SYNCR X-bit = 0 SYNCR X-bit = 1	f_{limp}	— —	$f_{sys}/2$ f_{sys}	— —	$f_{sys}/2$ f_{sys}	— —	$f_{sys}/2$ f_{sys}	kHz
	CLKOUT stability[4]	Δ_{CLK}	−1	+1	−1	+1	−1	+1	%
1[5]	CLKOUT Period in Crystal Mode	t_{cyc}	119.2	—	59.6	—	39.7	—	ns
1B[6]	External Clock Input Period	t_{EXTcyc}	119.2	—	59.6	—	39.7	—	ns
1C[7]	External Clock Input Period with PLL	t_{EXTcyc}	119.2	—	59.6	—	39.7	—	ns
2,3[8]	CLKOUT Pulse Width in Crystal Mode	t_{CW}	56	—	28	—	18.7	—	ns
2B, 3B[9]	CLKOUT Pulse Width in External Mode	t_{EXTCW}	53.6	—	26.8	—	17.9	—	ns
2C, 3C[10]	CLKOUT Pulse Width in External w/PLL Mode	t_{EXTCW}	59.6	—	29.8	—	19.9	—	ns
4,5	CLKOUT Rise and Fall Times	t_{Crf}	—	10	—	5	—	4	ns

NOTES:

(a) The electrical specifications in this document for both the 8.39 and 16.78 MHz @ 3.3 V ±0.3 V are preliminary and apply only to the appropriate MC68330V low-voltage part.

(b) The 25.16 MHz @ 5.0 V ±5% electrical specifications are preliminary.

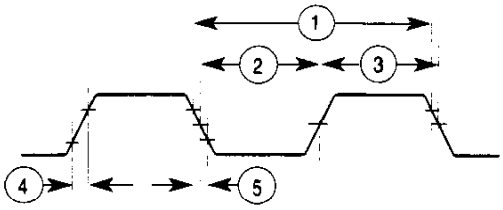
(c) For extended-temperature parts, T_A = −40 to +85°C. These specifications are preliminary.

1. All internal registers retain data at 0 Hz.
2. Assumes that a stable V_{CCSYN} is applied, that an external filter capacitor with a value of 0.1 µF is attached to the XFC pin, and that the crystal oscillator is stable. Lock time is measured from power-up to $\overline{\text{RESET}}$ release. This specification also applies to the period required for PLL lock after changing the W and Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after LPSTOP.
3. Determined by the initial control voltage applied to the on-chip VCO. The X-bit in the SYNCR controls a divide-by-two scaler on the system clock output.
4. CLKOUT stability is the average deviation from programmed frequency measured at maximum f_{sys}. Measurement is made with a stable external clock input applied using the PLL.
5. All crystal mode clock specifications are based on using a 32.768-kHz crystal for the input.
6. When using the external clock input mode (MODCK reset value = 0 V), the minimum allowable t_{EXTcyc} period will be reduced when the duty cycle of the signal applied to EXTAL exceeds 5% tolerance. The relationship between external clock input duty cycle and minimum t_{EXTcyc} is expressed:

   Minimum t_{EXTcyc} period = minimum t_{EXTCW} / (50% − external clock input duty cycle tolerance).

   Minimum external clock low and high times are based on a 45% duty cycle.
7. When using the external clock input mode with the PLL (MODCK reset value = 0 V), the external clock input duty cycle can be at a minimum 20% to produce a CLKOUT with a 50% duty cycle.
8. For crystal mode operation, the minimum CLKOUT pulse width is based on a 47% duty cycle.
9. For external clock mode operation, the minimum CLKOUT pulse width is based on a 45% duty cycle, with a 50% duty cycle input clock.
10. For external clock w/PLL mode operation, the minimum CLKOUT pulse width is based on a 50% duty cycle.

11. For external clock mode, there is a 10–40 ns skew between the input clock signal and the output CLKOUT signal from the MC68330. Clock skew is measured from the rising edges of the clock signals.
12. For external clock mode w/PLL, there is a 5 ns skew between the input clock signal and the output CLKOUT signal from the MC68330. Clock skew is measured from the rising edges of the clock signals.



NOTES: 1. All timing except two and three is measured with respect to 0.8 V and 2.0 V.
2. Two and three are measured from 1.5 V to 1.5 V.

Figure 4. Clock Output Timing Diagram

AC TIMING SPECIFICATIONS (See notes (a), (b), (c) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70°C; see numbered notes; see Figures 5–14.)

Num	Characteristic	Symbol	3.3 V		3.3 V/ 5.0 V		5.0 V		Unit
			8.39 MHz		16.78 MHz		25.16 MHz		
			Min	Max	Min	Max	Min	Max	
6	CLKOUT High to Address, FC, SIZ, $\overline{RMC}$ Valid	t_{CHAV}	0	60	0	30	0	20	ns
7	CLKOUT High to Address, Data, FC, SIZ, $\overline{RMC}$ High Impedance	t_{CHAZx}	0	120	0	60	0	40	ns
8	CLKOUT High to Address, FC, SIZ, $\overline{RMC}$ Invalid	t_{CHAZn}	0	—	0	—	0	—	ns
9[9]	CLKOUT Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{IFETCH}$, $\overline{IPIPE}$, $\overline{IACKx}$ Asserted	t_{CLSA}	3	60	3	30	3	20	ns
9A[2]	$\overline{AS}$, $\overline{CS}$ to $\overline{DS}$ Asserted (Read)	t_{STSA}	–30	30	–15	15	–6	6	ns
11	Address, FC, SIZ, $\overline{RMC}$ Valid to $\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read), $\overline{UWE}$, $\overline{LWE}$ Asserted	t_{AVSA}	30	—	15	—	10	—	ns
12	CLKOUT Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{IFETCH}$, $\overline{IPIPE}$, $\overline{IACKx}$ Negated	t_{CLSN}	3	60	3	30	3	20	ns
13	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{IACKx}$ Negated to Address, FC, SIZ Invalid (Address Hold)	t_{SNAI}	30	—	15	—	10	—	ns
14	$\overline{AS}$, $\overline{CS}$, $\overline{UWE}$, $\overline{LWE}$, (and $\overline{DS}$ Read) Width Asserted	t_{SWA}	200	—	100	—	70	—	ns
14A	$\overline{DS}$ Width Asserted (Write)	t_{SWAW}	90	—	45	—	30	—	ns
14B	$\overline{AS}$, $\overline{CS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{IACKx}$ (and $\overline{DS}$Read) Width Asserted (Fast Termination Cycle)	t_{SWDW}	80	—	40	—	30	—	ns
15[3]	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{UWE}$, $\overline{LWE}$ Width Negated	t_{SN}	80	—	40	—	30	—	ns
16	CLKOUT High to $\overline{AS}$, $\overline{DS}$, $\overline{UWE}$, $\overline{LWE}$, R/$\overline{W}$ High Impedance	t_{CHSZ}	—	120	—	60	—	40	ns
17	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{UWE}$, $\overline{LWE}$ Negated to R/$\overline{W}$ High	t_{SNRN}	30	—	15	—	10	—	ns
18	CLKOUT High to R/$\overline{W}$ High	t_{CHRH}	0	60	0	30	0	20	ns
20	CLKOUT High to R/$\overline{W}$ Low	t_{CHRL}	0	60	0	30	0	20	ns
21[9]	R/$\overline{W}$ High to $\overline{AS}$, $\overline{CS}$ Asserted	t_{RAAA}	30	—	15	—	10	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	t_{RASA}	140	—	70	—	47	—	ns
23	CLKOUT High to Data-Out Valid	t_{CHDO}	—	60	—	30	—	20	ns
24	Data-Out Valid to Negating Edge of $\overline{AS}$, $\overline{CS}$, $\overline{UWE}$, $\overline{LWE}$ (Fast Termination Write)	t_{DVASN}	30	—	15	—	10	—	ns
25	$\overline{DS}$, $\overline{CS}$, Negated to Data-Out Invalid (Data-Out Hold)	t_{SNDOI}	30	—	15	—	10	—	ns
26	Data-Out Valid to $\overline{DS}$ Asserted (Write)	t_{DVSA}	30	—	15	—	10	—	ns
27	Data-In Valid to CLKOUT Low (Data Setup)	t_{DICL}	10	—	5	—	5	—	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$, $\overline{BKPT}$ Asserted to CLKOUT Low (Setup Time)	t_{BELCL}	40	—	20	—	10	—	ns
28	$\overline{AS}$, $\overline{DS}$, $\overline{UWE}$, $\overline{LWE}$ Negated to $\overline{DSACKx}$ $\overline{BERR}$, $\overline{HALT}$ Negated	t_{SNDN}	0	160	0	80	0	50	ns
29[4]	$\overline{DS}$, $\overline{CS}$ Negated to Data-In Invalid (Data-In Hold)	t_{SNDI}	0	—	0	—	0	—	ns
29A[4]	$\overline{DS}$, $\overline{CS}$ Negated to Data-In High Impedance	t_{SHDI}	—	120	—	60	—	40	ns

AC TIMING SPECIFICATIONS (Continued)

Num	Characteristic	Symbol	3.3 V		3.3 V/5.0 V		5.0 V		Unit
			8.39 MHz		16.78 MHz		25.16 MHz		
			Min	Max	Min	Max	Min	Max	
30[4]	CLKOUT Low to Data-In Invalid (Fast Termination Hold)	t_{CLDI}	30	—	15	—	10	—	ns
30A[4]	CLKOUT Low to Data-In High Impedance	t_{CLDH}	—	180	—	90	—	60	ns
31[5]	$\overline{DSACKx}$ Asserted to Data-In Valid	t_{DADI}	—	100	—	50	—	32	ns
31A	$\overline{DSACKx}$ Asserted to $\overline{DSACKx}$ Valid (Skew)	t_{DADV}	—	60	—	30	—	20	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	t_{HRrf}	—	400	—	200	—	140	ns
33	CLKOUT Low to $\overline{BG}$ Asserted	t_{CLBA}	—	60	—	30	—	20	ns
34	CLKOUT Low to $\overline{BG}$ Negated	t_{CLBN}	—	60	—	30	—	20	ns
35[6]	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	t_{BRAGA}	1	—	1	—	1	—	CLKOUT
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2.5	1	2.5	1	2.5	CLKOUT
39	$\overline{BG}$ Width Negated	t_{GH}	2	—	2	—	2	—	CLKOUT
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	—	1	—	1	—	CLKOUT
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	300	—	150	—	100	—	ns
46A	R/$\overline{W}$ Width Asserted (Fast Termination Write or Read)	t_{RWAS}	180	—	90	—	60	—	ns
47A[8]	Asynchronous Input Setup Time	t_{AIST}	15	—	8, 5	—	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	30	—	15	—	10	—	ns
48[5,7]	$\overline{DSACKx}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted	t_{DABA}	—	60	—	30	—	20	ns
53	Data-Out Hold from CLKOUT High	t_{DOCH}	0	—	0	—	0	—	ns
54	CLKOUT High to Data-Out High Impedance	t_{CHDH}	—	60	—	30	—	20	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RADC}	80	—	40	—	25	—	ns
56	RESET Pulse Width (Reset Instruction)	t_{HRPW}	512	—	512	—	512	—	CLKOUT
56A	$\overline{RESET}$ Pulse Width (Input from External Device)	t_{RPWI}	590	—	590	—	590	—	CLKOUT
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	t_{BNHN}	0	—	0	—	0	—	ns
70	CLKOUT Low to Data Bus Driven (Show Cycle)	t_{SCLDD}	0	60	0	30	0	20	ns
71	Data Setup Time to CLKOUT Low (Show Cycle)	t_{SCLDS}	30	—	15	—	10	—	ns
72	Data Hold from CLKOUT Low (Show Cycle)	t_{SCLDH}	20	—	10	—	6	—	ns
80	DSI Input Setup Time	t_{DSISU}	30	—	15	—	10	—	ns
81	DSI Input Hold Time	t_{DSIH}	20	—	10	—	6	—	ns
82	DSCLK Setup Time	t_{DSCSU}	30	—	15	—	10	—	ns
83	DSCLK Hold Time	t_{DSCH}	20	—	10	—	6	—	ns
84	DSO Delay Time	t_{DSOD}	—	t_{cyc} + 50	—	t_{cyc} + 25	—	t_{cyc} + 16	ns
85	DSCLK Cycle	t_{DSCCYC}	2	—	2	—	2	—	CLKOUT

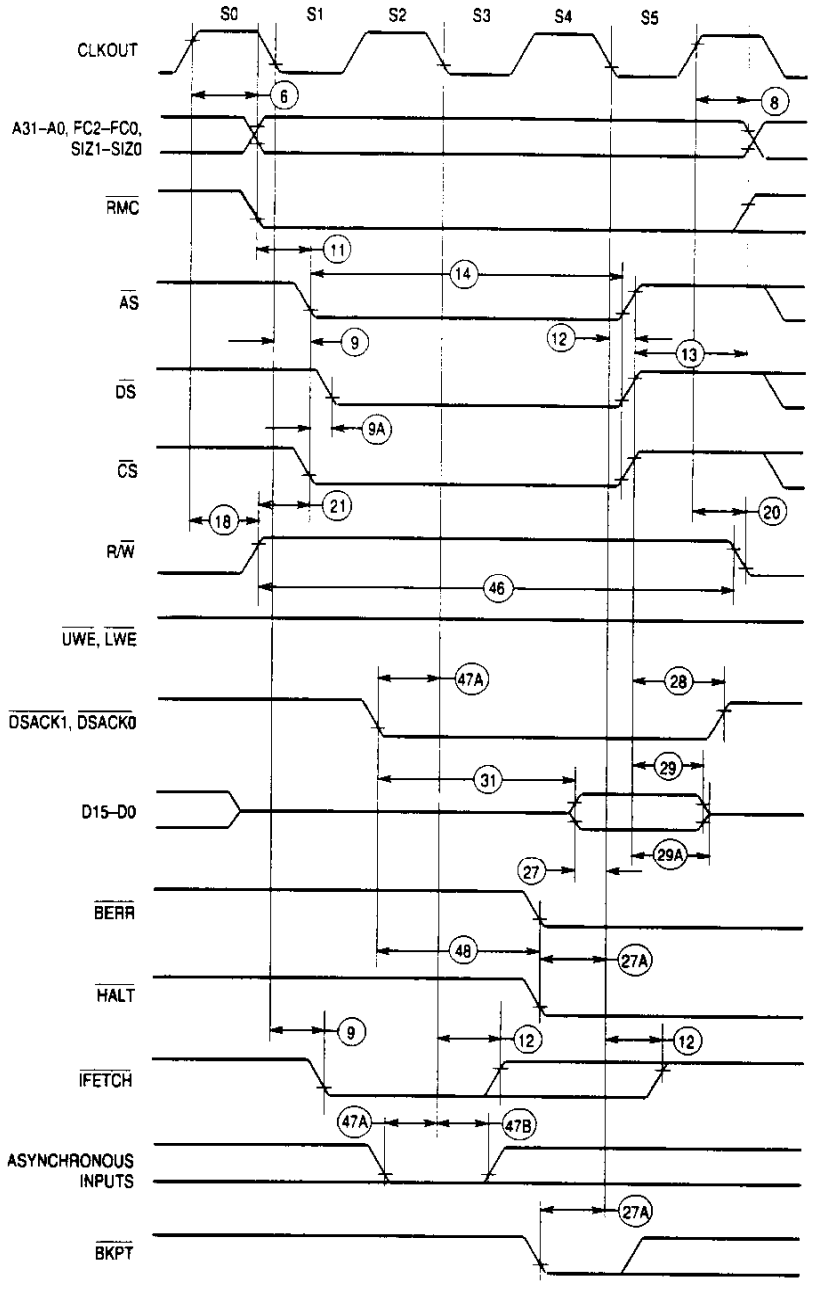
AC TIMING SPECIFICATIONS (Concluded)

Num	Characteristic	Symbol	3.3 V		3.3 V/ 5.0 V		5.0 V		Unit
			8.39 MHz		16.78 MHz		25.16 MHz		
			Min	Max	Min	Max	Min	Max	
86	CLKOUT High to FREEZE Asserted	t_{FRZA}	0	100	0	50	0	35	ns
87	CLKOUT High to FREEZE Negated	t_{FRZN}	0	100	0	50	0	35	ns
88	CLKOUT High to $\overline{\text{IFETCH}}$ High Impedance	t_{IFZ}	0	100	0	50	0	35	ns
89	CLKOUT High to $\overline{\text{IFETCH}}$ Valid	t_{IF}	0	100	0	50	0	35	ns

NOTES:

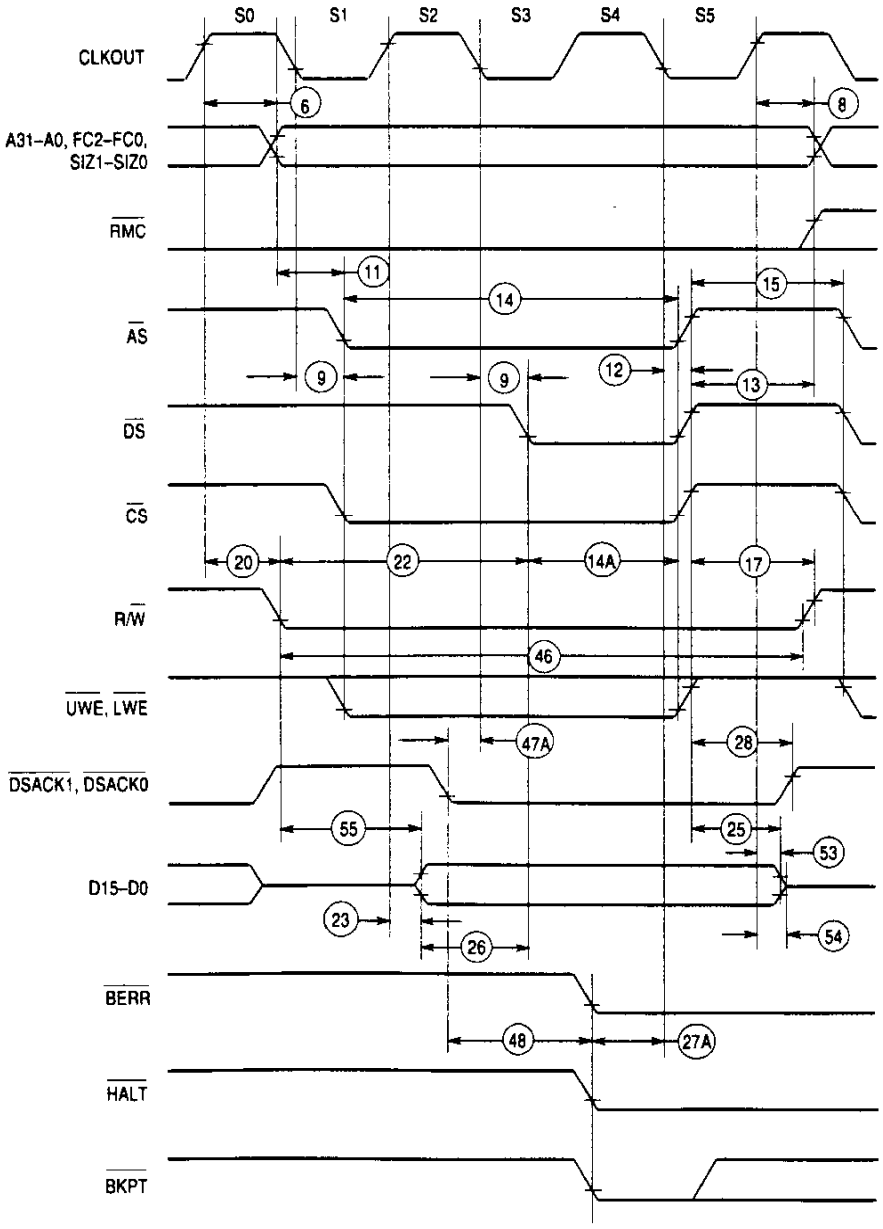
(a) The electrical specifications in this document for both the 8.39 and 16.78 MHz @ 3.3 V ±0.3 V are preliminary and apply only to the appropriate MC68330V low-voltage part.
(b) The 25.16 MHz @ 5.0 V ±5% electrical specifications are preliminary.
(c) For extended-temperature parts, T_A = –40 to +85°C. These specifications are preliminary.

1. All AC timing is shown with respect to 0.8 V and 2.0 V levels unless otherwise noted.
2. This number can be reduced to 5 ns if strobes have equal loads.
3. If multiple chip selects are used, the $\overline{\text{CS}}$ width negated (#15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select.
4. These hold times are specified with respect to $\overline{\text{DS}}$ or $\overline{\text{CS}}$ on asynchronous reads and with respect to CLKOUT on fast termination reads. The user is free to use either hold time for fast termination reads.
5. If the asynchronous setup time (#47) requirements are satisfied, the $\overline{\text{DSACKx}}$ low to data setup time (#31) and $\overline{\text{DSACKx}}$ low to $\overline{\text{BERR}}$ low setup time (#48) can be ignored. The data must only satisfy the data-in to CLKOUT low setup time (#27) for the following clock cycle: $\overline{\text{BERR}}$ must only satisfy the late $\overline{\text{BERR}}$ low to CLKOUT low setup time (#27A) for the following clock cycle.
6. To ensure coherency during every operand transfer, $\overline{\text{BG}}$ will not be asserted in response to $\overline{\text{BR}}$ until after the current operand transfer cycles are complete and $\overline{\text{RMC}}$ is negated.
7. In the absence of $\overline{\text{DSACKx}}$, $\overline{\text{BERR}}$ is an asynchronous input using the asynchronous setup time (#47).
8. Specification #47A for 16.78 MHz @ 3.3 V ±0.3V will be 8 ns.
9. During interrupt acknowledge cycles, up to two wait states may be inserted by the processor between states S0 and S1.



NOTE: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 5. Read Cycle Timing Diagram



NOTE: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 6. Write Cycle Timing Diagram

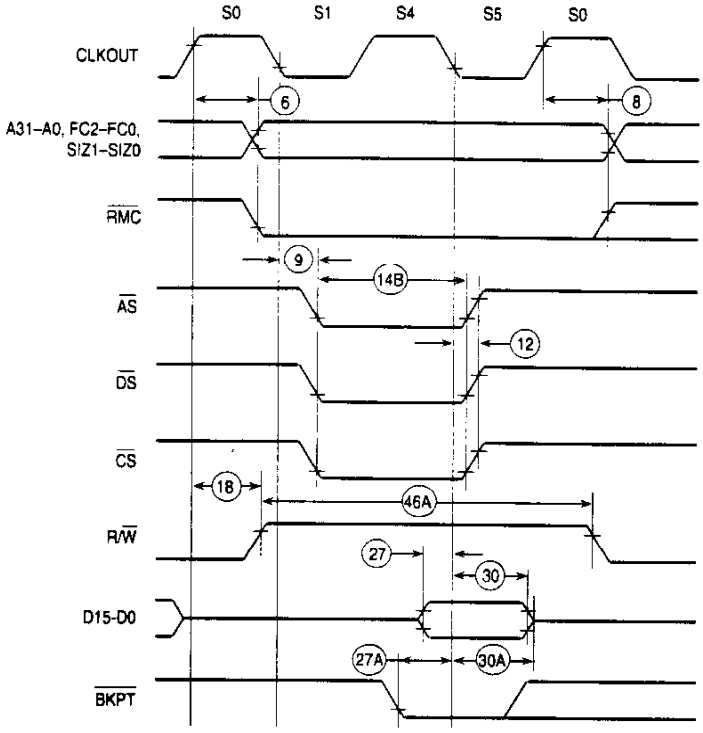


Figure 7. Fast Termination Read Cycle Timing Diagram

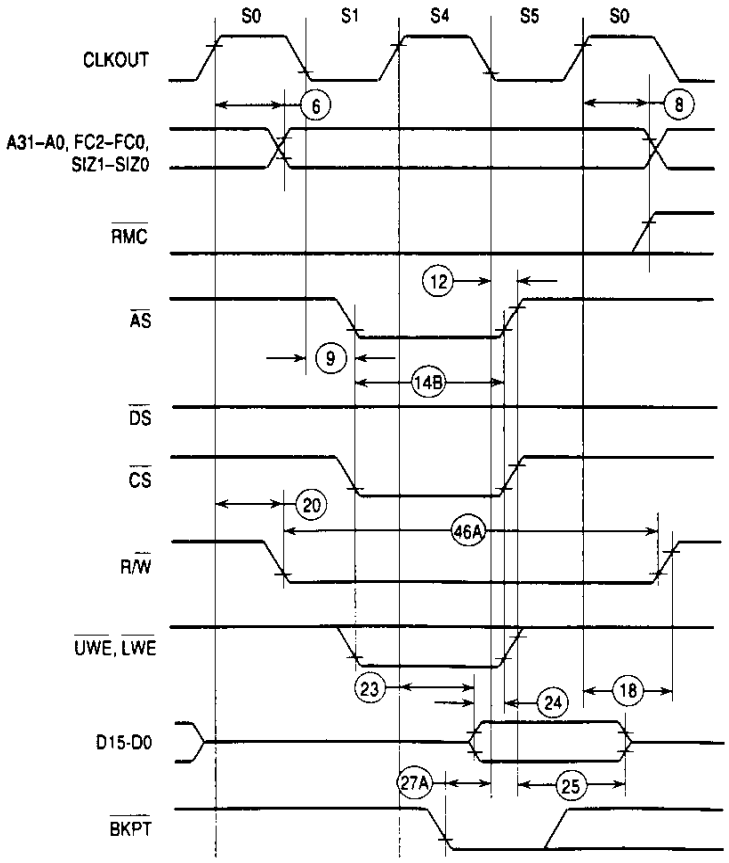


Figure 8. Fast Termination Write Cycle Timing Diagram

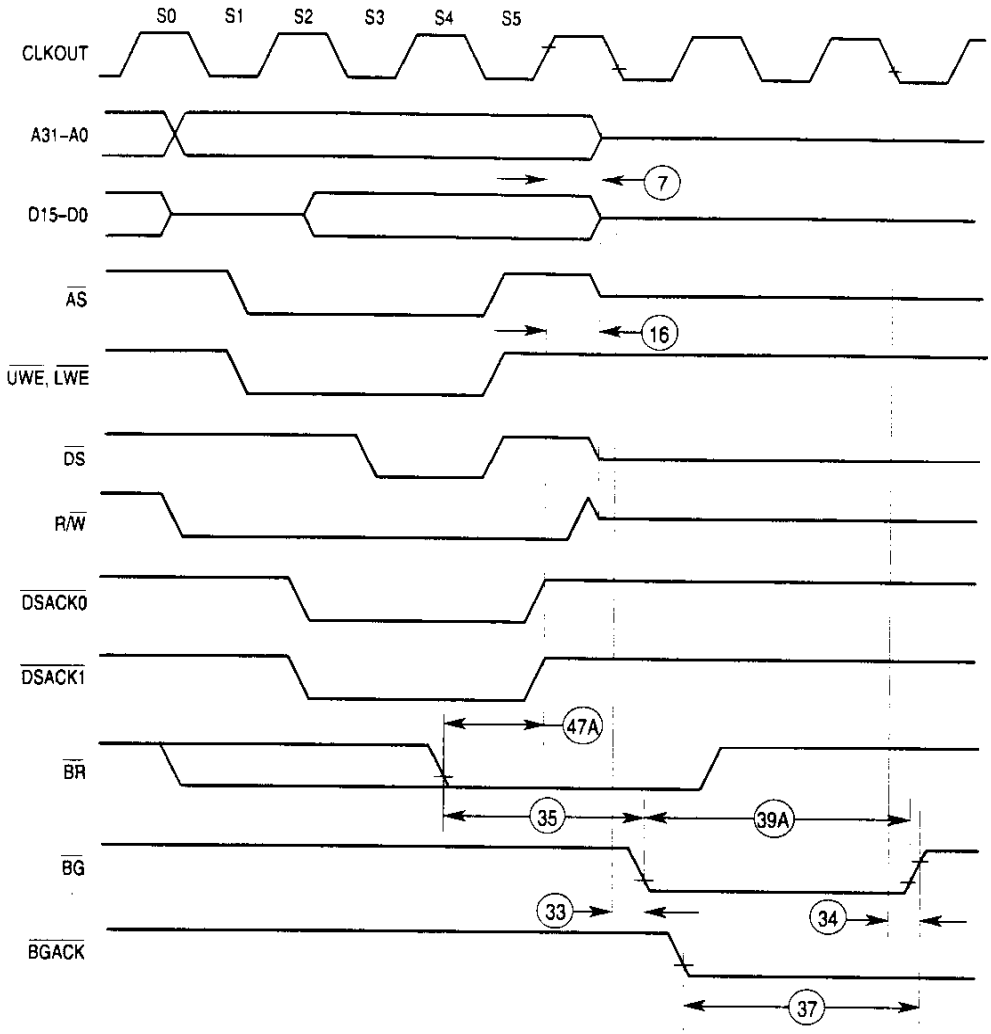


Figure 9. Bus Arbitration Timing—Active Bus Case

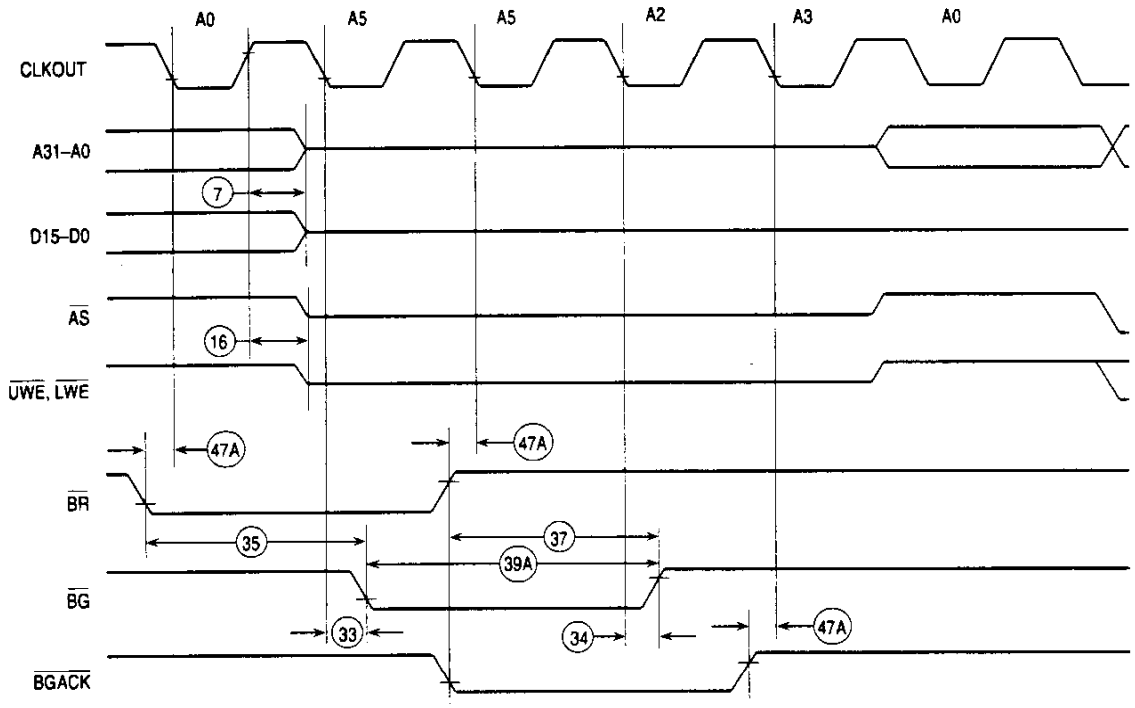


Figure 10. Bus Arbitration Timing—Idle Bus Case

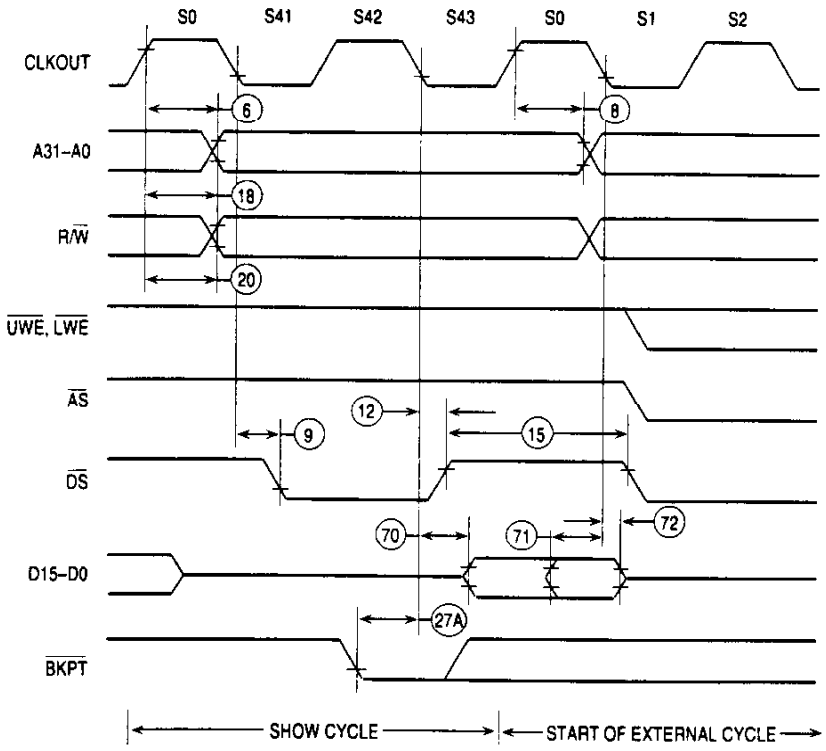
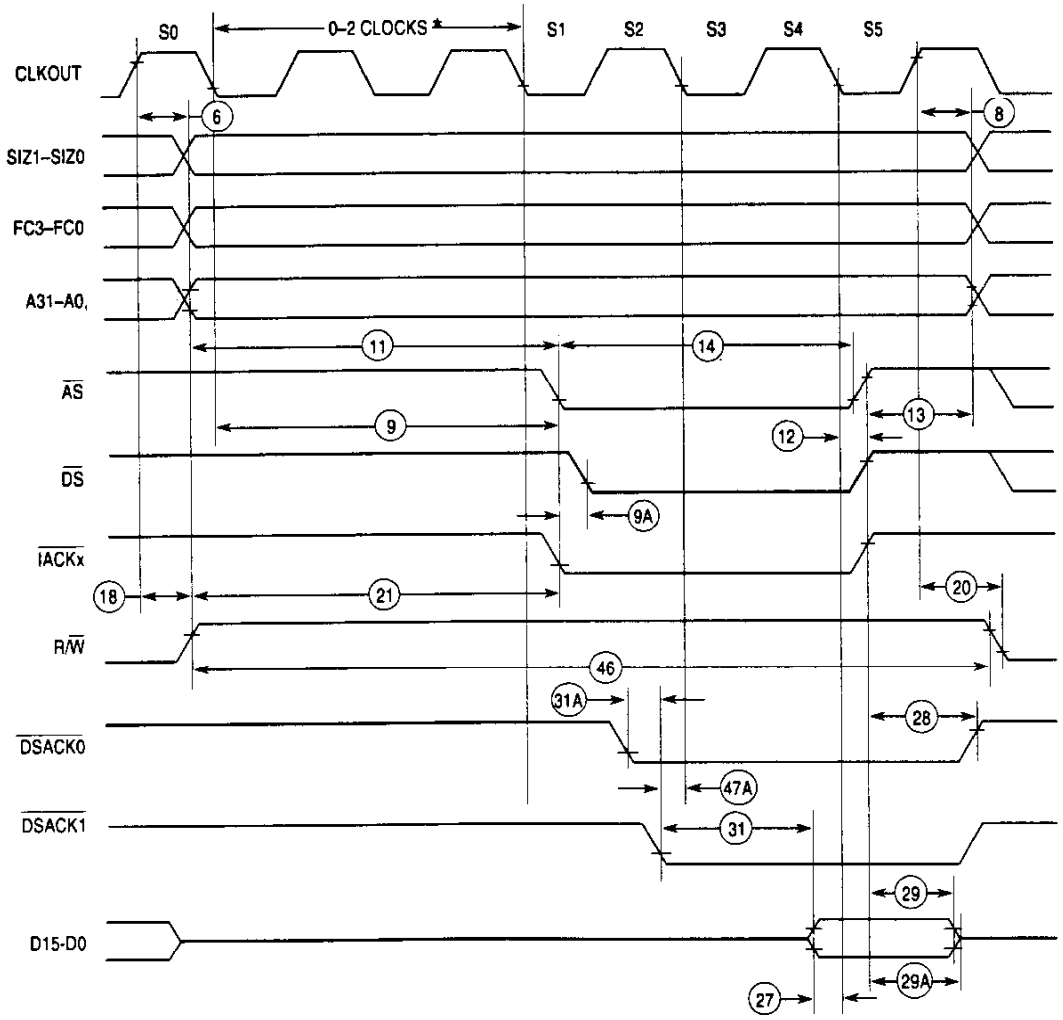


Figure 11. Show Cycle Timing Diagram



*Up to two wait states may be inserted by the processor between states S0 and S1.

Figure 12. IACK Cycle Timing Diagram

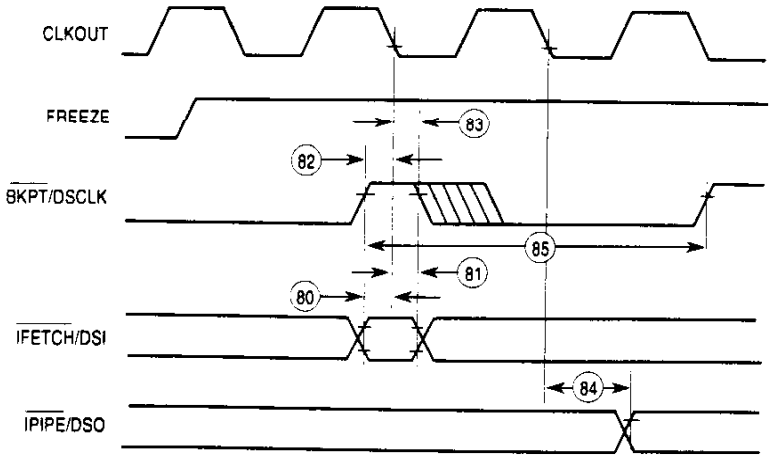


Figure 13. Background Debug Mode Serial Port Timing

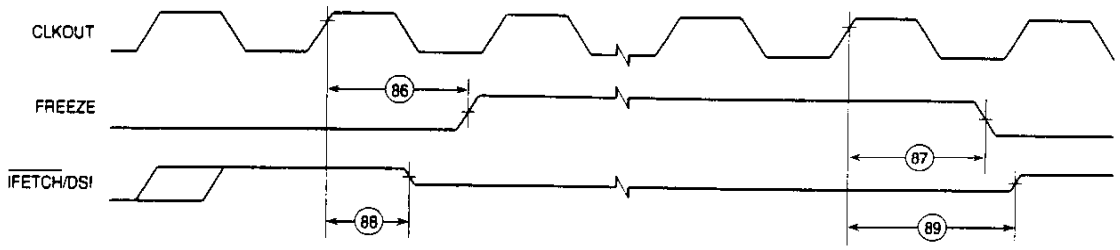


Figure 14. Background Debug Mode FREEZE Timing

IEEE 1149.1 ELECTRICAL SPECIFICATIONS (See notes (a), (b), (c) corresponding to part operation, GND = 0 Vdc, TA = 0 to 70°C; see Figures 15–17.)

Num.	Characteristic	3.3 V 8.39 MHz		3.3 V or 5.0 V 16.78 MHz		5.0 V 25.16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
	TCK Frequency of Operation	0	8.39	0	16.78	0	25.16	MHz
1	TCK Cycle Time in Crystal Mode	119.2	—	59.6	—	39.7	—	ns
2	TCK Clock Pulse Width Measured at 1.5 V	56	—	28	—	18.7	—	ns
3	TCK Rise and Fall Times	0	10	0	5	0	3	ns
6	Boundary Scan Input Data Setup Time	32	—	16	—	10	—	ns
7	Boundary Scan Input Data Hold Time	52	—	26	—	18	—	ns
8	TCK Low to Output Data Valid	0	80	0	40	0	26	ns
9	TCK Low to Output High Impedance	0	120	0	60	0	40	ns
10	TMS, TDI Data Setup Time	30	—	15	—	10	—	ns
11	TMS, TDI Data Hold Time	30	—	15	—	10	—	ns
12	TCK Low to TDO Data Valid	0	50	0	25	0	16	ns
13	TCK Low to TDO High Impedance	0	50	0	25	0	16	ns

NOTES:
(a) The electrical specifications in this document for both the 8.39 and 16.78 MHz @ 3.3 V ±0.3 V are preliminary and apply only to the appropriate MC68330V low-voltage part.
(b) The 25.16 MHz @ 5.0 V ±5% electrical specifications are preliminary.
(c) For extended-temperature parts, T_A = –40 to +85°C. These specifications are preliminary.

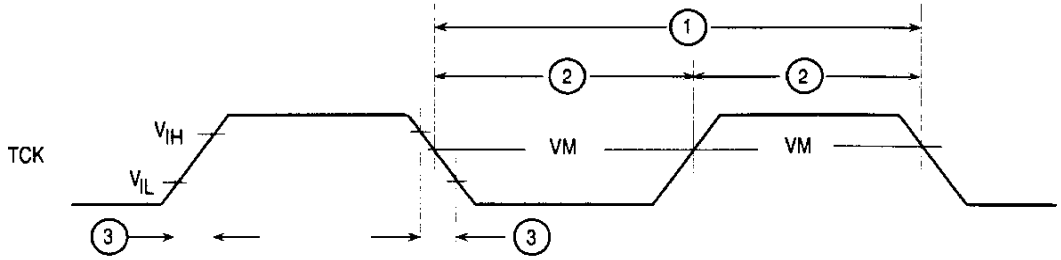


Figure 15. TCK Input Timing Diagram

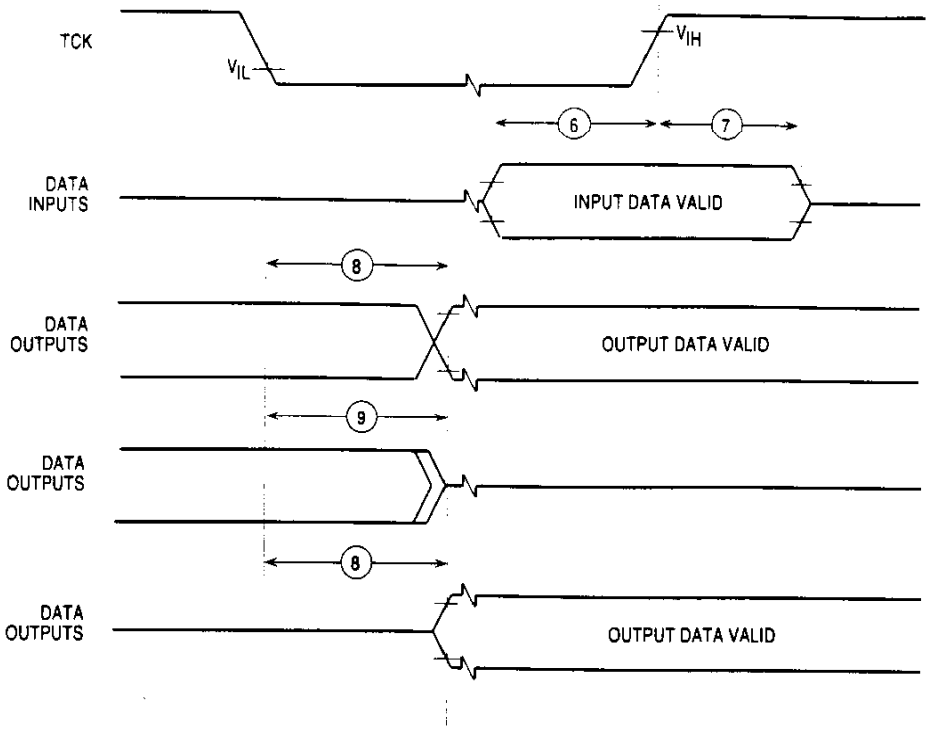


Figure 16. Boundary Scan Timing Diagram

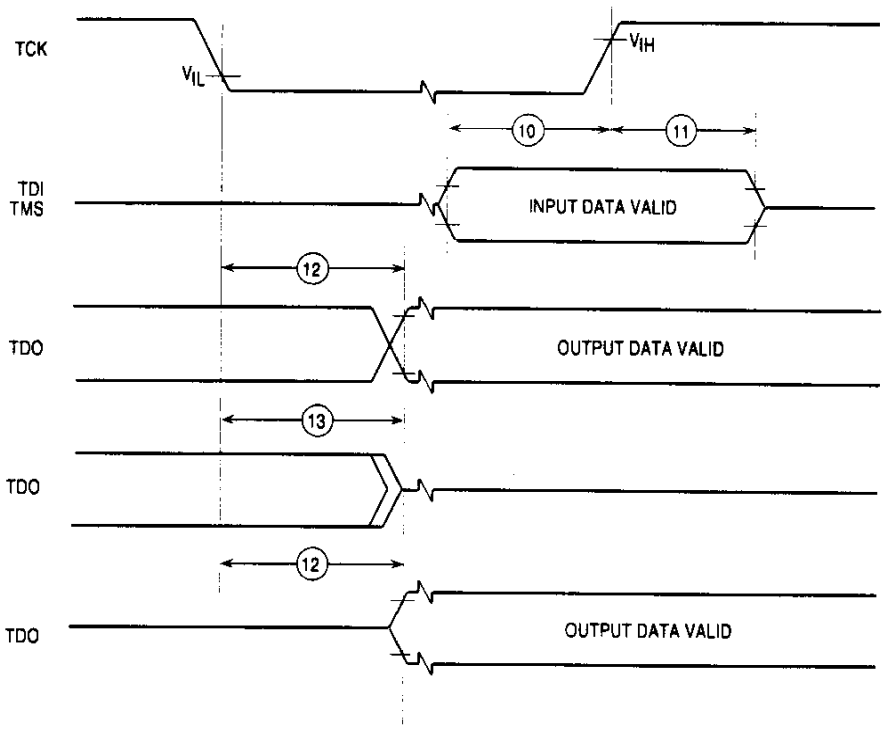


Figure 17. Test Access Port Timing Diagram

ORDERING INFORMATION AND MECHANICAL DATA

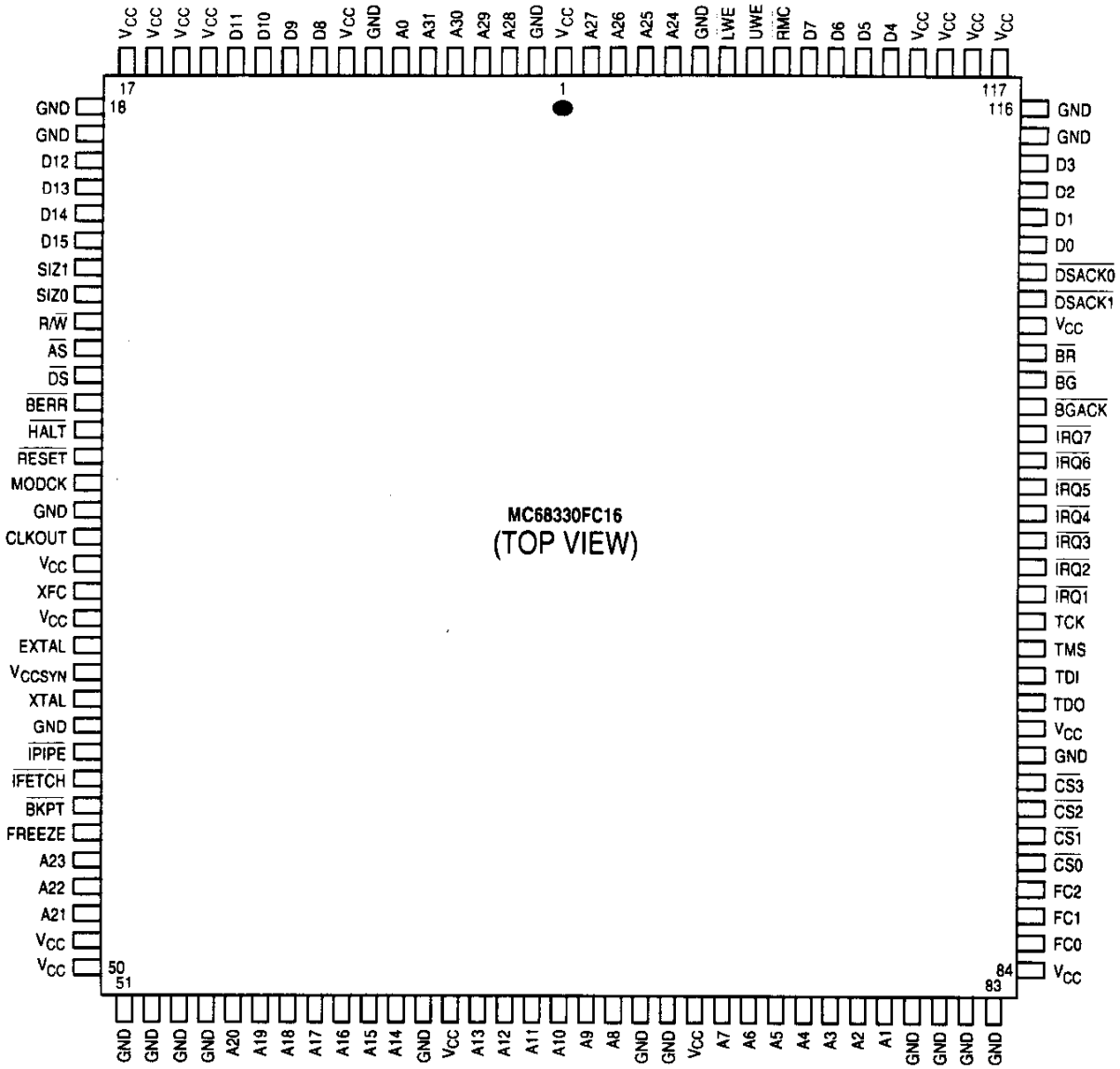
The following paragraphs discuss the ordering information, pin assignments, and package dimensions for the MC68330.

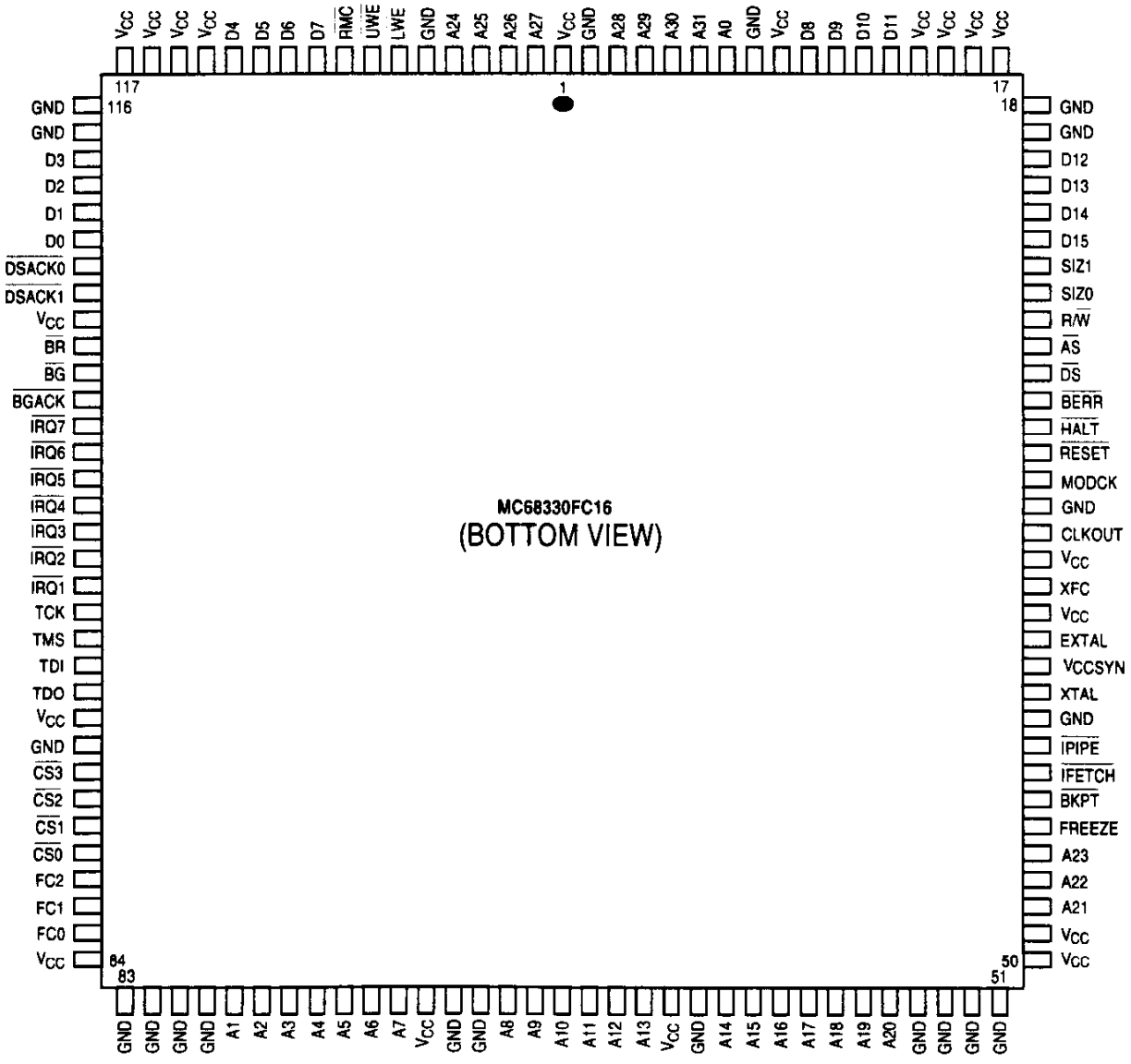
MC68330 ORDERING INFORMATION

Supply Voltage	Package Type	Frequency (MHz)	Temperature	Order Number
5.0 V	Plastic Quad Flat Pack FE Suffix	0–16.78 0–16.78 0–25.16	0°C to +70°C –40°C to +85°C 0°C to +70°C	MC68330FE16 MC68330CFE16 MC68330FE25
5.0 V	Plastic Quad Flat Pack FG Suffix	0–16.78 0–16.78	0°C to +70°C –40°C to +85°C	MC68330FG16 MC68330CFG16
3.3 V	Plastic Quad Flat Pack FE Suffix	0–8.39 0–8.39 0–16.78	0°C to +70°C –40°C to +85°C 0°C to +70°C	MC68330FE8V MC68330CFE8V MC68330FE16V

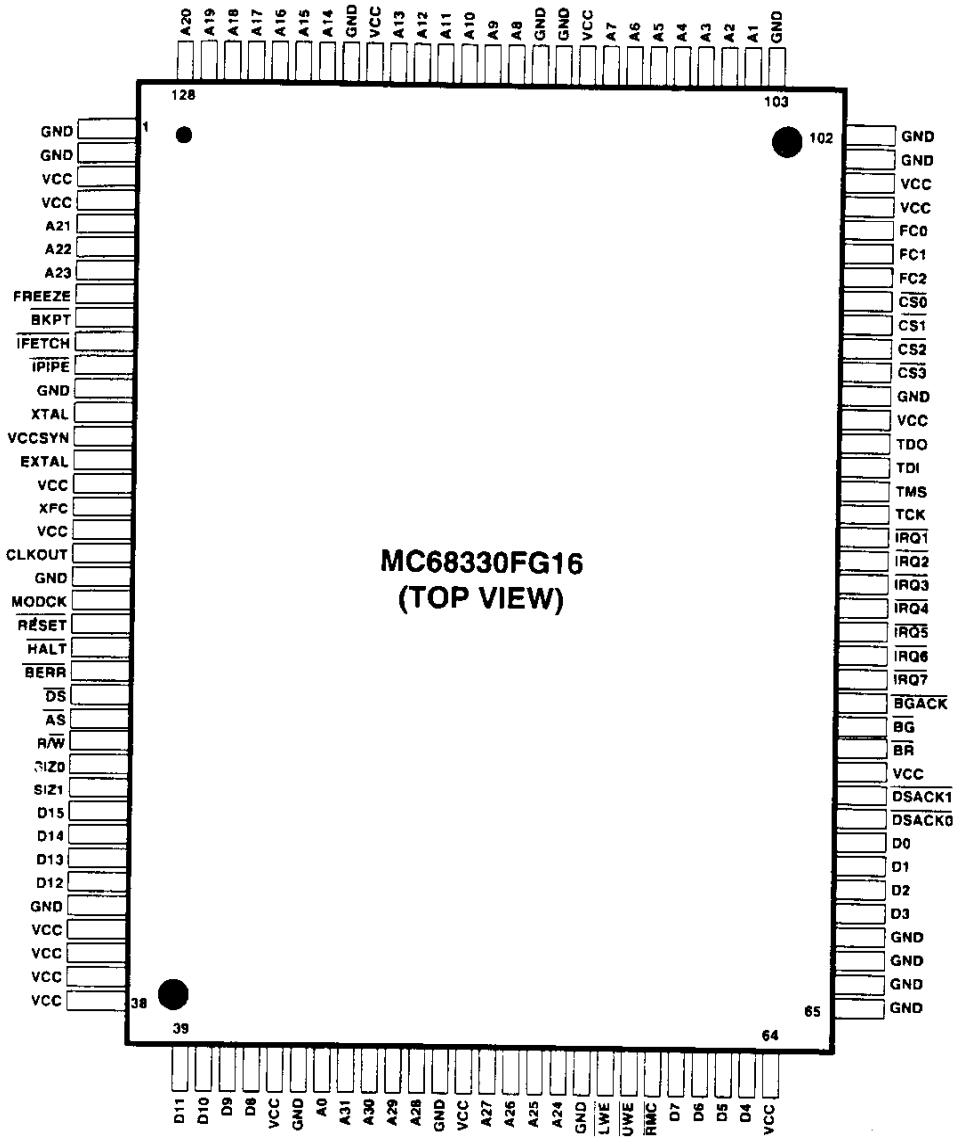
PIN ASSIGNMENTS

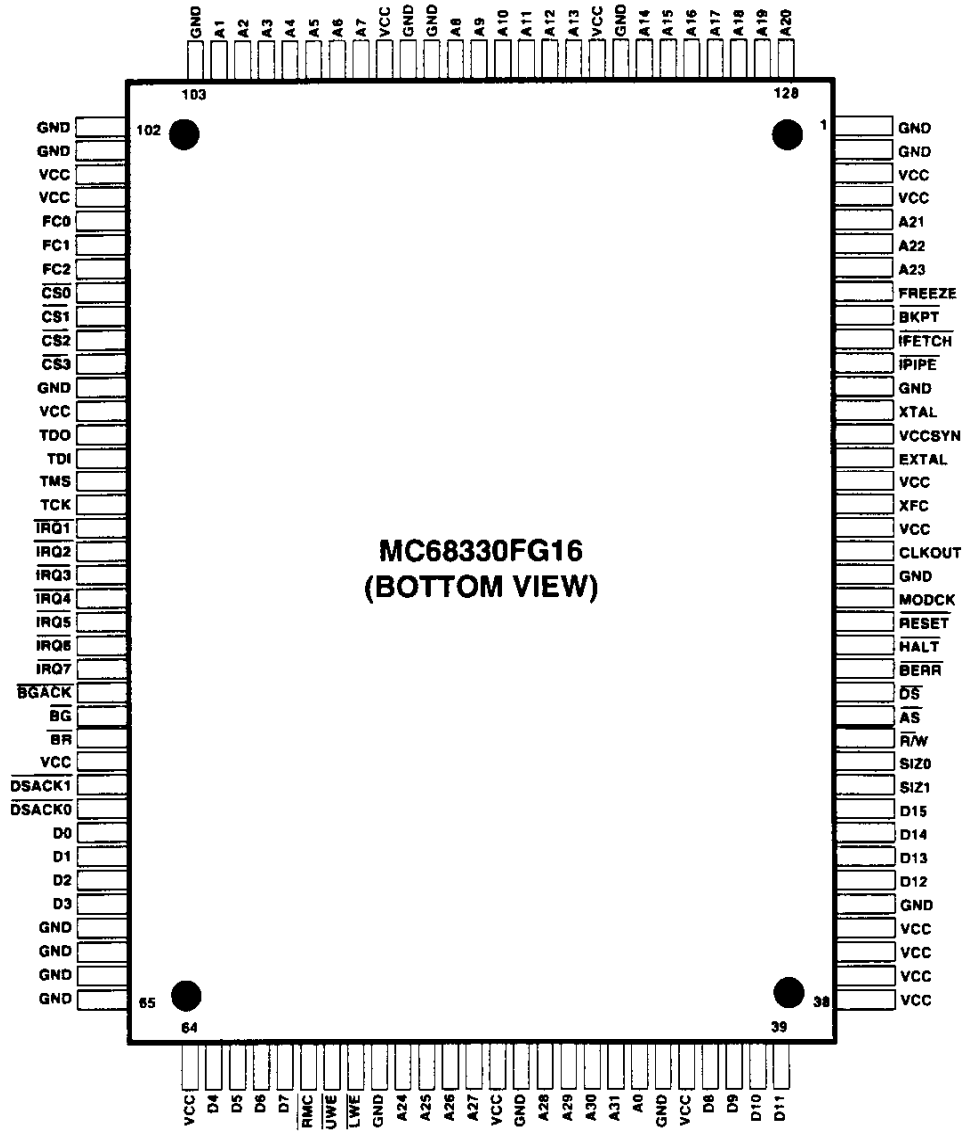
132-PIN PLASTIC QUAD FLAT PACK (FC)





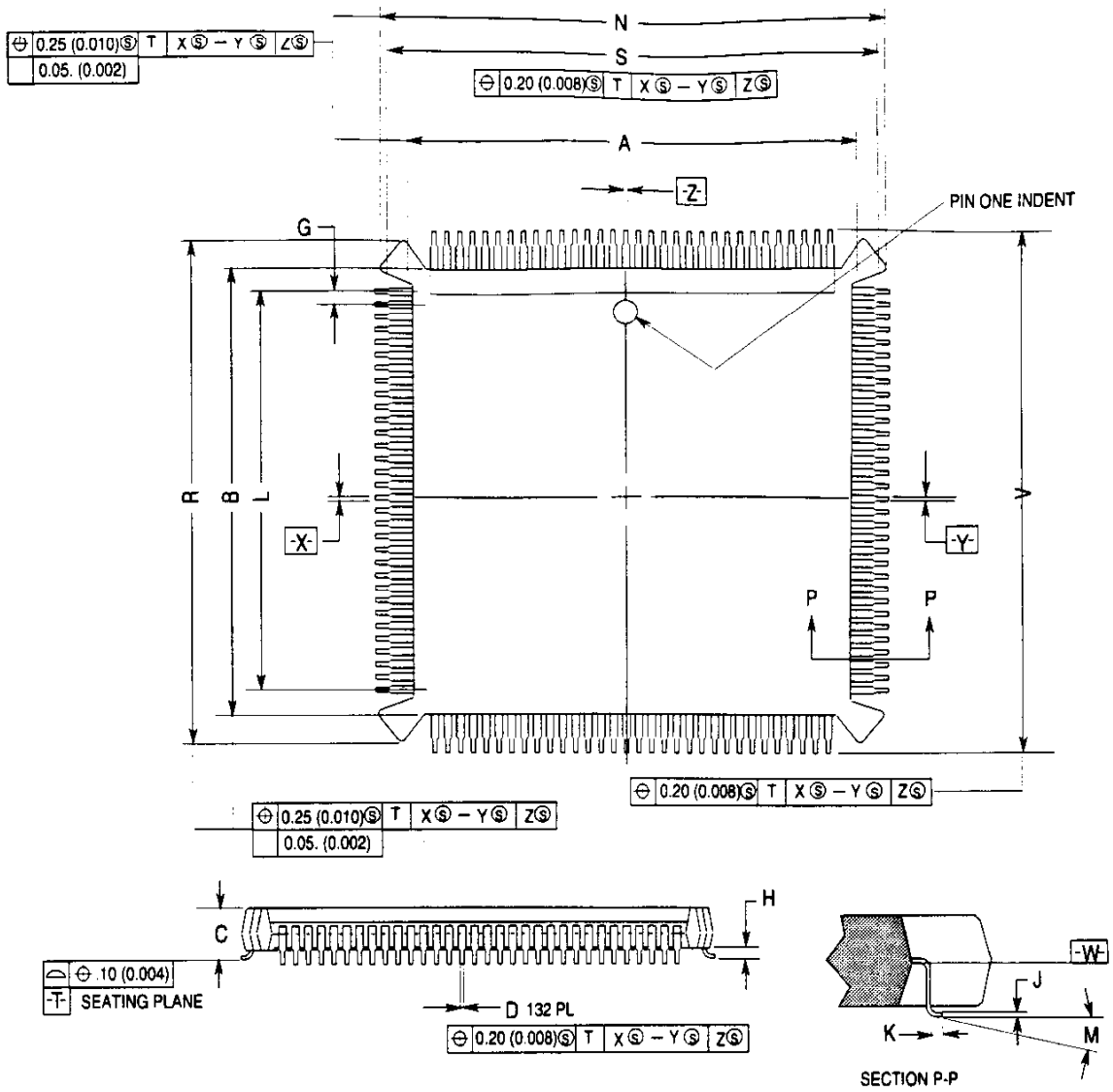
128-PIN PLASTIC QUAD FLAT PACK (FG)





PACKAGE DIMENSIONS

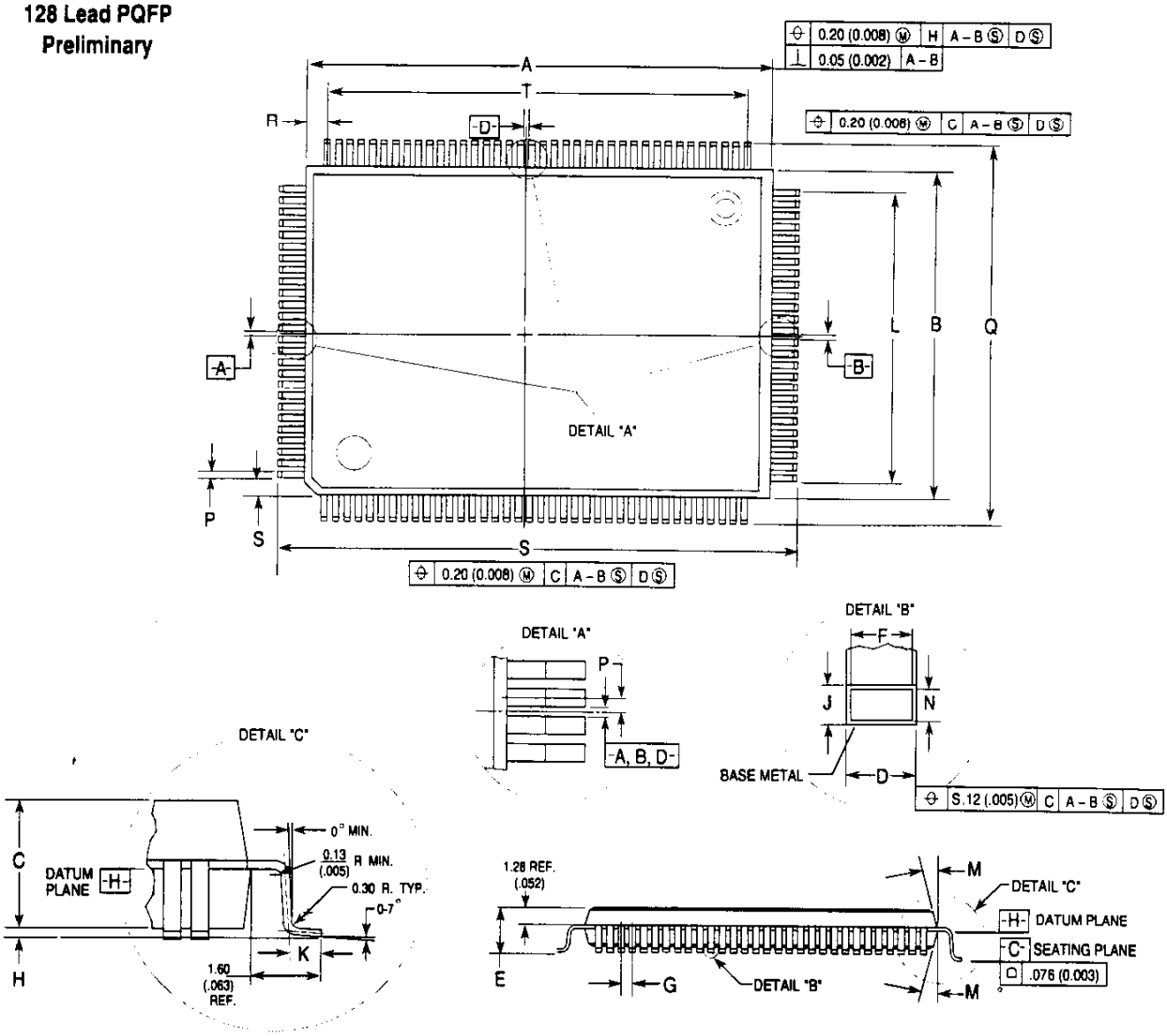
FC SUFFIX



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.06	24.20	0.947	0.953
B	24.06	24.20	0.947	0.953
C	4.07	4.57	0.160	0.180
D	0.21	0.30	0.008	0.012
G	0.64 BSC		0.025 BSC	
H	0.51	1.01	0.020	0.040
J	0.16	0.20	0.006	0.008
K	0.51	0.76	0.020	0.030
M	0°	8°	0°	8°
N	27.88	28.01	1.097	1.103
R	27.88	28.01	1.097	1.103
S	27.31	27.55	1.075	1.085
V	27.31	27.55	1.075	1.085

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. DIM A, B, N, AND R DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION FOR DIMENSIONS A AND B IS 0.25 (0.010), FOR DIMENSIONS N AND R IS 0.18 (0.007).
4. DATUM PLANE -W- IS LOCATED AT THE UNDERSIDE OF LEADS WHERE LEADS EXIT PACKAGE BODY.
5. DATUMS X-Y AND Z TO BE DETERMINED WHERE CENTER LEADS EXIT PACKAGE BODY AT DATUM -W-.
6. DIM S AND V TO BE DETERMINED AT SEATING PLANE, DATUM -T-.
7. DIM A, B, N AND R TO BE DETERMINED AT DATUM PLANE -W-.

FG Suffix
128 Lead PQFP
Preliminary



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.90	20.10	0.783	0.791
B	13.90	14.10	.547	.555
C	2.57	2.87	.101	.113
D	.13	.28	.005	.011
E	—	3.40	—	.134
F	.13	.25	.005	.010
G	0.50 BSC		0.020 BSC	
H	0.25	—	.010	—
J	.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	12.5 REF		.492 REF	
M	12°	16°	12°	16°
N	0.13	0.17	0.005	0.007
P	0.50 BSC		0.20 BSC	
Q	16.95	17.45	.667	.687
R	.75 REF		.029 REF	
S	.75 REF		.029 REF	
T	18.5 REF		.728 REF	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER. INCHES ARE IN "( )".
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B-, AND -D- TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm(0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS BY 0.20(.008) MILLIMETERS.

DOCUMENTATION

The documents listed in the following table contain detailed information on the MC68330. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Document Number	Document Name
BR1114/D	*M68300 Integrated Processor Family*
MC68330UM/AD	*MC68330 User's Manual*
M68000PM/AD	*M68000 Family Programmer's Reference Manual*
AN1063/D	*DRAM Controller for the MC68340*
AN453	*Software Implementation of SPI on the MC68340*
BR573/D	*M68340 Evaluation System Product Brief*
BR729/D	*The 68K Source*
BR1407/D	*3.3 Volt Logic and Interface Circuits*

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

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