

**MC8T26A**  
**(MC6880A)**

**QUAD THREE-STATE BUS TRANSCEIVER**

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the  $-48$  mA driver and  $-20$  mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of  $200 \mu\text{A}$  at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

The MC8T26A is identical to the NE8T26A and it operates from a single  $+5$  V supply.

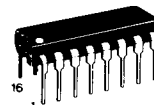
- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

**QUAD THREE-STATE  
 BUS TRANSCEIVER**

**MONOLITHIC SCHOTTKY  
 INTEGRATED CIRCUITS**

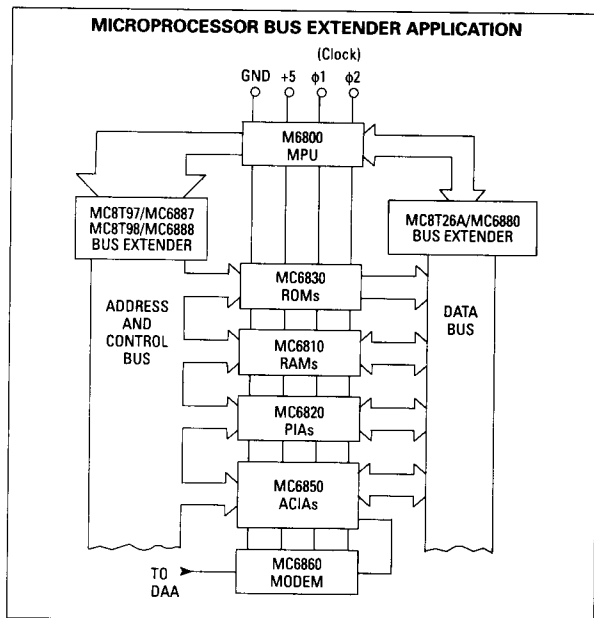


**L SUFFIX**  
 CERAMIC PACKAGE  
 CASE 620

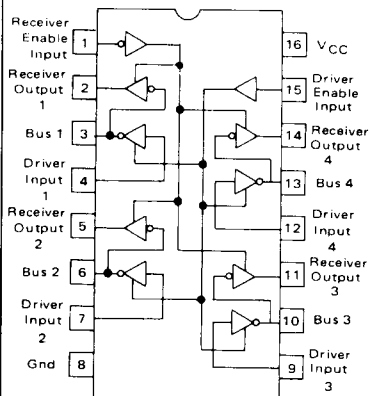


**P SUFFIX**  
 PLASTIC PACKAGE  
 CASE 648

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**PIN CONNECTIONS — MC8T26A  
 (MC6880A)**



**ORDERING INFORMATION**

Device	Alternate	Temperature Range	Package
MC8T26AL	MC6880AL	0 to $+75^{\circ}\text{C}$	Ceramic DIP
MC8T26AP	MC6880AP		Plastic DIP

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## MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	8.0	Vdc
Input Voltage	V <sub>I</sub>	5.5	Vdc
Junction Temperature	T <sub>J</sub>		°C
Ceramic Package		175	
Plastic Package		150	
Operating Ambient Temperature Range	T <sub>A</sub>	0 to +75	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C

## ELECTRICAL CHARACTERISTICS (4.75 V ≤ V<sub>CC</sub> ≤ 5.25 V and 0°C ≤ T<sub>A</sub> ≤ 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State (Receiver Enable Input, V <sub>IL</sub> (RE) = 0.4 V) (Driver Enable Input, V <sub>IL</sub> (DE) = 0.4 V) (Driver Input, V <sub>IL</sub> (D) = 0.4 V) (Bus (Receiver) Input, V <sub>IL</sub> (B) = 0.4 V)	I <sub>IL</sub> (RE) I <sub>IL</sub> (DE) I <sub>IL</sub> (D) I <sub>IL</sub> (B)	–	–	-200	μA
Input Disabled Current – Low Logic State (Driver Input, V <sub>IL</sub> (D) = 0.4 V)	I <sub>IL</sub> (D) DIS	–	–	-25	μA
Input Current-High Logic State (Receiver Enable Input, V <sub>IH</sub> (RE) = 5.25 V) (Driver Enable Input, V <sub>IH</sub> (DE) = 5.25 V) (Driver Input, V <sub>IH</sub> (D) = 5.25 V) (Receiver Input, V <sub>IH</sub> (B) = 5.25 V)	I <sub>IH</sub> (RE) I <sub>IH</sub> (DE) I <sub>IH</sub> (D) I <sub>IH</sub> (B)	–	–	25	μA
Input Voltage – Low Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	V <sub>IL</sub> (RE) V <sub>IL</sub> (DE) V <sub>IL</sub> (D) V <sub>IL</sub> (B)	–	–	0.85	V
Input Voltage – High Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	V <sub>IH</sub> (RE) V <sub>IH</sub> (DE) V <sub>IH</sub> (D) V <sub>IH</sub> (B)	2.0	–	–	V
Output Voltage – Low Logic State (Bus Driver) Output, I <sub>OL</sub> (B) = 48 mA) (Receiver Output, I <sub>OL</sub> (R) = 20 mA)	V <sub>OL</sub> (B) V <sub>OL</sub> (R)	–	–	0.5	V
Output Voltage – High Logic State (Bus (Driver) Output, I <sub>OH</sub> (B) = -10 mA) (Receiver Output, I <sub>OH</sub> (R) = -2.0 mA) (Receiver Output, I <sub>OH</sub> (R) = -100 μA, V <sub>CC</sub> = 5.0 V)	V <sub>OH</sub> (B) V <sub>OH</sub> (R)	2.4 2.4 3.5	3.1 3.1 –	– – –	V
Output Disabled Leakage Current – High Logic State (Bus Driver) Output, V <sub>OH</sub> (B) = 2.4 V) (Receiver Output, V <sub>OH</sub> (R) = 2.4 V)	I <sub>OHL</sub> (B) I <sub>OHL</sub> (R)	–	–	100	μA
Output Disabled Leakage Current – Low Logic State (Bus Output, V <sub>OL</sub> (B) = 0.5 V) (Receiver Output, V <sub>OL</sub> (R) = 0.5 V)	I <sub>OLL</sub> (B) I <sub>OLL</sub> (R)	–	–	-100	μA
Input Clamp Voltage (Driver Enable Input I <sub>ID</sub> (DE) = -12 mA) (Receiver Enable Input I <sub>IC</sub> (RE) = +12 mA) (Driver Input I <sub>IC</sub> (D) = -12 mA)	V <sub>IC</sub> (DE) V <sub>IC</sub> (RE) V <sub>IC</sub> (D)	–	–	-1.0 -1.0 -1.0	V
Output Short Circuit Current, V <sub>CC</sub> = 5.25 V, Note 1 (Bus (Driver) Output) (Receiver Output)	I <sub>OS</sub> (B) I <sub>OS</sub> (R)	-50 -30	–	-150 -75	mA
Power Supply Current (V <sub>CC</sub> = 5.25 V)	I <sub>CC</sub>	–	–	87	mA

Note 1. Only one output may be short-circuited at a time.

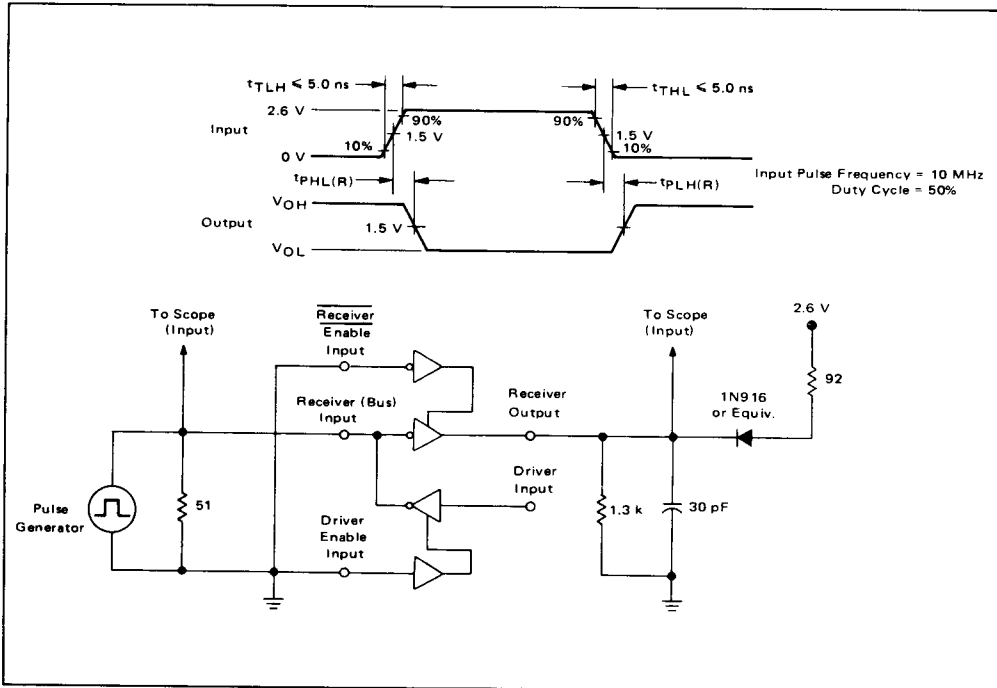
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# MC8T26A

**SWITCHING CHARACTERISTICS** (Unless otherwise noted, specifications apply at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5.0\text{ V}$ )

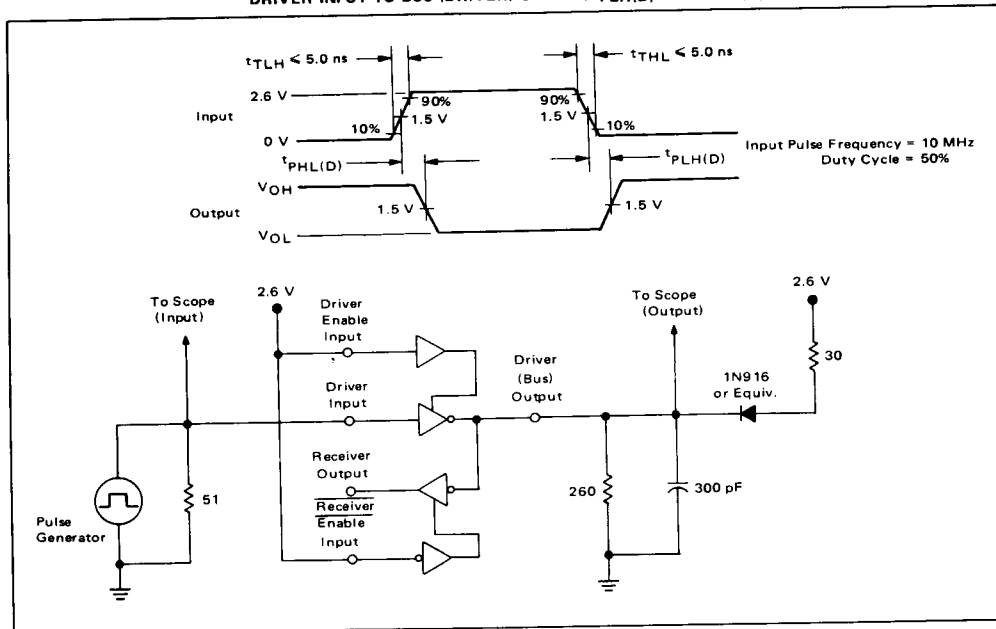
Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH}(R)$	1	—	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL}(R)$	1	—	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH}(D)$	2	—	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL}(D)$	2	—	14	ns
Propagation Delay Time from Receiver Enable Input to High Impedance (Open) Logic State Receiver Output	$t_{PLZ}(RE)$	3	—	15	ns
Propagation Delay Time from Receiver Enable Input to Low Logic Level Receiver Output	$t_{PZL}(RE)$	3	—	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLZ}(DE)$	4	—	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{PZL}(DE)$	4	—	25	ns

**FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT,  $t_{PLH}(R)$  AND  $t_{PHL}(R)$**

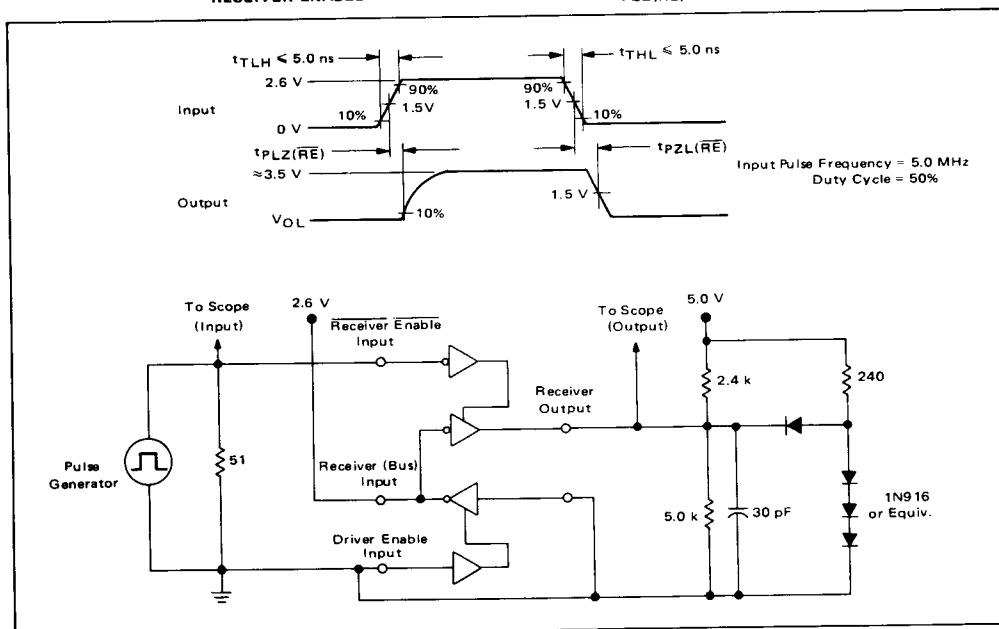


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**FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT,  $t_{PLH(D)}$  AND  $t_{PHL(D)}$**



**FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT,  $t_{PLZ(RE)}$  AND  $t_{PHZ(RE)}$**



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FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT,  $t_{PLZ(DE)}$  AND  $t_{PLZ(IE)}$

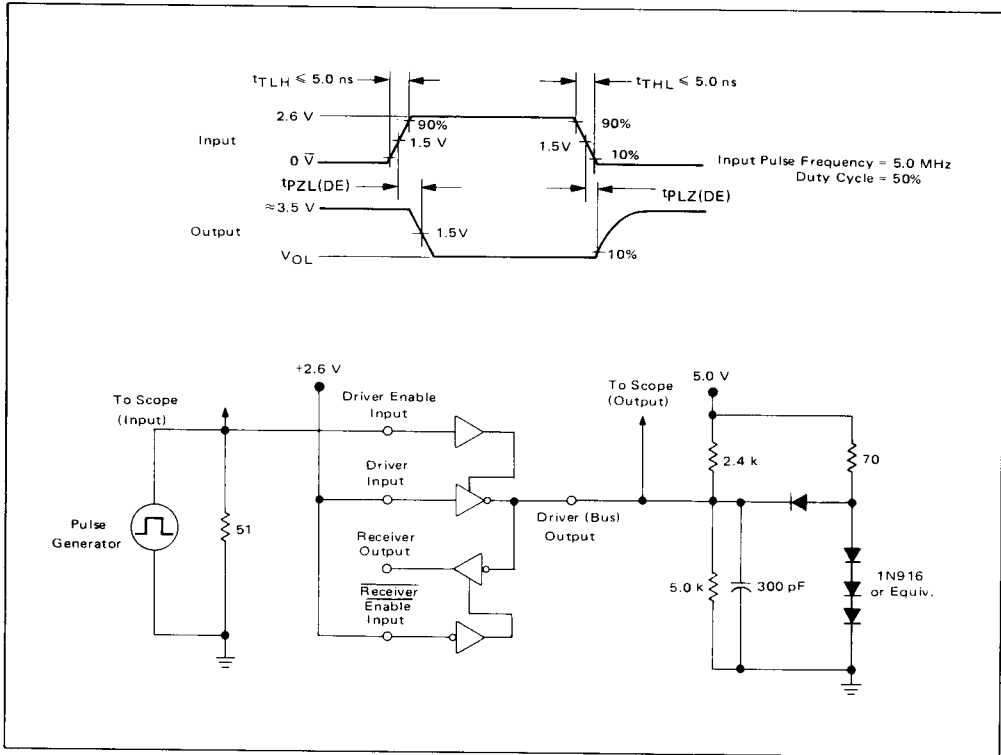
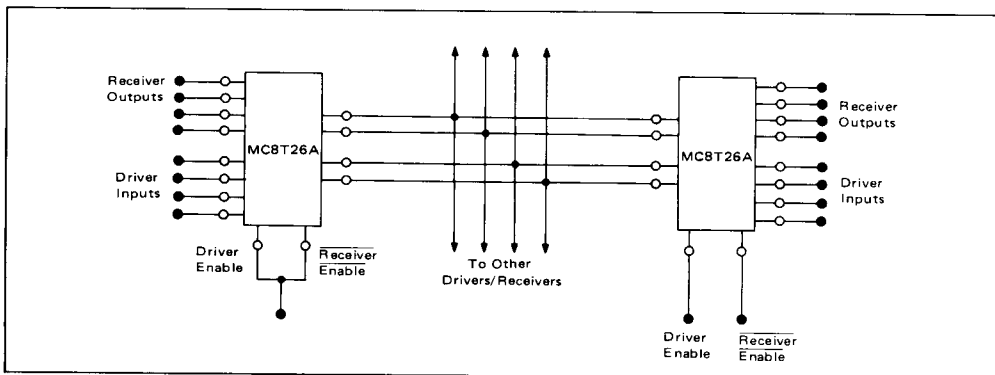


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS



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