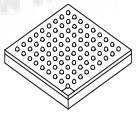
Advance Information
Data Sheet

MC72000/D
Rev. 2.6, 1/2003

MC72000 Integrated Bluetooth™ Radio

MOTOROLA intelligence everywhere™ | digital dna™

MC72000



Package Information
Plastic Package
Case 1398-01
(MAPBGA–100)

Ordering Information

Device	Operating Temperature Range	Package
MC72000	-40° C to 85° C	MAPBGA – 100

Contents

The MC72000 Integrated Bluetooth™ Radio provides a complete, low-power Bluetooth radio solution. The design is based on Motorola's third-generation Bluetooth architecture that has set a high standard for interoperability, complete functionality, and compliance with the Bluetooth specification.

The MC72000 Integrated Bluetooth Radio from Motorola implements the RF and baseband host controller interface (HCI) of the Bluetooth protocol in a small 7 mm x 7 mm BGA package. The MC72000 is the ideal solution for low-power, short-range Bluetooth applications with small size constraints and includes superior performance features like a dedicated Bluetooth audio processor module and on-chip memory. Debug and production test are fully supported through the joint test action group (JTAG) interface.

The RF portion of the radio provides a unique combination of high sensitivity, excellent C/I performance, and low power consumption. These performance parameters are extremely important to maintaining a robust link in high RF interference environments created by devices such as mobile phones, high density Bluetooth networks, 802.11b networks, and microwave ovens.

The MC72000 uses an innovative, highly advanced packaging technique to combine two die—the RF and baseband functions—into a single, cost-effective package. Motorola's optimized two-chip architecture avoids compromises between cost and performance that other one-chip solutions must make. With Motorola's integrated solution, customers get the best of both. Each die is implemented in its optimal process technology to deliver low cost, low power, and small size.

1 MC72000 Features

Radio Transceiver

- Low Current Drain
- Power Down Modes for Power Conservation
- Low IF Receiver with On-Chip Filters
- Fully Integrated Demodulator with ADC
- Direct Launch Transmitter
- Multi-Accumulator, Dual-Port, Fractional-N Synthesizer
- RSSI with ADC
- Bluetooth Class 2 Radio (Class 1 supported using external PA)
- Crystal Independent (12 to 15 MHz) Reference Oscillator or 12 to 26 MHz if supplied externally
- Power Supply Range: 2.5 V to 3.1 V

Baseband Controller

- Bluetooth Specification 1.1 Compliant
  - Point-to-multipoint with 7 slaves
  - All connection types
  - All packet types
  - All power saving modes
  - Master/Slave switch
  - Encryption
  - HCI UART transport layer
- Outstanding Audio Performance
  - Sample rate synchronization between CODECs and Bluetooth clock domains to avoid clicking effects
  - 3 Simultaneous SCO channels supported
  - All Bluetooth encoding/decoding schemes supported (CVSD, A-Law, μ-Law)
  - Very low audio delay to avoid the need for echo cancellation
- Support for 8, 16, 32, and 64 kHz Sample Rate CODECs
- Bluetooth Link Controller
- Bluetooth Audio Signal Processor
- ARM7 Processor Complex
- Peripherals
  - High-speed UART (up to 2 Mbps)
  - High-speed SSI (up to 2 Mbps)
  - High-speed SPI (up to 2 Mbps)
- Embedded Memory
  - SRAM (64 K)
  - ROM (256 K)

- JTAG Test Interface Controller
- 32.768 kHz Oscillator for Low Power Operation
- Operating Voltage: 1.65 V to 1.95 V

2 System Overview

This section provides a brief description of the system for the MC72000.

A system overview is shown in Figure 1

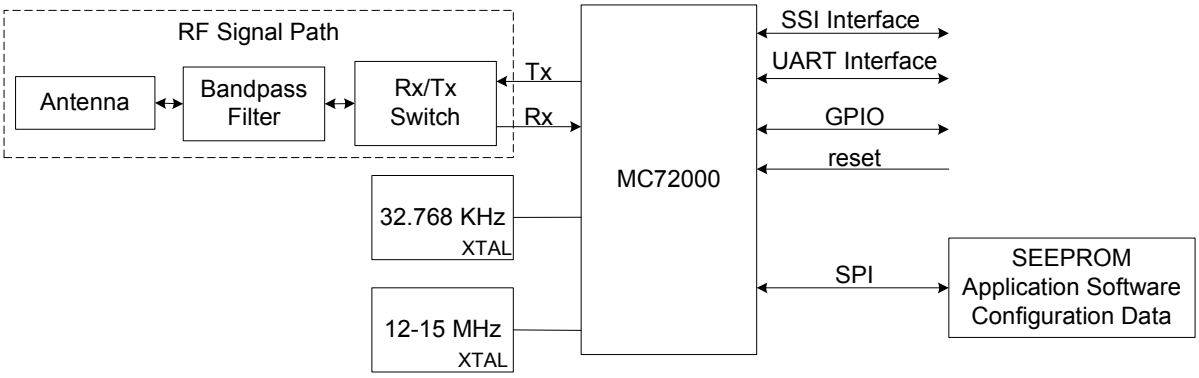


Figure 1. MC72000 Example Application Block Diagram

The main block is the MC72000, which will be described in depth in Section 5, “System Description.”

In addition to the MC72000, there are three other blocks:

- RF signal Path
- Interfaces
- Reference clocks

2.1 RF Signal Path

The switch for the RX and TX, the bandpass filter, and the antenna are all found in the RF signal path.

2.2 Interfaces

There are four bi-directional interfaces and one reset that only the host can initiate.

- The SSI interface is used for audio purposes.
- The UART interface is used for all communication to and from the host (for example, HCI commands).
- The SPI is used for communication with the SEEPROM.
- The GPIO pins are used for different configurations set by the MC72000.

2.3 Clocks/Crystals

The MC72000 has two clocks:

- The reference clock (12-26 MHz) is used when the MC72000 is active. Note that for a crystal connected to the on-chip oscillator, the frequency range is 12-15 MHz as shown in Figure 1.
- The low power clock (32.768 kHz) is also included and may have high initial tolerance.

3 Electrical Characteristics

The absolute maximum ratings given in Table 1 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

WARNING:

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to the high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either VDD or GND), except for JTAG signals. Refer to Section 10.12, "JTAG Interface," for details on how to handle JTAG signals.

3.1 Electrical Characteristics

The following tables provide information on the electrical characteristics of the MC72000.

Table 1. Absolute Maximum Ratings

Characteristics	Symbol	Value	Unit
Power Supply Voltage, RF		(GND – 0.3) to 3.2	VDC
Power Supply Voltage, BB		(GND – 0.3) to 2.0	VDC
Power Supply Voltage, IO		(GND – 0.3) to 3.6	VDC
Junction Temperature	T_J	150	ºC
Storage Temperature Range	T_{stg}	-55 to 150	ºC

Table 2. ESD Protection Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Human Body Model (HBM) All pins, except RFIN, PAO+, and PAO- RFIN, PAO+, and PAO-	 V_{HBM} V_{RFHBM}	 2000 100	 - -	 - -	V
Machine Model (MM) All pins, except RFIN, PAO+, and PAO- RFIN, PAO+, and PAO-	 V_{MM} V_{RFMM}	 200 50	 - -	 - -	V

Table 3. Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage, RF	VCC_{RF}	2.5	2.7	3.1	VDC
Power Supply Voltage, BB	VDD_{BB}	1.65	1.8	1.95	VDC
Power Supply Voltage, IO	VDD_{IO}	1.8	-	3.3	VDC
Input Frequency	f_{in}	2.4	-	2.5	GHz
Ambient Temperature Range	T_A	-40	-	85	ºC
Ref Osc Frequency Range (only integral multiples of 20 kHz may be used) With Crystal External Source	f_{ref}	 12 12	 13 -	 15 26	MHz
Low Power Osc Frequency Range With Crystal External Source	f_{lp}	 32.768 32.768			kHz

Table 4. Digital DC Electrical Specifications

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A= 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Current High (V_{IN} = VDD) BB Digital Pins IO Digital Pins	I_{IH}	 - -	 - -	 TBD TBD	µA
Input Current Low (V_{IN} = GND) BB Digital Pins IO Digital Pins	I_{IL}	 TBD TBD	 - -	 - -	µA
Output Current High-Impedance State	I_{OZ}	TBD	-	TBD	µA
Output Short-Circuit Current (V_{OUT} = VDD/VCC) BB Digital Pins IO Digital Pins RF Digital Pins (V_{OUT} = GND) BB Digital Pins IO Digital Pins RF Digital Pins	I_{OS}	 - - - - - -	 TBD TBD TBD TBD TBD TBD	 - - - - - -	mA
Input Voltage High BB Digital Pins IO Digital Pins	V_{IH}	 0.7 x VDD_BB 0.7 x VDD_IO	 - -	 VDD_BB VDD_IO	V
Input Voltage Low BB Digital Pins IO Digital Pins	V_{IL}	 -0.3 -0.3	 - -	 0.3 x VDD_BB 0.3 x VDD_IO	V

Table 4. Digital DC Electrical Specifications (Continued)

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A= 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage High BB Digital Pins (I_{OH} = -3mA) IO Digital Pins (I_{OH} = -3mA) RF Digital Pins (I_{OH} = -100µA)	V_{OH}	 0.8 x VDD_BB 0.8 x VDD_IO 0.8 x VCC_RF	 - - -	 VDD_BB VDD_IO VCC_RF	V
Output Voltage Low BB Digital Pins (I_{OL} = 3mA) IO Digital Pins (I_{OL} = 3mA) RF Digital Pins (I_{OL} = 100µA)	V_{OL}	 0 0 0	 - - -	 0.2 x VDD_BB 0.2 x VDD_IO 0.2 x VDD_RF	V
Internal Pull-up Device Current IO Digital pins at V_{ILMAX} IO Digital pins at V_{IHMIN} MODE1, TTS, TMS, TDI at V_{ILMAX} MODE1, TTS, TMS, TDI at V_{IHMIN}	 I_{IOPUL} I_{IOPUH} I_{BBPUL} I_{BBPUH}	 - -5 - -2	 - - - -	 -50 - -30 -	µA
Internal Pull-down Device Current RESET_BB, TCK, TRST_B at V_{ILMAX} RESET_BB, TCK, TRST_B at V_{IHMIN}	 I_{BBPDL} I_{BBPDH}	 - 2	 - -	 20 -	µA
Input Capacitance BB Digital Pins IO Digital Pins	 C_{BBIN} C_{IOIN}	 - -	 5 5	 - -	pF

Table 5. EPA DAC Electrical Specifications

Note: (VCC_RF = 3.1 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 94 except R11/7 = 1, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage EPADAC, I_{load} = ± 100 µA PADAC = 000000 PADAC = 100000 PADAC = 111111	V_{out}	 - - -	 0.02 1.60 3.08	 - - -	V
Resolution	RESOL	-	6	-	Bits
Linearity	INL/DNL	-	± 1.0	-	LSB
Average Supply Current (1-slot packet)	I_{CCDAC}	-	197	-	µA

Table 6. Power Consumption Characteristics

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Typical Average	Max Peak	Unit
Total Power Supply Current				mA
SCO link, HV1	I_{TOTHV1}	TBD	TBD	
SCO link, HV2	I_{TOTHV2}	TBD	TBD	
SCO link, HV3	I_{TOTHV3}	TBD	TBD	
ACL link, 1-slot symmetric	I_{TOTA1}	TBD	TBD	
ACL link, 3-slot symmetric	I_{TOTA3}	TBD	TBD	
ACL link, 5-slot symmetric	I_{TOTA5}	TBD	TBD	
Standby Mode (No RF activity)	$I_{TOTSTBY}$	TBD	TBD	
Sniff Mode, 0.5 s	$I_{TOTS0.5}$	TBD	TBD	
Sniff Mode, 1.0 s	$I_{TOTS1.0}$	TBD	TBD	
Sniff Mode, 2.0 s	$I_{TOTS2.0}$	TBD	TBD	
Hold Mode	$I_{TOTHOLD}$	TBD	TBD	
Inquiry Scan Mode, 1.28 s interval	I_{TOTIS}	TBD	TBD	
Page Scan Mode, 1.28 s interval	I_{TOTPS}	TBD	TBD	
Inquiry and Page Scan Mode, 1.28 s interval	I_{TOTIPS}	TBD	TBD	
RF Power Supply Current				
Transmit, 1 slot ACL	$I_{CCRFtx1}$	22	26	mA
Transmit, 3 slot ACL	$I_{CCRFtx3}$	25	26	
Transmit, 5 slot ACL	$I_{CCRFtx5}$	26	26	
Transmit, HV1	$I_{CCRFtxHV1}$	22	28	
Transmit, HV2	$I_{CCRFtxHV2}$	TBD	TBD	
Transmit, HV3	$I_{CCRFtxHV3}$	TBD	TBD	
Transmit, Continuous	$I_{CCRFtxc}$	26	26	
Receive, 1 slot ACL	$I_{CCRFrx1}$	33	38	
Receive, 3 slot ACL	$I_{CCRFrx3}$	36	38	
Receive, 5 slot ACL	$I_{CCRFrx5}$	37	38	
Receive, HV1	$I_{CCRFrxHV1}$	32	40	
Receive, HV2	$I_{CCRFrxHV2}$	TBD	TBD	
Receive, HV3	$I_{CCRFrxHV3}$	TBD	TBD	
Receive, Continuous	$I_{CCRFrxc}$	38	38	
Standby Mode (No RF activity)	$I_{CCRFstby}$	TBD	TBD	
Sniff Mode, 0.5s	$I_{CCRFs0.5}$	TBD	TBD	
Sniff Mode, 1.0s	$I_{CCRFs1.0}$	TBD	TBD	
Sniff Mode, 2.0s	$I_{CCRFs2.0}$	TBD	TBD	
Hold Mode	$I_{CCRFhold}$	TBD	TBD	
Inquiry Scan Mode, 1.28s interval	I_{CCRFis}	TBD	TBD	
Page Scan Mode, 1.28s interval	I_{CCRFps}	TBD	TBD	
Inquiry and Page Scan Mode, 1.28s interval	$I_{CCRFips}$	TBD	TBD	

Table 6. Power Consumption Characteristics (Continued)

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Typical Average	Max Peak	Unit
BB Power Supply Current				mA
Transmit, 1 slot ACL	$I_{CCBBtx1}$	27	38	
Transmit, 3 slot ACL	$I_{CCBBtx3}$	26	38	
Transmit, 5 slot ACL	$I_{CCBBtx5}$	25	38	
Transmit, HV1	$I_{CCBBtxHV1}$	27	41	
Transmit, HV2	$I_{CCBBtxHV2}$	TBD	TBD	
Transmit, HV3	$I_{CCBBtxHV3}$	TBD	TBD	
Transmit, Continuous	$I_{CCBBtxc}$	25	38	
Receive, 1 slot ACL	$I_{CCBBrx1}$	27	38	
Receive, 3 slot ACL	$I_{CCBBrx3}$	25	38	
Receive, 5 slot ACL	$I_{CCBBrx5}$	26	38	
Receive, HV1	$I_{CCBBrxHV1}$	28	42	
Receive, HV2	$I_{CCBBrxHV2}$	TBD	TBD	
Receive, HV3	$I_{CCBBrxHV3}$	TBD	TBD	
Receive, Continuous	$I_{CCBBrxc}$	26	38	
Standby Mode (No RF activity)	$I_{CCBBstby}$	TBD	TBD	
Sniff Mode, 0.5s	$I_{CCBBs0.5}$	TBD	TBD	
Sniff Mode, 1.0s	$I_{CCBBs1.0}$	TBD	TBD	
Sniff Mode, 2.0s	$I_{CCBBs2.0}$	TBD	TBD	
Hold Mode	$I_{CCBBhold}$	TBD	TBD	
Inquiry Scan Mode, 1.28s interval	I_{CCBBis}	TBD	TBD	
Page Scan Mode, 1.28s interval	I_{CCBBps}	TBD	TBD	
Inquiry and Page Scan Mode, 1.28s interval	$I_{CCBBips}$	TBD	TBD	
IO Power Supply Current				mA
Transmit, 1 slot ACL	$I_{CCIOtx1}$	0.6	0.6	
Transmit, 3 slot ACL	$I_{CCIOtx3}$	0.6	0.6	
Transmit, 5 slot ACL	$I_{CCIOtx5}$	0.6	0.6	
Transmit, HV1	$I_{CCIOtxHV1}$	0.4	0.4	
Transmit, HV2	$I_{CCIOtxHV2}$	TBD	TBD	
Transmit, HV3	$I_{CCIOtxHV3}$	TBD	TBD	
Transmit, Continuous	$I_{CCIOtxc}$	0.6	0.6	
Receive, 1 slot ACL	$I_{CCIOrx1}$	0.6	0.6	
Receive, 3 slot ACL	$I_{CCIOrx3}$	0.6	0.6	
Receive, 5 slot ACL	$I_{CCIOrx5}$	0.6	0.6	
Receive, HV1	$I_{CCIOrxHV1}$	0.4	0.4	
Receive, HV2	$I_{CCIOrxHV2}$	TBD	TBD	
Receive, HV3	$I_{CCIOrxHV3}$	TBD	TBD	
Receive, Continuous	$I_{CCIOrxc}$	0.6	0.6	
Standby Mode (No RF activity)	$I_{CCIOstby}$	TBD	TBD	
Sniff Mode, 0.5s	$I_{CCIOs0.5}$	TBD	TBD	
Sniff Mode, 1.0s	$I_{CCIOs1.0}$	TBD	TBD	
Sniff Mode, 2.0s	$I_{CCIOs2.0}$	TBD	TBD	
Hold Mode	$I_{CCIOhold}$	TBD	TBD	
Inquiry Scan Mode, 1.28s interval	I_{CCIOis}	TBD	TBD	
Page Scan Mode, 1.28s interval	I_{CCIOps}	TBD	TBD	
Inquiry and Page Scan Mode, 1.28s interval	$I_{CCIOips}$	TBD	TBD	

Table 6 shows the overall current consumed by the MC72000 in many well-known scenarios as well as detailed current in real-time specific modes.

The first row in Table 6 shows the maximum peak and typical average total current consumed by the device in most scenarios used by PDAs, cell phone design, and other audio-capable devices such as headsets. The current specified in this row is the total current consumed through the three power groups of the MC72000 (i.e., the voltage relationship between the three different supply voltages in these three groups are ignored). Power dissipated by the MC72000 may, therefore, be different than the direct power consumption calculated on the total current consumption.

In order to find current values for special scenarios not covered by the typical values of total current consumption, the current consumed in each of the three power groups are also defined in a variety of usages. Each value represents the current consumed in between a repeatedly symmetrical timeframe, for example, the BB power supply current for transmitting one-slot ACL packets is defined as the time from start of TX burst to the start of RX burst, as the same current consumption is repeated again in the next TX slot. This also applies to all currents defined for receiving packets regardless of packet type. See example below in Figure 2. The repeatedly symmetrical pattern definition for the listed scenarios are shown in Table 7.

Table 7. Real-time Current Consumption Definitions

Scenario	Defined as
TX and RX, ACL, HV	From TX burst to RX burst or vice versa
TX and RX Continuous	Absolute value as there is no repeated pattern
Standby Mode	Absolute value as there is no repeated pattern
Sniff Mode	One sniff cycle with defined length in seconds
Hold Mode	Total hold time from start to finish
Inquiry and/or Page Scan Mode	One page/inquiry scan interval with defined length in seconds

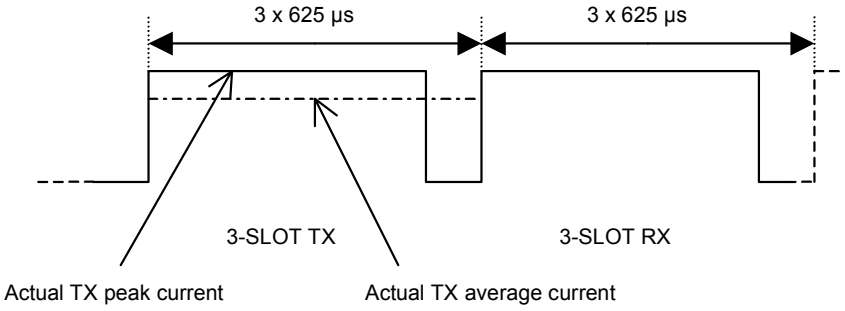


Figure 2. Power Consumption Characteristics

Table 8. Receiver AC Electrical Specifications

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, unless otherwise noted, Desired RF_{in} = 2.441 GHz @ f_{dev} = 157.5 kHz, Interferer f_{dev} = 160 kHz, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Modulating payload data for desired signal = PRBS9, Modulating data for interfering signal = PRBS15 continuously modulated, Measured BER = 0.1%, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. Measurements made from LNA_{in} to Recovered Data out. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	BT Spec	Unit
Receiver Sensitivity	$SENS_{min}$					dBm
T_A = 25º C		-	-85	-		
T_A = -40 to 85º C		-	-80	-75	≤ -70	
Maximum Usable Signal Level T_A = -40 to 85º C	$SENS_{max}$	-20	> 0	-	≥ -20	dBm
Co-Channel Interference @ -60 dBm	C/I co	-	9	11	≤ 11	dB
Adjacent Interference						dB
Adjacent (±1 MHz) Interference @ -60 dBm	C/I 1MHz	-	-7	-3	≤ 0	
Adjacent (±2 MHz) Interference @ -60 dBm	C/I 2MHz	-	-33	-30	≤ -30	
Adjacent (≥3 MHz) Interference @ -67 dBm	C/I =3MHz	-	-41	-40	≤ -40	
Image Frequency Interference @ -67 dBm	C/I Image	-	-16	-12	≤ -9	dB
Adjacent Interference to In-Band Image Frequency @ -67 dBm	C/I Image ±1	-	-32	-28	≤ -20	dB
Spurious Response Frequencies		-	3	5	5	
Intermodulation Performance[1]		-39	-33	-	≥ -39	dBm
Receiver Spurious Emissions -40 to 85º C						dBm/ 100kHz
Bluetooth						
30 MHz to 1.0 GHz		-	-66	-57	≤ -57	
1.0 GHz to 12.75 GHz		-	-57	-47	≤ -47	
GSM/DCS and UMTS downlink						
2110 MHz - 2170 MHz (WCDMA-FDD)[2]		-	-186	-180		dBm/Hz
2010 MHz - 2025 MHz (WCDMA-TDD)[2]		-	-184	-180		
1900 MHz - 1920 MHz (WCDMA-TDD)[2]		-	-184	-180		
869 MHz - 894 MHz (GSM 850)[3]		-	-177	-163		
921 MHz - 960 MHz (GSM 900)[3]		-	-177	-163		
1805 MHz - 1880 MHz (DCS1800)[3]		-	-177	-170		
1930 MHz - 1990 MHz (PCS1900)[3]		-	-174	-168		

Table 8. Receiver AC Electrical Specifications (Continued)

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, unless otherwise noted, Desired RF_{in} = 2.441 GHz @ f_{dev} = 157.5 kHz, Interferer f_{dev} = 160 kHz, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Modulating payload data for desired signal = PRBS9, Modulating data for interfering signal = PRBS15 continuously modulated, Measured BER = 0.1%, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. Measurements made from LNA_{in} to Recovered Data out. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	BT Spec	Unit
Receiver Blocking Performance[4] (See Figure 11)						dBm
Bluetooth						
30 MHz to 1.999 GHz		TBD	-9	-	≥ -10	
2.0 GHz to 2.399 GHz		TBD	-16	-	≥ -27	
2.498 GHz to 2.999 GHz		TBD	TBD	-	≥ -27	
3.0 GHz to 12.75 GHz		TBD	TBD	-	≥ -10	
GSM/DCS and UMTS uplink[5]						
1920 MHz - 1980 MHz (WCDMA-FDD)		-21	-15	-		
2010 MHz - 2025 MHz (WCDMA-TDD)		-20	-16	-		
1900 MHz - 1920 MHz (WCDMA-TDD)		-23	-15	-		
824 MHz - 849 MHz (GSM 850)		-18	-10	-		
876 MHz - 915 MHz (GSM 900)		-11	-5	-		
1710 MHz - 1785 MHz (DCS1800)		-16	-11	-		
1850 MHz - 1910 MHz (PCS1900)		-23	-15	-		
RSSI Conversion Value, (R4/6 and R9/8 = 1) RF level at LNA input to maintain conversion value of:	RSSI					dBm
1000 (binary)		-60	-56	-52		
1111		-	-70	-66		
RSSI Resolution, (R4/6 and R9/8 = 1)	$RSSI_{res}$	-	1.8	-		dB/bit
RSSI Dynamic Range		20	-	-		dB
RSSI Average Supply Current, (R4/6 and R9/8 = 1)		-	40	-		µA

1. Measured at f2 – f1 = 5.0 MHz in accordance with Bluetooth specification.
2. Equivalent noise floor to 5 MHz bandwidth
3. Equivalent noise floor to 200 kHz bandwidth
4. As allowed by the Bluetooth specification, up to five exceptions may be taken for spurious response.
5. Measured according to Bluetooth Specification, but using a correct modulated and bursting GSM/DCS/ UMTS interfering signal, based on one timeslot.

Table 9. Transmitter AC Electrical Specifications

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = -40 to 85° C, unless otherwise noted, Modulation = GFSK, BT = 0.5, Bit Rate = 1.0 Mbps, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. Measurements made at PAout. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Bluetooth Specification	Unit
RF Transmit Output Power T_A = 25º C T_A = 85º C T_A = -40º C	P_{out}	 -3.5 -3.5 -3.5	 1.5 -1.0 2.5	 4.0 4.0 4.0	- 6 to 4	dBm
-20 dBc Occupied Bandwidth	OccBW	-	930	1000	≤ 1000	kHz
In-Band Spurious Emissions Adjacent Channel ±2 MHz Offset Adjacent Channel ±3 MHz Offset Adjacent Channel >3 MHz Offset	 Inb2 Inb3 Inbg3	 - - -	 -53 -63 -65	 -20 -40 -40	 ≤ -20 ≤ -40 ≤ -40	dBm/ 100kHz
In-Band Spurious Emission Exceptions	Inbex	-	0	3	≤ 3	
Out of Band Spurious Emissions Bluetooth 30 MHz to 1.0 GHz 1.0 GHz to 12.75 GHz (2nd Harmonic) 1.8 GHz to 1.9 GHz 5.15 GHz to 5.3 GHz GSM/DCS and UMTS downlink 2110 MHz - 2170 MHz (WCDMA-FDD)[1] 2010 MHz - 2025 MHz (WCDMA-TDD)[1] 1900 MHz - 1920 MHz (WCDMA-TDD)[1] 869 MHz - 894 MHz (GSM 850)[2] 921 MHz - 960 MHz (GSM 900)[2] 1805 MHz - 1880 MHz (DCS1800)[2] 1930 MHz - 1990 MHz (PCS1900)[2]	 Outb1 Outb2 Outb3 Outb4	 - - - - - - - - - - - -	 -66 -17 -76 -77 -177 -190 -190 -175 -175 -175 -175	 -36 -5 -47 -47 -168 -178 -182 -153 -156 -165 -167	 ≤ -36 ≤ -30 ≤ -47 ≤ -47	dBm/ 100kHz dBm/Hz
Average Frequency Deviation	Dev	140	160	175	140 to 175	kHz
Minimum Frequency Deviation	DevMin	115	152	-	≥ 115	kHz
High vs. Low Frequency Modulation Percentage	ModIn	80	95	-	≥ 80	%
Initial Frequency Accuracy	InitFA	-75	± 5	75	± 75	kHz
Transmitter Center Frequency Drift One-slot packet Three-slot packet Five-slot packet	 d1 d3 d5	 -25 -40 -40	 ± 8 ± 12 ± 12	 25 40 40	 ± 25 ± 40 ± 40	kHz
Maximum Drift Rate	Dmax	-20	± 8	20	± 20	kHz/ 50µs
PA Output Impedance 25° C	S22	See Table 22				dB

1. Equivalent noise floor to 5 MHz bandwidth
2. Equivalent noise floor to 200 kHz bandwidth

Table 10. MC72000 Receive Characteristics

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = -40 to 85° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. Interfering access code at the minimum Hamming distance of 14 according to Bluetooth specifications. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
False Detection Rate In Presence of Noise In Presence of Interfering Access Code @ Actual Sensitivity @ Actual Sensitivity + 10 dB		 - - -	 0 0 0	 - - -	%
Missed Detection Rate @ Actual Sensitivity @ Actual Sensitivity + 10 dB @ Actual Sensitivity – 16 dB		 - - -	 0 0 100	 - - -	%

Table 11. Reference Oscillator Electrical Specifications

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
Crystal Frequency Range	$f_{RefXTAL}$	12	-	15	MHz
External Drive Frequency Range	$f_{RefXTAL}$	12	-	26	MHz
Oscillator Drive Level External Reference Crystal Reference		 0.2 -	 - 0.8	 1.0 -	V_{pp}
Crystal Load Capacitance (Resonant Parallel)		-	13	-	pF
Maximum Crystal Equivalent Series Resistance (ESR)		-	-	100	Ω
Typical Crystal Adjustment Range		See Figure 26			
Recommended Crystal Tolerance over Temperature (-40 to +85° C)		-	±10	-	ppm
Electronic Parallel Trim Capacitance Range	C_{PT}	-	0 to 9.3	-	pF
Electronic Parallel Trim Capacitance Resolution		-	0.3	-	pF
Oscillator Bias Current (R11/0) = 0, (R11/4) = 0 or 1 (R11/0) = 1, (R11/4) = 0 (R11/0) = 1, (R11/4) = 1		 - - -	 0 50 200	 - - -	µA

Table 11. Reference Oscillator Electrical Specifications (Continued)

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Impedance at XBASE (Reference Frequency = 12 to 26 MHz, R11/0 = 0 or 1) Parallel Capacitance	C_P	-	1.0 + Parallel Trim Capaci-tance	-	pF
Parallel Resistance	R_P	-	20	-	kΩ
Input Phase Noise at XBASE (Reference Frequency = 12 to 26 MHz, R11/0 = 0 or 1) 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz		 - - - - -	 - - - - -	 -70 -90 -105 -110 -130	dBc/ Hz
Duty Cycle for External Reference		TBD	50	TBD	%
Input Bias Voltage (XBASE)		-	1.2	-	V
Start-up Time (using Crystal)	T_{WAIT}	-	7.5	-	Ms

Table 12. Low Power Oscillator Electrical Specifications

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 5, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
Crystal Frequency	fLPXTAL		32.768		kHz
External Drive Frequency Range	fLPXTAL		32.768		kHz
Oscillator Drive Level (DC or AC coupled) External Reference Crystal Reference		 TBD -	 - TBD	 VDD_BB -	Vpp
Crystal Load Capacitance (Resonant Parallel)		-	TBD	-	pF
XTAL Transconductance		-	15	-	mA/V
XTAL Output Resistance (XTAL_BB)	g_{mLP}	-	250	-	kΩ
Maximum Crystal Equivalent Series Resistance (ESR)	R_{oLP}	-	-	TBD	
Recommended Crystal Tolerance over Temperature (-40 to +85°C)		-	± 200	-	ppm
Oscillator Bias Current		-	TBD	-	µA

Table 12. Low Power Oscillator Electrical Specifications (Continued)

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 5, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Impedance at EXTAL_BB Parallel Capacitance Parallel Resistance			 TBD TBD		
Duty Cycle for External Reference		TBD	50	TBD	%
Start-up Time (using Crystal)	T_{LPWAIT}	5	-	700	ms

Table 13. Data Clock PLL Electrical Specifications

Note: (VCC_RF = 2.7 VDC, VDD_BB = 1.8 VDC, VDD_IO = 3 VDC, T_A = 25° C, Reference Crystal = 13 MHz, Register bit settings according to Figure 94, unless otherwise noted. See Figure 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
Internal Reference Frequency		-	20	4000	kHz
Data Clock Output Frequency		-	24	-	MHz
R Counter (R6/9-0) (Base 10)		3	650	1023	
N Counter (R7/10-0) (Base 10)		3	1200	2047	
Loop Filter Bandwidth		-	1	200	kHz
Phase Detector Gain Constant	K_{pd}	-	15.9	-	µA/rad
VCO Gain Constant	K_{VCO}	-	15	-	MHz/V
Start-up Time External Reference Crystal Reference		 - -	 1.0 7.5	 - -	Ms

The following figure shows a typical test circuit schematic.

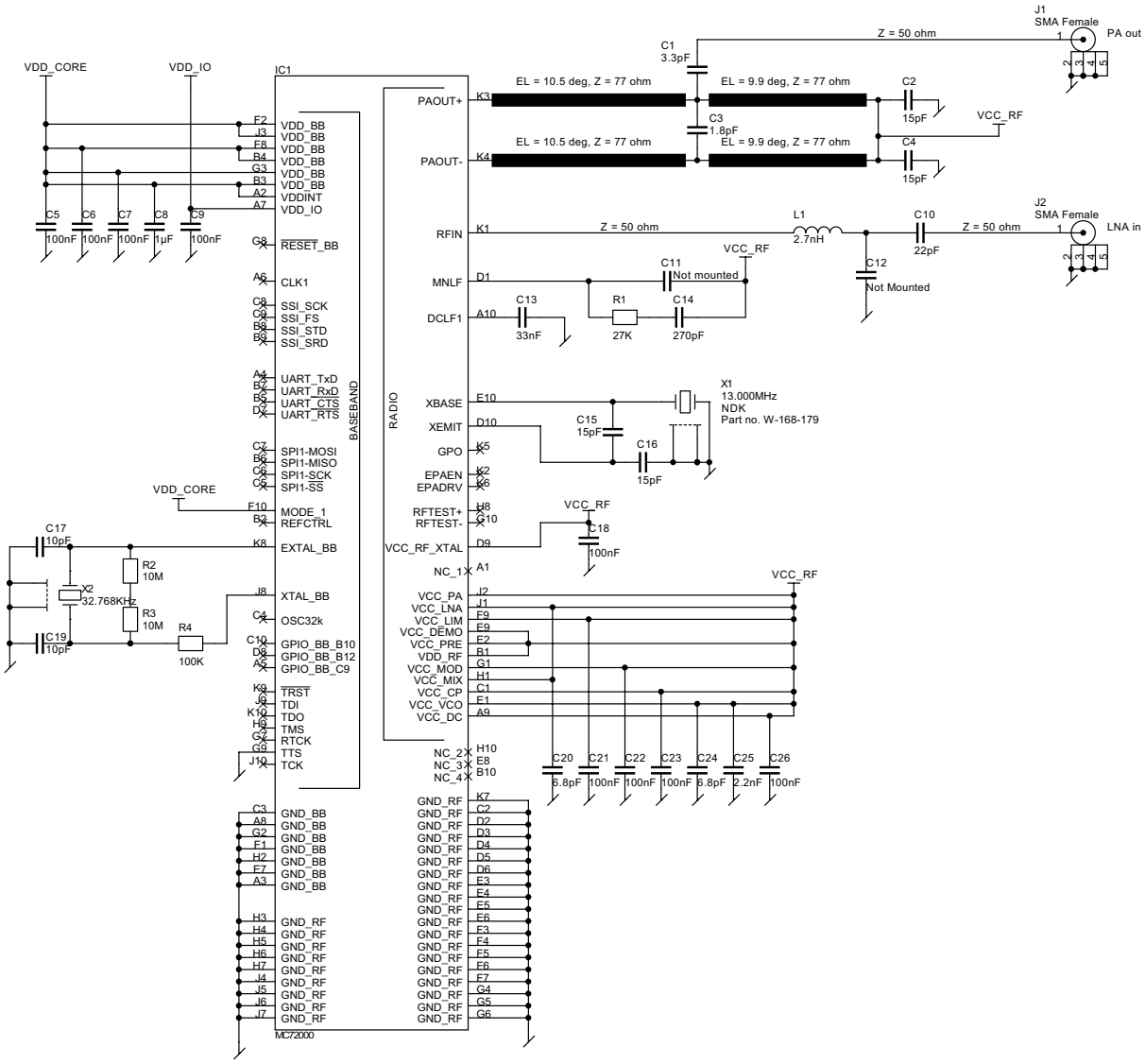


Figure 3. Typical Test Circuit Schematic

4 Package Pinout

NOTE:

Low power and small PCB footprints are critical for certain applications. Therefore, input pins not used must be pulled high using internal pull-ups to avoid floating nodes and the need for external pull-up resistors. Unused pins may also be tied to an external appropriate logic voltage level (for example, either VDD or GND). Weak pull-ups are available internally on all IO and BB pins (100k ohms typical case), pull-downs are available on RESET_BB, TCK, TRST_B pins. Internal level-shifters are used to accommodate the difference between BB and IO voltages. This provides glueless interface to peripherals.

4.1 Pin Assignment Listing

The following table (Table 9) shows the pin assignment listing for the MC72000 IC. The pins are organized into functional groups.

- The Pin Name and Functionality columns show the actual name and a brief description of each pin, with respect to the ball assignment in the column Ball #.
- The Power Group column lists the Supply Power Group assignment.
- The Pin Type column shows the type of internal circuitry to the chip.
- The Reset State column lists the pin input/output direction at chip RESET_BB.
- The Alternate Function column lists each of the GPIO port alternate input and output selections available. Some selections are test- or development-mode specific.

Table 14. Pin Names and Functions

Ball #	Pin Name	Functionality	Power Group	Pin Type	Reset State	Alternate Function
A1	N/C	Not connected	-	-	-	-
A2	VDD_BB	Baseband interface supply	CORE	Power line	-	-
A3	GND_BB	Baseband ground	CORE	Power line	-	-
A4	UART_TXD	UART - Transmit data	I/O	Digital tri-state output	Z/H	GPIO_C0 CSPI0_REQ
A5	GPIO_BB_C9	General purpose I/O	I/O	Digital I/O	Z/H	XACK
A6	CLK1	Programmable clock output	I/O	Digital I/O	O/L	GPIO_C8 TIM_0_O
A7	VDD_IO	I/O port B and C supply	I/O	Power line	-	-
A8	GND_IO	I/O ground	I/O	Power line	-	-
A9	VCC_DC	RF Data clock supply	RF	Power line	-	-
A10	DCLF1	RF Data clock loop filter	RF	Analog output	-	-

Table 14. Pin Names and Functions (Continued)

B1	VDD_RF	RF logic supply	RF	Power line	-	-
B2	REFCTRL	RF reference clock control	CORE	Digital output	O/L	-
B3	VDD_BB	Baseband miscellaneous supply	CORE	Power line	-	-
B4	VDD_BB	Baseband core supply	CORE	Power line	-	-
B5	UART_CTS	UART - Clear to send	I/O	Digital tri-state output	Z/H	GPIO_C1 CSPI1_REQ
B6	SPI1_MISO	SPI1 - Master in/Slave out	I/O	Digital I/O	O/L	GPIO_C6 ABORT
B7	UART_RXD	UART - Receive data	I/O	Digital I/O	Z/H	GPIO_C2 TIM_0_I
B8	SSI_STD	SSI - Serial transmit data	I/O	Digital I/O	Z/H	GPIO_B2 BT_TP2
B9	SSI_SRD	SSI - Serial receive data	I/O	Digital I/O	Z/H	GPIO_B5 BT_TP5
B10	N/C	Not connected	-	-	-	-
C1	VCC_CP	RF Frac-N charge pump supply	RF	Power line	-	-
C2	GND_RF	RF front end ground	RF	Power line	-	-
C3	GND_BB	Baseband miscellaneous ground	CORE	Power line	-	-
C4	OSC32K	Buffered low power 32.768 kHz clock	I/O	Digital I/O	O/L	GPIO_C10 TIM_1_O
C5	SPI1_SS	SPI1 - Slave select	I/O	Digital output	O/H	GPIO_C4 SYSCLK
C6	SPI1_SCK	SPI1 - Serial clock	I/O	Digital output	O/H	GPIO_C5 SH_STROBE
C7	SPI1_MOSI	SPI1 - Master out/Slave in	I/O	Digital I/O	Z/H	GPIO_C7 REFCLK
C8	SSI_SCK	SSI - Serial clock	I/O	Digital I/O	Z/H	GPIO_B0/ GPIO_B3 BT_TP0/ BT_TP3
C9	SSI_FS	SSI - Frame sync	I/O	Digital I/O	Z/H	GPIO_B1/ GPIO_B4 BT_TP1/ BT_TP4
C10	GPIO_BB_B10	General purpose I/O	I/O	Digital I/O	Z/H	UART_TXD
D1	MNLF	RF Main Frac-N loop filter	RF	Analog output	-	-

Table 14. Pin Names and Functions (Continued)

D2	GND_RF	RF front end ground	RF	Power line	-	-
D3	GND_RF	RF front end ground	RF	Power line	-	-
D4	GND_RF	RF front end ground	RF	Power line	-	-
D5	GND_RF	RF front end ground	RF	Power line	-	-
D6	GND_RF	RF front end ground	RF	Power line	-	-
D7	UART_RTS	UART - Request to send	I/O	Digital I/O	Z/H	GPIO_C3 TIM_1_I
D8	GPIO_BB_B 12	General purpose I/O	I/O	Digital I/O	Z/H	UART_RXD
D9	VCC_RF_XT AL	RF crystal oscillator supply	RF	Power line	-	-
D10	XEMIT	RF crystal oscillator emitter	RF	Analog output	-	-
E1	VCC_VCO	RF VCO supply	RF	Power line	-	-
E2	VCC_PRE	RF Frac-N prescaler supply	RF	Power line	-	-
E3	GND_RF	RF front end ground	RF	Power line	-	-
E4	GND_RF	RF front end ground	RF	Power line	-	-
E5	GND_RF	RF front end ground	RF	Power line	-	-
E6	GND_RF	RF front end ground	RF	Power line	-	-
E7	GND_BB	Baseband ground	CORE	Power line	-	-
E8	N/C	Not connected	-	-	-	-
E9	VCC_DEMO	RF demodulator supply	RF	Power line	-	-
E10	XBASE	Crystal oscillator base	RF	Analog input	-	-
F1	GND_BB	Baseband ground	CORE	Power line		
F2	VDD_BB	Baseband core supply	CORE	Power line	-	-
F3	GND_RF	RF front end ground	RF	Power line	-	-
F4	GND_RF	RF front end ground	RF	Power line	-	-
F5	GND_RF	RF front end ground	RF	Power line	-	-
F6	GND_RF	RF front end ground	RF	Power line	-	-
F7	GND_RF	RF front end ground	RF	Power line	-	-
F8	VDD_BB	Baseband core supply	CORE	Power line	-	-
F9	VCC_LIM	RF limiter supply	RF	Power line	-	-
F10	MODE1	Baseband boot mode select 1	CORE	Digital input	I	-

Table 14. Pin Names and Functions (Continued)

G1	VCC_MOD	RF modulation DAC supply	RF	Power line	-	-
G2	GND_BB	Baseband ground	CORE	Power line	-	-
G3	VDD_BB	Baseband EIM supply	CORE	Power line	-	-
G4	GND_RF	RF front end ground	RF	Power line	-	-
G5	GND_RF	RF front end ground	RF	Power line	-	-
G6	GND_RF	RF front end ground	RF	Power line	-	-
G7	RTCK	JTAG - Test clock output	CORE	Digital output	O	-
G8	RESET_BB	Baseband reset	CORE	Digital Schmitt Trigger input	I	-
G9	TTS	JTAG - Test tap select	CORE	Digital input	I	-
G10	RFTEST-	RF negative differential monitor output (Reserved for production factory test only. Leave open)	RF	Analog output	-	-
H1	VCC_MIX	RF mixer supply	RF	Power line	-	-
H2	GND_BB	Baseband ground	CORE	Power line	-	-
H3	GND_RF	RF front end ground	RF	Power line	-	-
H4	GND_RF	RF front end ground	RF	Power line	-	-
H5	GND_RF	RF front end ground	RF	Power line	-	-
H6	GND_RF	RF front end ground	RF	Power line	-	-
H7	GND_RF	RF front end ground	RF	Power line	-	-
H8	RFTEST+	RF positive differential monitor output (Reserved for production factory test only. Leave open)	RF	Analog output	-	-
H9	TMS	JTAG - Test mode select input	CORE	Digital input	I	-
H10	N/C	Not connected	-	-	-	-
J1	VCC_LNA	RF LNA supply	RF	Power line	-	-
J2	VCC_PA	RF power amplifier supply	RF	Power line	-	-
J3	VDD_BB	Baseband core supply	CORE	Power line	-	-
J4	GND_RF	RF front end ground	RF	Power line	-	-
J5	GND_RF	RF front end ground	RF	Power line	-	-
J6	GND_RF	RF front end ground	RF	Power line	-	-
J7	GND_RF	RF front end ground	RF	Power line	-	-

Table 14. Pin Names and Functions (Continued)

J8	XTAL_BB	32.768 kHz baseband crystal clock output	CORE	Digital output	O	-
J9	TDI	JTAG - Test data input	CORE	Digital input	I	-
J10	TCK	JTAG - Test clock input	CORE	Digital Schmitt Trigger input	I	-
K1	RFIN	RF LNA input	RF	RF input (no ESD)	-	-
K2	EPAEN	RF External power amplifier enable	RF	Digital output	-	-
K3	PAOUT+	RF positive differential PA output	RF	RF output (no ESD)	-	-
K4	PAOUT-	RF negative differential PA output	RF	RF output (no ESD)	-	-
K5	GPO	General purpose output	RF	Digital output	-	-
K6	EPADRV	RF external PA driver DAC output	RF	Analog output	-	-
K7	GND_RF	RF logic ground	RF	Power line	-	-
K8	EXTAL_BB	32.768 kHz baseband external crystal clock input	CORE	Digital input	I	-
K9	TRST_B	JTAG - Test reset	CORE	Digital Schmitt Trigger input	I	-
K10	TDO	JTAG - Test data output	CORE	Digital tri-state output	O/L	-

4.2 Pin Descriptions

The following table provides detailed pin descriptions for the RF; clock, reset, and JTAG; Bluetooth; SSI and UART; and UART, SPI1, and TIM including the GPIO shared package pins.

In the following table, the general-purpose input/output (GPIO) is designed to share package pins with other peripheral modules on the chip. If the peripheral, which normally controls a given pin, is not required, then the pin may be programmed to be a general-purpose input/output (GPIO) or alternate function 2 with programmable pull-up. The GPIO module design has two available ports (Port B and Port C). The individual control for each pin can be in normal functional mode, alternate function mode 2, or GPIO mode. The individual direction control for each pin is in GPIO mode. The individual pull-up enable control for each pin is in normal function mode, alternate function mode 2, or GPIO mode.

- Normal mode. The peripheral module controls the output enable and any output data to the pad and any input data from the pad is passed to the peripheral.
- Alternate function 1 mode (GPIO). The GPIO module controls the output enable to the pad and supplies any data to be output.
- Alternate function 2 mode. The peripheral module controls the output enable and any output data to the pad and any input data from the pad is passed to the peripheral.

Not all power supply pins including ground pins are described in the following pin description list as all of these pins share the same name within the three power groups. Refer to Section 10, "Applications Information," for details on how to isolate and identify the correct configuration for the power supply pins.

Table 15. Pin Descriptions

RF Signals	
DCLF1	Data Clock Loop Filter charge pump output for external loop filter.
MNLF	Main Frac-N Loop Filter (Charge Pump). The external loop filter is referenced to VCC_RF in order to minimize transmit phase noise.
XEMIT	Reference oscillator emitter. A bias current of 50 μA is supplied internally to the emitter. This pin must be left open if external (not crystal) reference frequency is used.
XBASE	Reference oscillator base. The base is the reference oscillator input. An on-chip capacitor trim network is also included to allow the user to use relatively inexpensive crystals. This pin is also the feed-point in case of using external (not crystal) reference frequency.
RFTEST+	This pin is for factory use only. It must be left open.
RFTEST-	This pin is for factory use only. It must be left open.
RFIN	RFIN is the RF input to the LNA. The LNA is a bipolar cascode design. The input is the base of the common emitter transistor. Minimum external matching is required to optimize the input return loss and gain. The cascode output drives the primary of an on-chip balun single-ended.
PAOUT+	Positive differential PA output. An external differential-to-single-ended matching network is desired.
PAOUT-	Negative differential PA output. An external differential-to-single-ended matching network is desired.
EPAEN	External PA enable is a digital output which can be used to enable an external PA. It is normally placed under sequence manager control. This output can also be used to control an external Rx/Tx switch requiring complementary drive.
EPADRV	External PA driver DAC output. Analog output ranges from 0.02 to VCC_RF - 0.02. The EPADRV is linearly scaled to a maximum VCC_RF of 3.1 V.
GPO	The General Purpose Output is a digital output. GPO is normally controlled by the internal sequence manager but may also be programmable. This signal is typically used to control an external Rx/Tx switch.
Baseband Clock, Reset, and JTAG Signals	
EXTAL_BB	32.768 kHz baseband external crystal clock input. In case of using external clock, the signal must be fed to this pin, while leaving XTAL pin open.
XTAL_BB	32.768 kHz baseband crystal clock output. This pin must be left open in case of using external clock.
TDI	The test data input pin provides a serial input data stream to all TAP controllers. TDI is sampled on the rising edge of TCK. Leave open if JTAG is unused.
TDO	The test data output pin is tri-statable, providing serial output data from the Master TAP or ARM Core TAP controller. It is actively driven in the shift-IR and shift-DR controller states of the TAP controller state machine. TDO changes on the falling edge of TCK.

Table 15. Pin Descriptions (Continued)

TRST_B	This active low Schmitt trigger input pin provides an asynchronously reset signal to all TAP controllers to initialize the test controller. Leave open or pull-down if JTAG is unused.	
TMS	The test mode select input pin is used to sequence all TAP controllers. The TAP control module and the TTS device port determine the TAP sequenced. TMS is sampled on the rising edge of TCK. Leave open or pull-up if JTAG is unused.	
TCK	The test clock input pin is used to synchronize the JTAG test logic. It provides the clock to synchronize the test logic and shift serial data to and from all TAP controllers. Leave open if JTAG is unused.	
RTCK	The return test clock output pin returns the synchronization test clock to ARM development tools to be entered from the serial debug input line.	
TTS	The test tap select input pin directly controls the multiplexing logic to select between the chip TAP and the core TAP. A logic 1 applied to the tap select input will select the chip TAP. Leave open if JTAG is unused.	
MODE1	Test/boot mode select pins. In order to support a flexible development system, the system must be able to boot from different memories during system reset and power-up. This pin can select two of the four different memory maps, as MODE0 is hardwired internally. All the different boot modes start reading data at address 0x0000_0000, since this is where the ARM7 reset vector is located.	
RESET_BB	The reset in pin is an active low Schmitt trigger input that provides reset to the internal circuitry. The RESET input will be qualified as valid if it will be asserted for at least three CLK cycles.	
Bluetooth Signals		
REFCTRL	The reference control pin is a dedicated output from the clock reset module (CRM) which enables/ disables the reference clock.	
SSI and UART Signals		
SSI_SCK/GPIO_B0/GPIO_B3/BT_TP0/BT_TP3		
SSI_SCK	Normal mode	The serial transmit clock signal is used by the transmitter and can be either continuous or gated. The pin is normally used in synchronous mode. Two signals are internally connected in the chip to this pin. Use precautions when configuring these two signals, as the two internal signals must be configured to comply with each other.
GPIO_B0/ GPIO_B3	Alternate Function 1 (GPIO)	GPIO_0 or GPIO_3 on Port B. Two signals are internally connected in the chip to this pin. Use precautions when configuring these two signals, as the two internal signals must be configured to comply with each other.
BT_TP0/ BT_TP3	Alternate Function 2	Bluetooth test port signal. Two signals are internally connected in the chip to this pin. Use precautions when configuring these two signals, as the two internal signals must be configured to comply with each other.
SSI_FS/GPIO_B1/GPIO_B4/BT_TP1/BT_TP4		

Table 15. Pin Descriptions (Continued)

SSI_FS	Normal mode	The serial transmit frame sync signal is used by the transmitter to synchronize the transfer of data. The frame sync signal can be one bit or one word in length. Two signals are internally connected in the chip to this pin. Use precautions when configuring these two signals, as the two internal signals must be configured to comply with each other.
GPIO_B1/ GPIO_B4	Alternate Function 1 (GPIO)	GPIO_1 or GPIO_4 on Port B. Two signals are internally connected in the chip to this pin. Use precautions when configuring these two signals, as the two internal signals must be configured to comply with each other.
BT_TP1/ BT_TP4	Alternate Function 2	Bluetooth test port signal. Two signals are internally connected in the chip to this pin. Use precautions when configuring these two signals, as the two internal signals must be configured to comply with each other.
SSI_STD/GPIO_B2/BT_TP2		
SSI_STD	Normal mode	The serial transmit data signal is used to transmit serial data.
GPIO_B2	Alternate Function 1 (GPIO)	GPIO_2 on Port B.
BT_TP2	Alternate Function 2	Bluetooth test port signal.
SSI_SRD/GPIO_B5/BT_TP5		
SSI_SRD	Normal mode	The serial receive data signal is used to receive serial data.
GPIO_B5	Alternate Function 1 (GPIO)	GPIO_5 on Port B.
BT_TP5	Alternate Function 2	Bluetooth test port signal.
GPIO_B10/UART_TXD		
GPIO_B10	Alternate Function 1 (GPIO)	**Note:** GPIO_10 on Port B.
UART_TXD	Alternate Function 2	**Note:** Transmit data serial (output signal).
GPIO_B12/UART_RXD		
GPIO_B12	Alternate Function 1 (GPIO)	GPIO_12 on Port B.
UART_RXD	Alternate Function 2	Receive data serial (input signal).
UART, SPI1, and TIM Signals		
UART_TXD/GPIO_C0		
UART_TXD	Normal mode	UART transmit data serial (output signal).
GPIO_C0	Alternate Function 1 (GPIO)	GPIO_0 on Port C.
UART_CTS/GPIO_C1/SPI1_REQ		
UART_CTS	Normal mode	UART clear to send (CTS) output signal, when asserted, indicates that the MC72000 is ready to accept new data and the remote device can transmit when it has data to send.

Table 15. Pin Descriptions (Continued)

GPIO_C1	Alternate Function 1 (GPIO)	GPIO_1 on Port C.
SPI1_REQ	Alternate Function 2	External data transfer rate control for SPI1.
UART_RXD/GPIO_C2/TIM_0_I		
UART_RXD	Normal mode	UART receive data serial (input signal).
GPIO_C2	Alternate Function 1 (GPIO)	GPIO_2 on Port C.
TIM_0_I	Alternate Function 2	Input signal to timer 0.
UART_RTS/GPIO_C3/TIM_1_I		
UART_RTS	Normal mode	UART ready to send (RTS) input signal, when asserted, indicates that the remote device is ready to accept new data and that the MC72000 can transmit when it has data to send.
GPIO_C3	Alternate Function 1 (GPIO)	GPIO_3 on Port C.
TIM_1_I	Alternate Function 2	Input signal to timer 1.
SPI1_SS/GPIO_C4/SYSCLK		
SPI1_SS	Normal mode	Slave Select: This bi-directional signal is an output in master mode and an input in slave mode.
GPIO_C4	Alternate Function 1 (GPIO)	GPIO_4 on Port C.
SYSCLK	Alternate Function 2	System clock used by the entire ARM7 platform and all peripherals attached to the IP and AHB bus. Some of the peripherals (for example, UART) will also use this clock signal to generate their own module clock.
SPI1_SCK/GPIO_C5/SH_STROBE		
SPI1_SCK	Normal mode	This bi-directional signal is the SPI clock output in master mode. In slave mode, SPI1_SCK is an input clock signal to the SPI.
GPIO_C5	Alternate Function 1 (GPIO)	GPIO_5 on Port C.
SH_STROBE	Alternate Function 2	Indicates data is valid on the external bus when show cycle is used.
SPI1_MISO/GPIO_C6/ABORT		
SPI1_MISO	Normal mode	Master In Slave Out (MISO): In master mode, this bi-directional signal is the RXD input signal. In slave mode, MISO is the TXD output signal.
GPIO_C6	Alternate Function 1 (GPIO)	GPIO_6 on Port C.
ABORT	Alternate Function 2	Indicates the current memory access cannot be completed.
SPI1_MOSI/GPIO_C7/REFCLK		
SPI1_MOSI	Normal mode	Master Out Slave In (MOSI): In master mode, this bi-directional signal is the TXD output signal. In slave mode, MOSI is the RXD input signal.

Table 15. Pin Descriptions (Continued)

GPIO_C7	Alternate Function 1 (GPIO)	GPIO_7 on Port C.
REFCLK	Alternate Function 2	RF reference clock input (12-32 MHz).
CLK1/GPIO_C8/TIM_0_O		
CLK1	Normal mode	Output to external devices generated by the integer divider. CLK1 is a programmable clock and derivative of REFCLK. Frequencies are programmable in the range of REFCLK/64 to REFCLK. CLK1 can be used to feed an external USB, a CODEC, or whatever device the applications need. The integer divider should divide REFCLK with (1, 2, 4, 8, 16, 32, or 64). The value 0 disables the timer.
GPIO_C8	Alternate Function 1 (GPIO)	GPIO_8 on Port C.
TIM_0_O	Alternate Function 2	Output signal from timer 0.
GPIO_C9/XACK		
GPIO_C9	Alternate Function 1 (GPIO)	GPIO_9 on Port C.
XACK	Alternate Function 2	External acknowledge signal.
OSC32K/GPIO_C10/TIM_1_O		
OSC32K	Normal mode	Buffered output from the 32.768 kHz on-chip oscillator.
GPIO_C10	Alternate Function 1 (GPIO)	GPIO_10 on Port C.
TIM_1_O	Alternate Function 2	Output signal from timer 1.

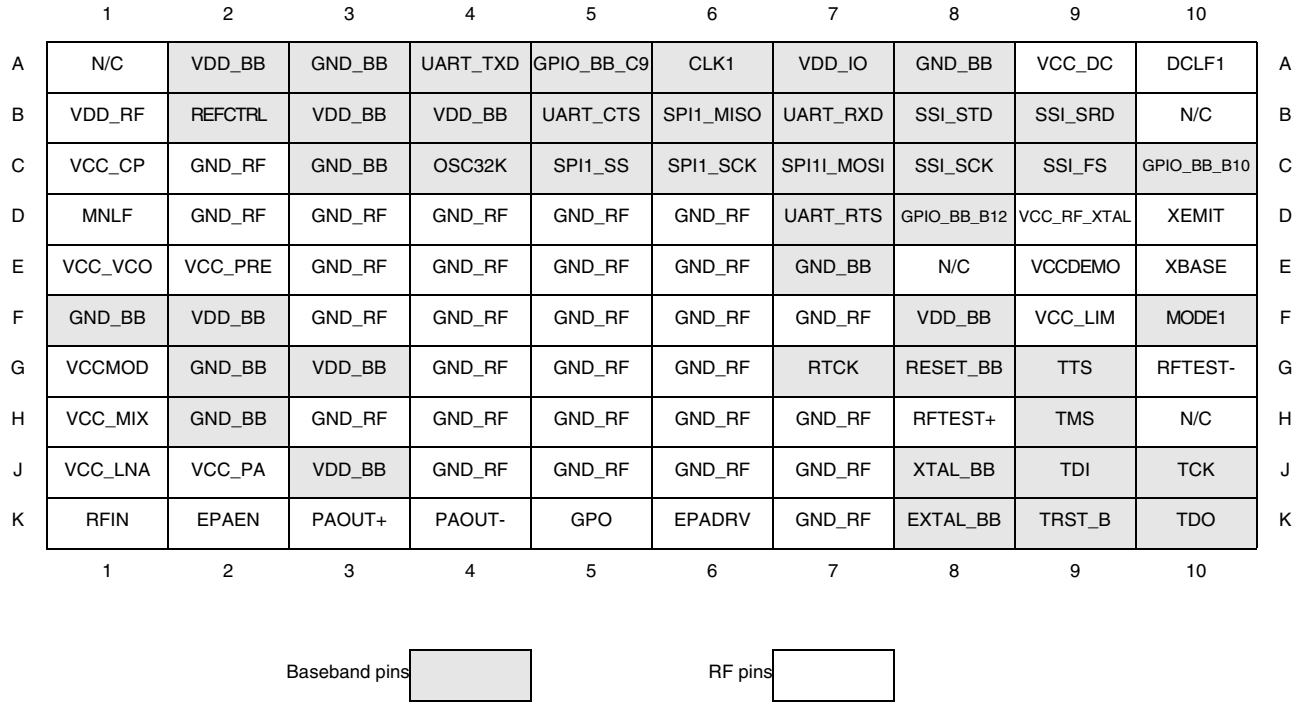


Figure 4. MC72000 Package Pinout (Top View)

5 System Description

This section describes the MC72000 system in more detail than in Section 2, “System Overview.” It also includes a section listing other documents of relevance (see Section 5.2, “Document References”).

5.1 MC72000 System Description

The detailed MC72000 design is shown in the block diagram in Figure 5.

Note that the voltages on the figure are the recommended setup of the MC72000, and the input frequencies are clocks and not crystals as in Figure 1.

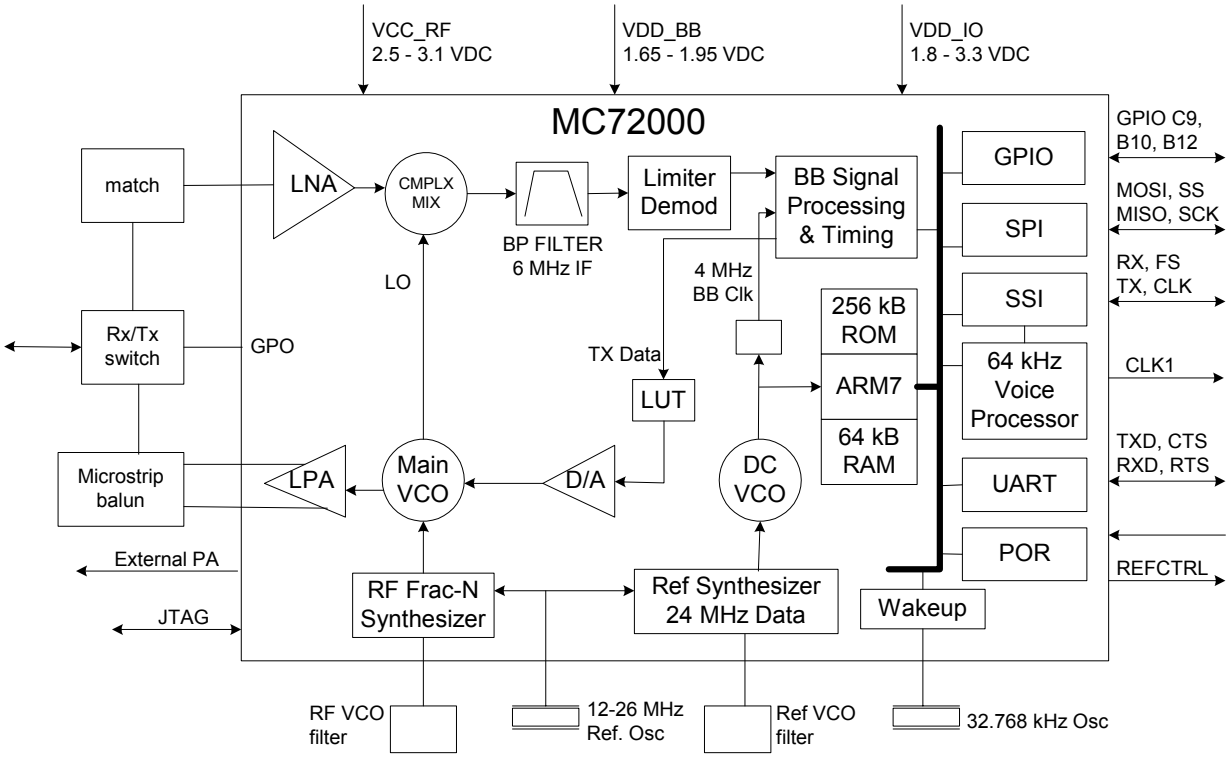


Figure 5. MC72000 Block Diagram

The following sections describe the different blocks of the MC72000.

5.1.1 ARM7 Processor

The MC72000 Bluetooth Baseband Controller architecture is based on the 32-bit ARM7TDMI microprocessor. It is an industry-standard processor recognized for its efficient MIPS/WATT benchmark, along with excellent code efficiency when working in the 16-bit THUMB mode. The architecture is based on RISC principles and supports two instruction sets:

- 32-bit ARM instruction set
- 16-bit THUMB instruction set

The ARM7 processor handles the high speed processing of data and link control management. The MC72000 has 64 Kb RAM and 256 Kb ROM embedded containing a full Bluetooth baseband and upper stacks. The ARM7 processor is primarily executing code from ROM and handles device initialization, power control, protocol behavior, and packet formatting.

The program execution in the MC72000 Bluetooth Baseband Controller is predominantly ROM-based, with internal RAM for data storage, application code, and ROM code patching. However, it is necessary to download the application software and configuration data into RAM from an external interface. This is done either as individual files when needed, as a complete image at power up containing all the files from a host system, or from a low-cost serial EEPROM (four-wire connection) connected to the serial peripheral interface (SPI).

5.1.2 Baseband Processor

The baseband processor digitally demodulates the signal at the output of the radio discriminator. Rather than immediately making a threshold decision based on the amplitude of the signal, it analyzes the waveform shape over more than one symbol before it makes a decision. This feature allows the Maximum Likelihood Sequence Estimation and Joint Detection algorithms (JD/MLSE) to improve adjacent channel rejection and signal acquisition. Without the joint detection and MLSE algorithms, it is possible to have high sensitivity but low throughput because of false/missing acquisitions and high interference. Joint detection provides simultaneous frequency and timing acquisition on the entire header rather than relying on just the synchronization portion.

5.1.2.1 Bluetooth Link Controller

The Bluetooth link controller module (BTLC) handles all link controller specific functions.

Raw data can be read from/written to the module, and the BTLC takes care of transmission-related timing, as well as data signal processing functions like encryption and cyclic redundancy check (CRC)/header error correction (HEC) generation. Embedded in the BTLC are also the dedicated Bluetooth timers, which maintain an accurate estimate of time in both the native and the remote module.

A small, dedicated Bluetooth serial peripheral interface controller handles all serial communication with the radio part of the MC72000 Integrated Bluetooth Radio.

The functionality of the baseband will be elaborated on in Section 8, “Bluetooth Baseband Functionality Overview.”

5.1.3 Bluetooth Radio

The design is based on Motorola's third-generation Bluetooth architecture that has set the industry standard for interoperability, complete functionality, and compliance with the Bluetooth specification.

The radio portion of MC72000 exhibits superior RF performance with small size and low cost. A minimum of external components are required to complete the RF link of a Bluetooth system, while maintaining superior performance.

5.1.3.1 Receiver

The receiver is a 6 MHz low-IF frequency type using analog image cancellation. The LO is set to either high-side or low-side injection so that the image will fall within the ISM band when the frequency to be received is set to edge of the ISM band. The integrated Bluetooth baseband automatically decides the use of high-side or low-side injection to the receiver, based on the active receive channel. The low-power integrated LNA and BPF exhibits the excellent sensitivity and noise rejection performance, which is further improved by the total system solution using the JD/MLSE baseband signal processing.

5.1.3.2 Transmitter

The shape of the transmit pulse as required by the Bluetooth specification is controlled by a look-up table that directly modulates the high frequency and accuracy main fractional VCO. The gain of the transmitter is adjustable, and pin connections for controlling an external PA are provided for Class 1 operation. The output of the PA is differential and, therefore, requires a balun that may be implemented in stripline or by using a discrete balun. The GPO pin controls the external antenna switch, which is set automatically by the internal sequence manager, and therefore requires no baseband interruption. As the transmitter section is a direct launch transmitter operating directly at the transmit frequency, the out-of-band spurious emissions are reduced to a minimum to comply with sensitive environments and strict requirements for other applications like cell phones, PDAs, and computer accessories.

5.1.4 Clock and Reset Module

The clock and reset module (CRM) is dedicated to handling all clock, reset, and power management features in the MC72000 Bluetooth Baseband Controller.

It ensures that the different clock and reset signals are stable before they are fed to the internal logic in the MC72000 Bluetooth Baseband Controller. The CRM is designed to make full use of the facilities supplied by the Bluetooth standard to conserve power, while still maintaining a Bluetooth link.

Two reference clocks are used to drive the MC72000: one for low power mode (32.768 kHz), and one for accurate transmit, receive, and timing operation. Reference frequency can be chosen to cover a great variety of typical reference frequencies used in cell phones, PDAs, and other equipment. This is due to an internal data clock VCO ensuring that the ARM7 processor always runs at the correct frequency. The internal crystal oscillator that feeds its clock to the data clock VCO and the radio portion covers the full supply and temperature range with its very low-noise and trimable reference frequency based on an external crystal. The oscillator may also be driven using an external reference clock from other applications with minimum load to the external application.

The CRM module also includes a watchdog to safeguard against potential software failures.

5.1.5 High-Speed UART

The universal asynchronous receiver/transmitter (UART) module provides one of the main interfaces to the MC72000 Bluetooth Baseband Controller. The generated baud rate is based on a configurable divisor and input clock. The UART transmit and receive buffer sizes are 32 bytes each.

5.1.6 High-Speed CSPI

The MC72000 Bluetooth Baseband Controller contains one configurable serial peripheral interface (CSPI) module, CSPI1. CSPI1 may be connected to a variety of SEEPROM and serial flash devices. They are described in Section 10.8.7, “Possible EEPROM Types.”

The CSPI module is master/slave configurable, equipped with 16 byte data out buffers (transmit and receive FIFOs), and allows the MC72000 Bluetooth Baseband Controller to interface with external CSPI master or slave devices. It enables fast data communication with a fewer number of software interrupts by incorporating the SPIRDY and SS control signals.

5.1.7 High-Speed SSI

The synchronous serial interface module (SSI) is a full-duplex serial port allowing digital signal processors (DSPs) to communicate with a variety of serial devices, including industry-standard CODECs, other DSPs, microprocessors, and peripherals. The SSI is typically used to transfer samples in a periodic manner and consists of a variety of registers that handle port, status, control, transmit and receive, serial clock generation, and frame synchronization.

5.1.8 Bluetooth Audio Signal Processor

High audio quality is of great importance to the end user. Section 10.9, “Audio,” describes the audio features.

A dedicated Bluetooth audio signal-processing module (BTASP) has been designed to give users superior audio performance. The BTASP module handles all filtering, interpolation, as well as encoding/decoding with a minimum of processor intervention.

The internal voice-processing unit converts raw 16-bit PCM voice data and compressed voice data to uncompressed voice. Compression modes are A-Law, μ-Law, and CVSD. It performs filtering and accepts CODEC rates of 8, 16, 32, and 64 kbits/sec.

An external CODEC connected to the synchronous serial interface (SSI) is required for voice processing, if needed.

5.1.9 Timer

The dual timer module (TMR) is a general purpose module, used for timing control and application-specific tasks. The TMR can also be configured to perform pulse width modulation (PWM) or put into a quadrature-count mode if needed. The TMR contains two identical 16-bit counter/timer groups, each of which supports counting, prescaling, comparing, loading, capturing, and holding options.

5.1.10 General Purpose Input/Output

The MC72000 Bluetooth Baseband Controller supports a maximum of 16 GPIO lines grouped in two ports. Port B contains 6 lines, Port C contains 10 lines. These ports can be configured as GPIO pins or dedicated peripheral interface pins.

5.1.11 JTAG Test Interface Controller

The JTIC interface offers full JTAG and boundary scan capabilities for debug and production test purposes, as well as access to the JTAG interface on the ARM.

5.2 Document References

The following is a list of documents providing additional information or implementation guidance for different systems.

MC72000-related documents:

1. *Motorola Bluetooth File System, Overview Application Note* (document number 94001481001)
2. *Motorola Bluetooth File System, Host-based General Application Note* (document number 94001481003)
3. *Motorola Bluetooth File System, Host Based One File Application Note* (document number 94001481004)
4. *Motorola Bluetooth File System, Embedded File System Application Note* (document number 94001481002)
5. *Motorola Bluetooth Solutions, Bluetooth Qualification Application Note* (document number AN2386/D)
6. *UART/SSI Configuration User´s Guide* (document number 94001481900)
7. *Vendor-Specific HCI Reference* (public) (document number 79000001800).
8. *Specification of the Bluetooth System* (22 Feb. 2001, v.1.1)—official book available from: http://www.bluetooth.com.

Implementation-related documents:

1. *Bluetooth IC File System File Formats Application Note* (document number 94001481200).
2. *MC72000 Implementation for Cellular Phones Application Note* (document number 94001481800)
3. *MC71000/MC72000 Wake-Up, Reset, and Host Clock Request Sequences Application Note* (document number AN2340/D)
4. *Production Test Application Note* (document number 94001481100)

6 Radio Functional Description

NOTE:

In the following description, control bits contained in the MC72000 Radio Register Map for various functions will be identified by register number and bit number(s). For example, bit R4/8 references bit 8 of register 4 while R5/9-3 identifies bits 9 through 3, inclusive, of register 5 (decimal notation). Unless otherwise noted, a default register map configuration as listed in Figure 94 is assumed. The information contained in this section will describe in detail how to calculate and find the appropriate values of the MC72000 Radio Register Map in your specific setup. The information that concerns the radio performance and its ability to function, consisting of the MC72000 Radio Register Map and a Main Synthesizer Channel Table, is gathered and assembled in the File410x.vfs in the Motorola Bluetooth File System. Refer to Section 5.2, “Document References,” for details on the file system.

6.1 RF Receive Chain

The MC72000 is placed into the receive mode from the idle mode by asserting the internal RXTXEN master signal after setting the Radio Receive Enable bit (R2/13), clearing the Radio Transmit Enable bit (R2/14), and clearing the Radio Narrow Bandwidth Enable bit (R2/12). The data represents a 6-Bit, 2's-complement digital value and is sampled four times for every data bit. Once the receive cycle is complete, the RXTXEN master signal to the radio is deasserted and the MC72000 begins an internal power down sequence. This is all controlled by the internal baseband processor. The receive chain is optimized to provide high adjacent channel rejection, which is the most important specification in a high interference environment. This is accomplished by setting the IF bandpass filter to 720 kHz and then using Maximum Likelihood Sequence Estimation (MLSE) in baseband processing to remove the effects of intersymbol interference.

A low voltage SPI interface is used between the radio and the baseband processor. The baseband synchronizes the radio timing through the master RXTXEN signal to the radio. A logic low transition on this signal indicates the beginning of idle state, while a logic high transition indicates either transmit or a receive cycle.

6.2 RF Transmit Chain

The MC72000 is placed into the transmit mode from the idle mode by setting the Radio Transmit Enable bit (R2/14), setting the Radio Narrow Bandwidth Enable bit (R2/12), and clearing the Radio Receive Enable bit (R2/13) of the Radio Register Map, then asserting the RTXEN pin of the device. Once the data stream has been transmitted, the RTXEN pin is deasserted and the MC72000 begins an internal power down sequence. Since RF power is still present at the PA output, no SPI operations or additional cycles between the radio and the baseband processor can be performed until a certain amount of time has passed after the deassertion of RXTXEN. At this time, RF power is at a substantially low enough level so as not to produce undesired emissions. The internal baseband processor also handles this timing.

6.3 Receiver

The MC72000 receiver is intended to be used in Time Division Duplex (TDD), Frequency Hopping Spread Spectrum (FHSS) Bluetooth applications. The receiver uses a low intermediate frequency (IF) of 6.0 MHz and is capable of receiving up to 1.0 Mbit/s Gaussian Frequency Shift Keyed (GFSK) serial data through the entire 2.4 GHz Industrial, Scientific, and Medical (ISM) band. The output of the receiver is a demodulated, serial bit stream of 24 Mbit/s data. This data represents a 4X over sample by a 6-bit D/A of the actual demodulated analog data recovered from the desired channel. A detailed discussion of each of the functional blocks within the receiver is provided in the following sections.

6.3.1 LNA

The first portion of the receiver chain is the Low Noise Amplifier (LNA). The LNA is a bipolar cascode design and provides gain with low noise at RF frequencies. The LNA is designed with a single-ended (unbalanced) input and is converted to a differential (balanced) output by means of an on-chip, integrated balun.

For optimum performance, the LNA input impedance must be matched to the complex conjugate of the source impedance (usually 50 Ω).

The LNA of the MC72000 exhibits two distinctly different impedances depending upon whether the LNA is active or disabled. During a receive cycle, the S11 of the LNA is shown in the Table 16.

Table 16. S11 for LNA During Receive

Frequency	MAG (dB)	Angle (degree)
2.45 GHz	TBD	TBD

The LNA can be matched to 50 Ω by a simple capacitor/inductor network as shown in Figure 6.

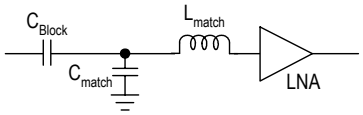


Figure 6. Simple Capacitor/Inductor Network

When the LNA is disabled or the device is in the Idle or Transmit mode, the impedance of the LNA becomes the value shown in Table 16.

Table 17. S11 for LNA Disabled

Frequency	MAG (dB)	Angle (degree)
2.45 GHz	TBD	TBD

The use of an antenna switch to interface the LNA with an antenna is the preferred circuit configuration as shown in Figure 92.

In this implementation, a true RF Single-Pole, Double-Throw (SPDT) switch is used to isolate the PA output from the LNA input during receive and transmit modes. A 1/4 wavelength trace is not required. As a result, this implementation has the highest performance (due to the lowest loss) and smallest size at the penalty of increased system cost. An external switch must be used for Class 1 Bluetooth devices as the LNA input will become overloaded if not sufficiently isolated from the external PA output. The LNA provides a nominal 6.7 dB of power gain when properly matched. The LNA is enabled approximately 150 µs after the assertion of the RTXEN pin when programmed for Receive mode. It is disabled immediately after the deassertion of the RTXEN pin or during any Idle or Transmit mode.

6.3.2 High/Low Image Reject Mixer (I/R Mixer)

The mixer is used to convert the desired RF channel to a 6.0 MHz Intermediate Frequency (IF). The mixer is completely balanced on all ports, and the local oscillator (LO) is derived from the buffered output of the on-chip voltage controlled oscillator (VCO).

In general, it is desirable to keep all image frequencies in-band. Therefore, when receiving the six lowest channels, the mixer can be programmed for high-side injection and the LO will be programmed to be 6.0 MHz above the desired channel frequency. When receiving the six highest channels, the mixer can be programmed for low-side injection, and the LO will be programmed to be 6.0 MHz below the desired channel frequency. This is shown in Figure 7. Selection of high or low side injection is accomplished by bit R2/11 of the register map. For all other in-band channels, the choice of high or low side injection is arbitrary. The baseband uses high-side injection for frequencies up to 2.441-GHz inclusive and low-side injection thereafter.

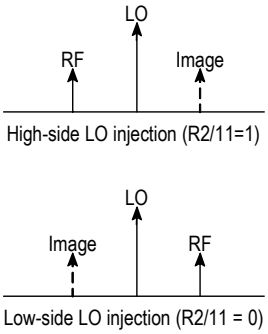


Figure 7. High-Side and Low-Side Mixer Injection

The mixer delivers approximately 15.8 dB of voltage gain and 22 dB of image rejection.

The mixer is enabled approximately 150 µs after the assertion of the RTXEN pin when programmed for Receive mode. It is disabled immediately after the deassertion of the RTXEN pin or during any Idle or Transmit mode.

6.3.3 Bandpass Filter (BPF)

The 6.0 MHz bandpass filter is used to block undesired channels. The filter is self-adjusting and is calibrated during each receive cycle, based on an internally generated 6.0 MHz signal. The gain of the filter is fixed at 4.0 dB.

The nominal pass band for the filter is 720 kHz. This deliberately low pass band can cause significant intersymbol interference (ISI) issues for a GFSK modulated signal with a 1 Mbit/s data rate. The advantages are increased sensitivity, adjacent channel interference performance, and ease of manufacture. Due to this low pass band, a digitally implemented decoder scheme is utilized to eliminate ISI. This is referenced as the JD/MLSE and is incorporated into all Motorola Bluetooth basebands.

The BPF is enabled approximately 10 µs after the assertion of the RTXEN pin while programmed for Receive mode and automatic tuning is complete after approximately 140 µs. It is disabled immediately after the deassertion of the RTXEN pin or during any Idle or Transmit mode.

6.3.4 Limiter with Received Signal Strength Indicator (RSSI)

The received signal strength indicator (RSSI) is integrated into the limiter. The RSSI ADC converts the RSSI current into a 4-bit digital signal. When the RSSI enable (R4/6) and RSSI Read Enable (R9/8) are both set, the 4-bit RSSI conversion value can be read from the MC72000 Radio Register Map (R29/3-0) while in Idle mode. The RSSI is updated approximately 40 µs after receiving the first bit in a receive cycle. Enabling RSSI will result in additional current consumption as noted in the Receiver AC Electrical Specifications shown in Table 8. Figure 8 shows the RSSI conversion value versus the RF level input to the LNA at various temperatures. Figure 9 shows the RSSI conversion versus the RF level at different power supplies.

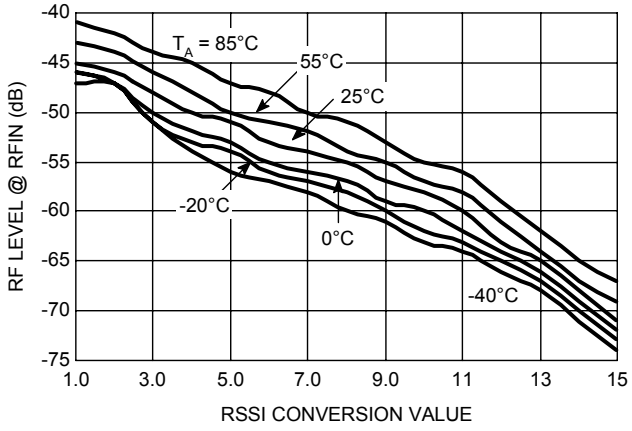


Figure 8. RF Level vs. RSSI at Temperature

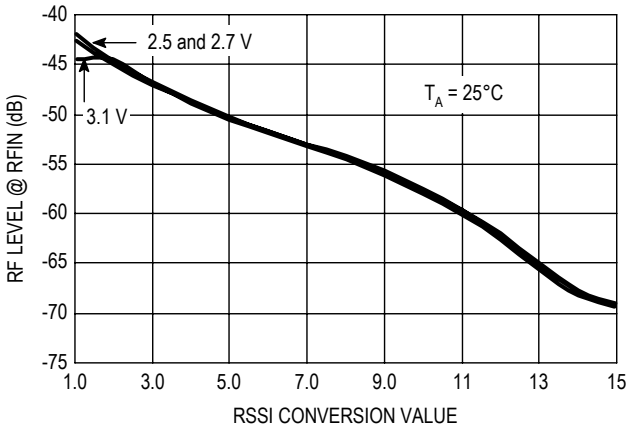


Figure 9. RF Level vs. RSSI at V_{CC}RF

6.3.5 Demodulator

The receiver in the MC72000 down converts the RF signal and demodulates it. The demodulator takes the IF signal from the limiter and delivers a baseband signal to an A/D converter (ADC). The 6-bit ADC uses the Redundant Sign Digit (RSD) Cyclic architecture that samples the analog input at 4.0 Msamples/s. The resulting demodulated data out of the MC72000 is a 24 Mbit/s, 2's-complement serial bit stream. The start of each 6-bit data stream is indicated by a frame sync (FS) signal internal to the baseband processor. A 24 MHz clock output accompanies the demodulated data.

6.3.5.1 Receiver Characteristics

For optimum intermodulation and C/I performance, the MC72000 GND_RF pins require good conduction to the PCB ground layer. Figure 10 through Figure 16 show typical performance of the receiver for various conditions.

TBD

Figure 10. Receive Sensitivity vs. Temperature

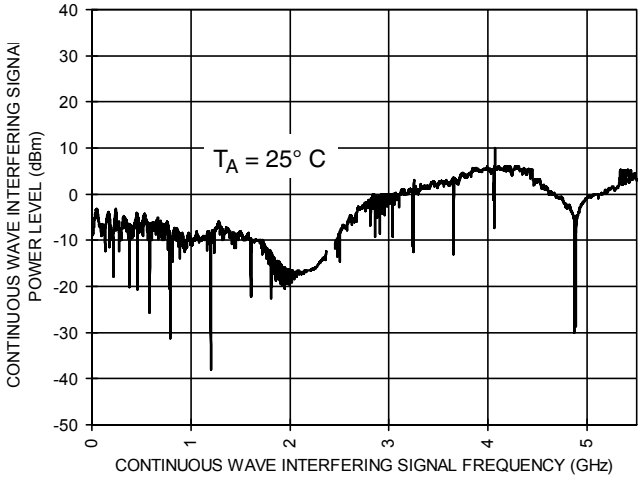


Figure 11. Blocking Performance vs. Continuous Wave Interfering Signal

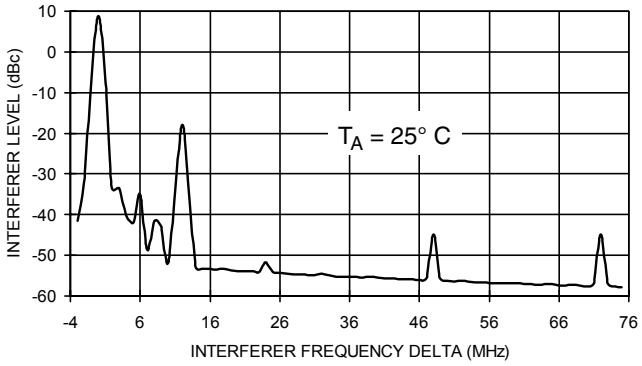


Figure 12. C/I Performance for Channel 3 (2.405 GHz, High-Side Injection)

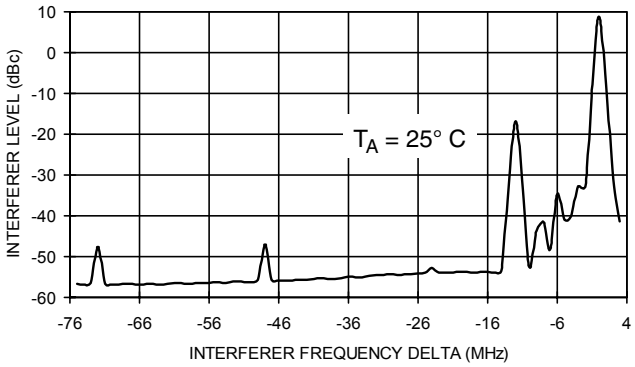


Figure 13. C/I Performance for Channel 75 (2.477 GHz, Low-Side Injection)

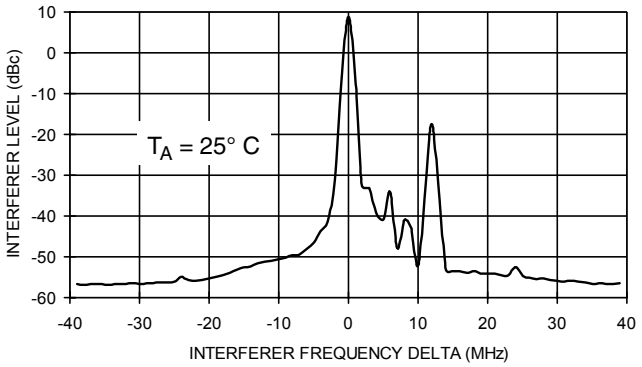


Figure 14. C/I Performance for Channel 39 (2.405 GHz, High-Side Injection)

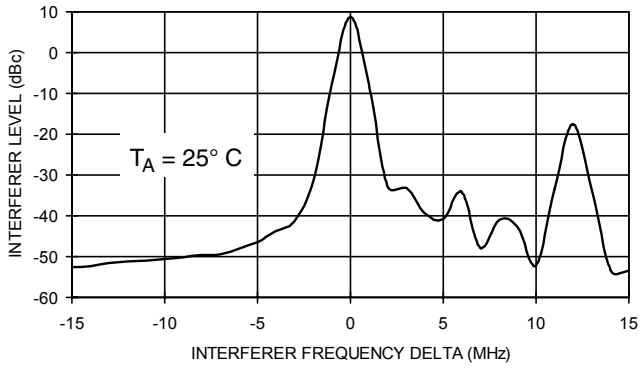


Figure 15. C/I Performance for Channel 39 (2.405 GHz, High-Side Injection)

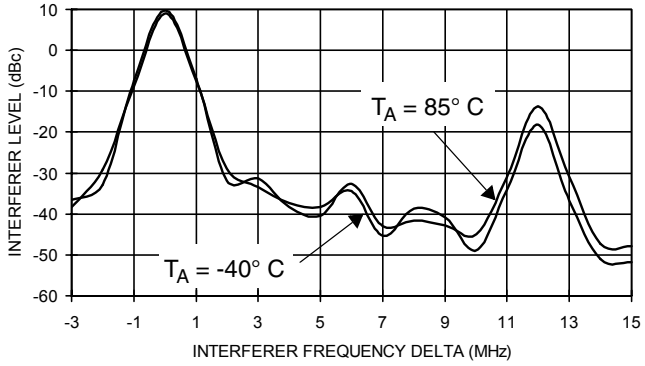


Figure 16. C/I Performance vs. Temperature

6.4 Transmitter

The MC72000 uses a direct launch transmitter taken from the output of the local oscillator (LO). During a transmit cycle the VCO of the LO is automatically trimmed. Following the LO are the output power stages, sequenced in the proper order. To minimize splattering, the output of the programmable low power amplifier (LPA) drives a balanced ramp up/ramp down generator, which is fed to a "Balun" to provide a single-ended output for the external antenna switch. The transmit start up/warm down sequences are shown in Figure 30.

6.4.1 Transmit Synchronization Delay

A programmable delay exists between the rising edge of RTXEN and the first available bit of on-the-air data during a transmit cycle. This delay range is TX_{sync} and is set via Radio Register Map bits of Transmit Synchronization Time Delay Value (R8/15-8) where the decimal value represents the delay in microseconds. Packet data is seen at the antenna approximately 2.5 µs after this delay. All Bluetooth packets require a minimum of four preamble bits of pattern 0101 or 1010. For minimum power consumption, set the delay to TX_{sync} minimum. If additional settling time or preamble bits are required, manipulate the delay as necessary, up to TX_{sync} maximum.

6.4.2 Main Synthesizer Operation

The internal local oscillator (LO) of the MC72000 is derived from the external reference frequency by means of a 3-accumulator, fractional-N synthesizer. The external low pass filter (C14/R1 of Figure 3) has a corner frequency of approximately 140 kHz. The external low pass filter requires two or three passive components, dependent on the reference frequency.

$\mathbf{f_{dev}}$ is the nominal transmit ROM frequency deviation (typically 157500 Hz).

I is the integer portion of the fractional synthesizer.

R is the numerator portion of the fractional synthesizer.

$\mathbf{f_{ref}External}$ is the external reference frequency.

LO is the desired local oscillator frequency then,
I = (LO/f_{ref}External - f_{dev}/f_{ref}External) - 3
R = REM(LO/f_{ref}External - f_{dev}/f_{ref}External) x 2^{16}
where the INT function is the integer portion of the result and REM is the remainder portion of the result.

An example is shown below:

$\mathbf{f_{dev}}$ = 157500 Hz

LO = 2.441 GHz

$\mathbf{f_{ref}External}$ = 13 MHz

then,

I = INT(2.441 GHz/13 MHz - 157.5 kHz/13 MHz) - 3 = 184_{10}

R = REM(2.441 GHz/13 MHz - 157.5 kHz/13 MHz) x 2^{16} = 49618_{10}

Accuracy to at least 10 decimal places is suggested.

6.4.3 Transmit ROM Operation

The MC72000 uses a look-up table (LUT or Transmit ROM) to shape incoming transmit data bits and produce a Gaussian filtered mask with BT=0.5. The value of the current data bit, along with knowledge of the previous two bits, determines a unique trajectory for shaping. Only four unique trajectories are required to implement this filter, and due to the symmetrical nature of the Gaussian response, these trajectories can be reduced to a single quadrant. Furthermore, without compromising accuracy, this table can be reduced to only 11 values.

The output of the LUT is fed to the accumulators of the fractional synthesizer. The seven MSBs are eventually fed to the second port of the main VCO during transmit operation (see Figure 17). For receive operation, the output of the LUT is constantly held to the value contained in R1C1.

These 11 trajectory constants are listed in Table 18 (see also Figure 94, Radio Register Map). The actual value to place in the LUT is calculated as:

LUT $RxCx_{b10}$ = (f_{dev}/f_{ref}External) x 2^{16} x (RxCx constant)

This number is then rounded and converted to binary:

LUT RxC_{xb2} = INT((LUT $RxCx_{b10}$+2)/4)

where the INT function is the integer portion of the result.

As an example for calculating the LUT value for R4C2 and f_{ref}External = 13 MHz:

LUT R_4C_{2b10} = (157.5 kHz/13.0 MHz) x 2^{16} x 0.5229292198 = 415.2

LUT R_4C_{2b2} = INT((415.2+2)/4) $_{b10}$ = INT(104.3) $_{b10}$ = 104 $_{b10}$ or 011010000 $_{b2}$ or 68_{b16}

The following table lists all values of RxCx for supported reference.

Table 18. RxCx Constants

R1C1	0.9999739537
R2C2	0.9980246857
R2C3	0.9911665663
R2C4	0.9678427310
R3C1	0.1881990082
R3C2	0.5249014674
R3C3	0.7660791186
R3C4	0.9043672052
R4C2	0.5229292198
R4C3	0.7572459756
R4C4	0.8722099597

6.4.4 M-Dual Port Multiplier and B-Dual Port Multiplier

For proper operation of the dual-port synthesizer, it is necessary to maintain a constant deviation injection at the input of Port 2 of the VCO. As appears from the Transmit ROM operation and Figure 17, the output of the LUT is fed to a digital multiplier prior to being presented to the input of the modulation DAC. Since the LUT values decrease proportionately with input reference frequency, the multiplier must scale these values to achieve a constant deviation. This scaling is linear. Two programmable constants are used to form the equation of a line, the M & B dual-port multipliers. M-Dual Port Digital Multiplier Value (R17/15-8), determines the slope, and B-Dual Port Digital Multiplier Value (R8/7-0), determines the intercept.

M-Dual Port Digital Multiplier = (f_{ref}External) /13 MHz * 108_{10}

B-Dual Port Digital Multiplier = (f_{ref}External) /13 MHz * 97_{10}

Table 20 contains slope and intercept point values across all supported input reference frequencies.

6.4.5 Dual-Port Programmable Delay (R7/15-11)

It is necessary to maintain a constant deviation at Port2 of the VCO. Likewise, it is necessary to maintain a constant phase at the FV and FR inputs of the main charge pump. The total delay from the output of the LUT to the FV input of the charge pump is given as follows:

LUT $\rightarrow$ FV delay = 10.5 / (f_{ref}External)

Likewise, the total delay from the LUT to the FR input of the charge pump is as follows:

LUT $\rightarrow$ FR delay = 28 ns + Delay

where delay is the programmed delay value shown in Table 19. Therefore, for a given external reference frequency:

Delay = 10.5 / (f_{ref}External) - 28 ns.

Consult Table 19 for the closest available value.

Table 20 lists all values of the programmable delay for supported reference frequencies.

Table 19. Dual-Port Programmable Delay Values

R7/15-11 (decimal)	**$Delay_{b10}$** (ns)	**R7/15-11** (decimal)	**$Delay_{b10}$** (ns)
4	167	13	542
5	208	14	583
6	250	15	625
7	292	16	667
8	333	17	708
9	375	18	750
10	417	19	792
11	458	20	833
12	500	21	875

Table 20. Register Settings and Component Values vs. Reference Frequency

Note: (All register setting values in hex notation)

Register	Fref= 12 MHz	Fref= 13 MHz	Fref= 14.40 MHz	Fref= 15.26 MHz	Fref= 16.80 MHz	Fref= 19.22 MHz	Fref= 19.44 MHz	Fref= 19.68 MHz	Fref= 19.88 MHz	Fref= 26 MHz
Data Clk R (R6/9-0)	258	28A	2D0	2FB	348	3C1	3CC	3D8	3E2	28A
Data Clk N (R7/10-0)	4B0	4B0	4B0	4B0	4B0	4B0	4B0	4B0	4B0	258
R1C1 (R12/7-0)	D7	C6	B3	A9	9A	86	85	83	82	63
R2C2 (R12/15-8)	D7	C6	B3	A9	99	86	84	83	82	63
R2C3 (R13/7-0)	D5	C5	B2	A8	98	85	84	82	81	62
R2C4 (R13/15-8)	D0	C0	AD	A4	95	82	80	7F	7E	60
R3C1 (R14/7-0)	28	25	22	20	1D	19	19	19	18	12
R3C2 (R14/15-8)	71	68	5E	59	51	46	46	45	44	34
R3C3 (R15/7-0)	A5	98	89	82	76	67	66	64	63	4C
R3C4 (R15/15-8)	C2	B4	A2	99	8B	79	78	77	75	5A
R4C2 (R16/7-0)	70	68	5E	58	50	46	45	45	44	34
R4C3 (R16/15-8)	A3	96	88	80	74	66	65	63	62	4B
R4C4 (R17/7-0)	BC	AD	9C	93	86	75	74	72	71	56
M-Dual Port Multiplier (R17/15-8)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
B-Dual Port Multiplier (R8/7-0)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Dual Port Programmable Delay (R7/15-11)	14	13	11	10	E	C	C	C	C	9
R1 (kΩ)	27	27	24	22	20	18	18	18	18	13
C14 (pF)	270	270	270	330	330	390	390	390	390	560

Table 20. Register Settings and Component Values vs. Reference Frequency (Continued)

Note: (All register setting values in hex notation)

Register	Fref= 12 MHz	Fref= 13 MHz	Fref= 14.40 MHz	Fref= 15.26 MHz	Fref= 16.80 MHz	Fref= 19.22 MHz	Fref= 19.44 MHz	Fref= 19.68 MHz	Fref= 19.88 MHz	Fref= 26 MHz
C11 (pF)	0	0	0	0	0	4.7	4.7	4.7	4.7	10

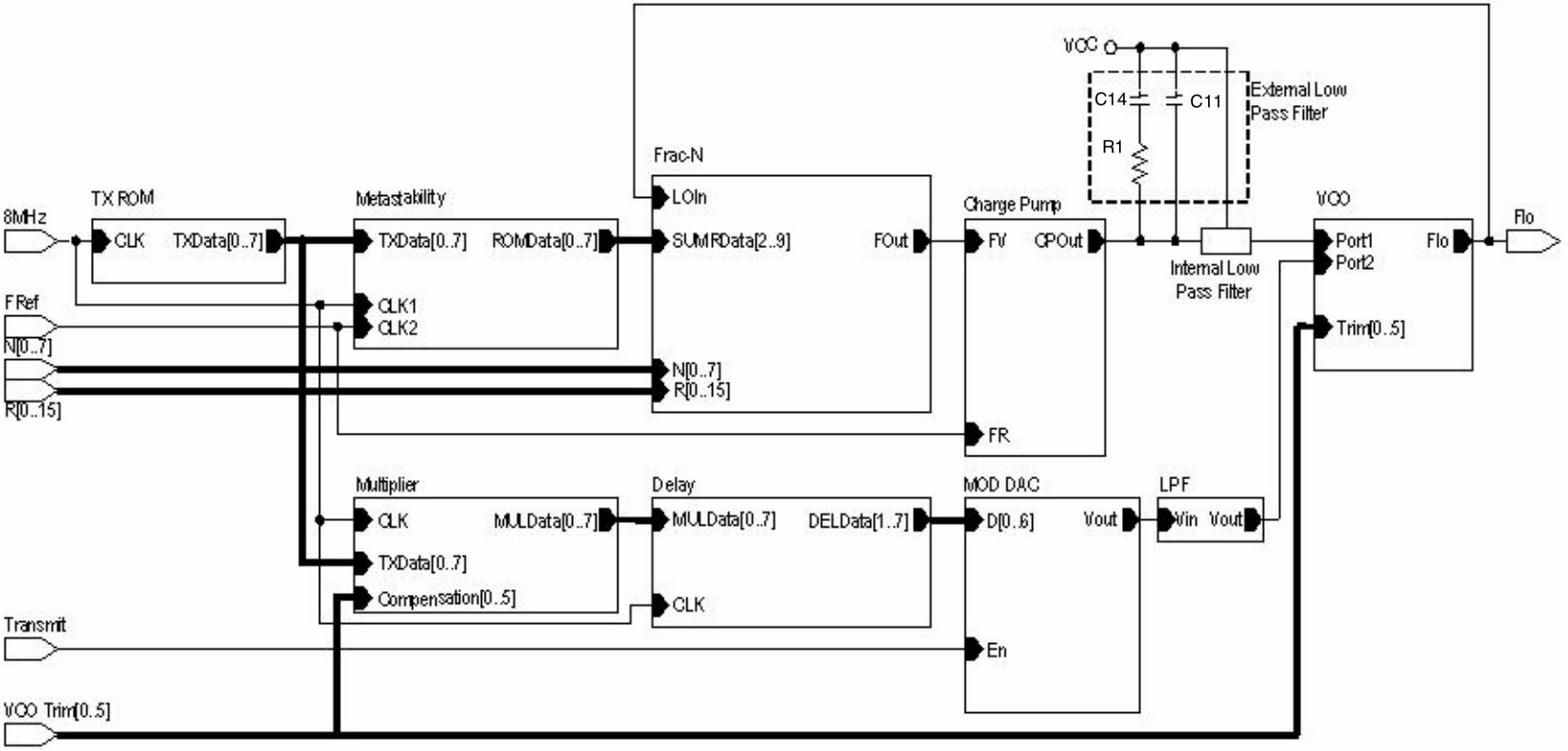


Figure 17. Main PLL Synthesizer Block Diagram

6.4.6 Programmable LPA

The output power of the LPA can be varied by programming PA Bias Adjust (R5/2-0) in the register map. Table 21 displays the response of RF output power, current consumption and 2nd Harmonic power level with respect to the programmable bit settings. Class 1 operations are supported through the use of an external power amplifier not shown here. Refer to Section 10.6, "Class 1 Operation," for more detail. Figure 18 and Figure 19 provide additional LPA characteristic data.

The LPA also includes a ramp generator which has an exponential ramp up/ramp down function with a maximum settling time of 20 µs. Increasing the output power exponentially is useful to avoid splattering and minimize load pulling.

6.4.7 External Balun

The LPA provides a differential output that is converted to a single-ended signal through the use of an inexpensive printed circuit board balun. Optionally, an external discrete balun may be used. Figure 20 and Figure 92 show the physical dimensions and characteristics of this network. Table 22 shows the output impedance, S22 of the PA during active and inactive cycles.

Table 21. RF Power Out vs. PA Bias Adjust

PA Bias Adjust			Output Power (dBm)	Current Consumption (Continuous Transmit)(mA)	2nd Harmonic (dBc)
R5/2	R5/1	R5/0			
0	0	0	TBD	TBD	TBD
0	0	1	TBD	TBD	TBD
0	1	0	TBD	TBD	TBD
0	1	1	TBD	TBD	TBD
1	0	0	TBD	TBD	TBD
1	0	1	TBD	TBD	TBD
1	1	0	TBD	TBD	TBD
1	1	1	TBD	TBD	TBD

Figure 18. RF Output Power vs. Carrier Frequency

Figure 19. RF Output Power vs. Temperature

Figure 20. Balun Physical Dimensions

Table 22. S22 for PA During Transmit

Note: (R5/2-0 = 010)(Measured Differential-Ended)

Operation Mode	**Frequency** (GHz)	**MAG** (dB)	**Angle** (degree)
Active	2.45	TBD	TBD
Inactive	2.45	TBD	TBD

6.5 Crystal Oscillator

The crystal oscillator provides the reference for the data clock PLL and main PLL. It can be configured as a Colpitts type (negative resistance) oscillator and utilize an external parallel resonant crystal or may be driven from an external source. The oscillator circuit has an on-chip capacitor trim network that provides the capability to compensate for crystal and/or load capacitor tolerances. This allows the use of relatively inexpensive crystals with as much as 50 ppm tolerance. The oscillator also provides three bias current modes. Xtal Enable (R11/0) enables/disables the bias current and Xtal Boost Enable (R11/4) enables/disables a high current mode. Refer to the Reference Oscillator Electrical Characteristics in Table 11 for the available current modes. Table 23 gives examples of parallel trim capacitances that can be programmed to register map location Xtal Trim (R6/14-10). Typical stray capacitance is on the order of 1.0 pF.

To drive the oscillator with an external source, program the Xtal Enable (R11/0) to zero and AC-couple the external signal into the oscillator base with a 15 to 100 pF capacitor. It is also recommended to set Radio Xtal Trim (R6/14-10) to zero to reduce the load on the external source. The external source may be either a sine or a square as long as it is AC-coupled and keeps the requirements for phase noise, amplitude, and duty cycle in Table 11. Additional characteristic data is shown in the following figures.

Table 23. Examples of Programmable XTAL Trim Capacitances

XTAL Trim (R6/14-10) Setting (MSB to left)	**Electronic Parallel Crystal Trim Capacitance (C_{PT})**
00000	0 pF
00100	1.2 pF
10000	4.8 pF
10101	6.3 pF
11111	9.3 pF

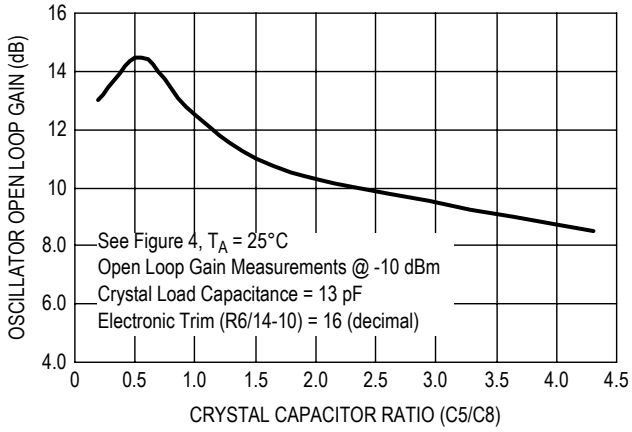


Figure 21. Oscillator Open Loop Gain vs. Capacitor Ratio

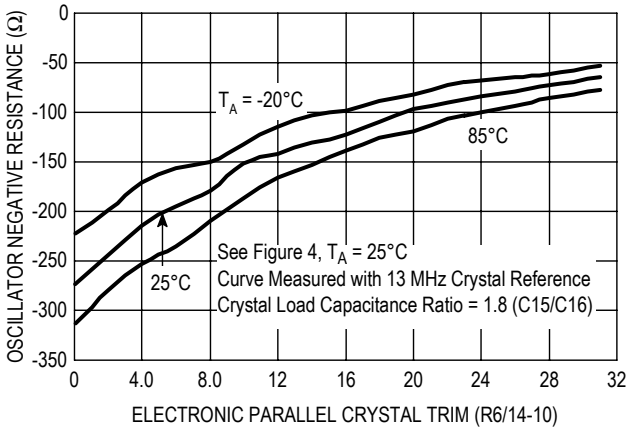


Figure 22. Oscillator Negative Resistance vs. Electronic Parallel Crystal Trim (C_{PT})
(Crystal Boost Enable R11/4) = 0

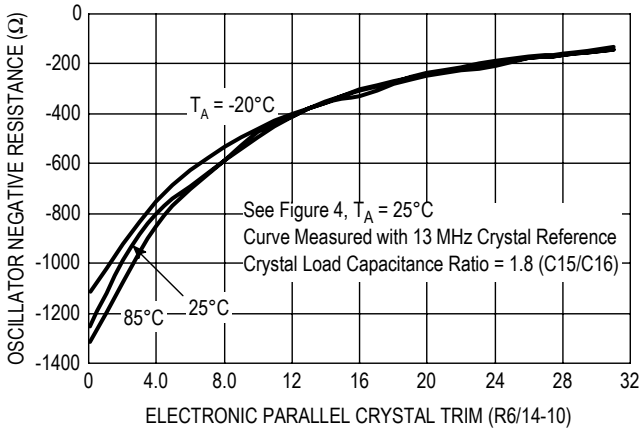


Figure 23. Oscillator Negative Resistance vs. Electronic Parallel Crystal Trim (C_{PT})
(Crystal Boost Enable R11/4) = 1

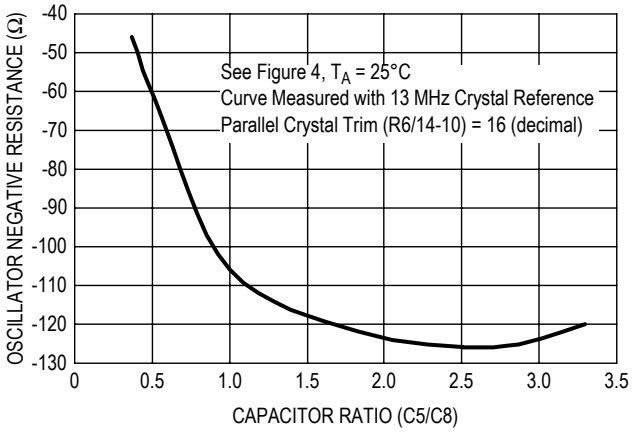


Figure 24. Oscillator Negative Resistance vs. Crystal Capacitor Ratio
(Crystal Boost Enable R11/4) = 0

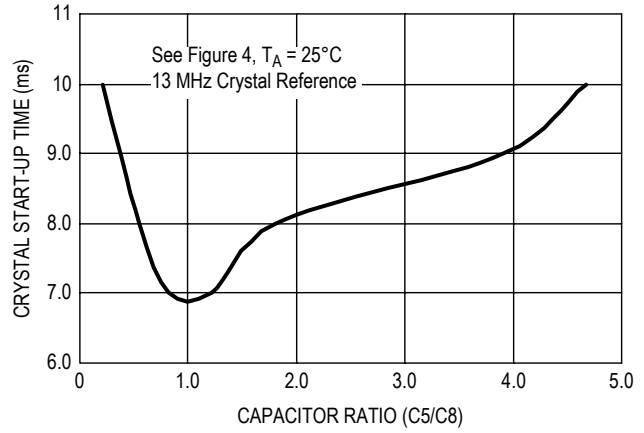


Figure 25. Crystal Start-up Time vs. Capacitor Ratio

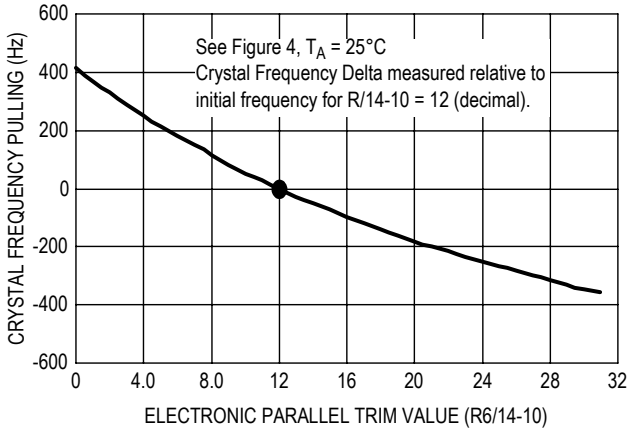


Figure 26. Crystal Frequency Pulling vs. Electronic Parallel Trim Value

6.6 Data Clock Operation

The data clock phase lock loop is responsible for providing a constant 24 MHz reference for use throughout the device. The MC72000 uses a simple integer-N synthesizer to derive a 24 MHz clock (CLK) from the reference frequency. This allows the MC72000 to adapt to external reference oscillator or crystal in the range of 12 to 26 MHz. The counter values must always be set to the appropriate values to generate this 24 MHz clock frequency. The general model for the phase lock loop (PLL) is shown in Figure 27.

For the circuit in Figure 92, the external low pass filter has a loop filter bandwidth (LBW) of 1.0 kHz. This proves to be adequate for any value of external reference frequency that is an integral multiple of 20 kHz. The external low pass filter requires one capacitor. More details about PLL loop filters can be obtained from *An Improved PLL Design Method Application Note* (document number AN1253/D).

The R-counter of the synthesizer (R6/9-0) is set to a value which will set the internal reference frequency f_{ref}Internal to 20 kHz; thus, R = f_{ref}Internal/20 kHz. The N-counter of the synthesizer (R7/10-0) is set to multiply f_{ref}Internal to 24 MHz; thus N = 24 MHz/f_{ref}Internal. For the case of a 13 MHz external reference, $R = 650_{10}$ and $N = 1200_{10}$.

For applications utilizing f_{ref}Internal > 20 MHz, the external low pass filter with a 1.0 kHz corner frequency is still usable. However, due to the R counter limitations, the R counter is programmed to generate the f_{ref}Internal to 40 kHz (recommended). In case of a 26 MHz external reference or other frequencies above 20 MHz, $R = 650_{10}$ and $N = 600_{10}$.

The N and R counters can only divide by integer values and the greatest common divider must be found to represent f_{ref}Internal and achieve CLK. Table 24 provides the appropriate values for various f_{ref}Internal. For applications requiring a faster data clock PLL response time, refer to the data clock electrical characteristics and *An Improved PLL Design Method Application Note* (document number AN1253/D) Additional data clock characteristic data is shown in Figure 28 and Figure 29.

Table 24. Data Clock R and N Counter Values for 20 kHz f_{ref}Internal with 1.0 kHz LBW

f_{ref}External (MHz)	f_{ref}Internal (kHz)	R Counter (Decimal)	N Counter (Decimal)	LBW (kHz)
12	20	600	1200	1.0
13	20	650	1200	1.0
14.4	20	720	1200	1.0
16.8	20	840	1200	1.0
19.22	20	961	1200	1.0
19.68	20	984	1200	1.0
19.88	20	994	1200	1.0
26	40	650	600	1.4

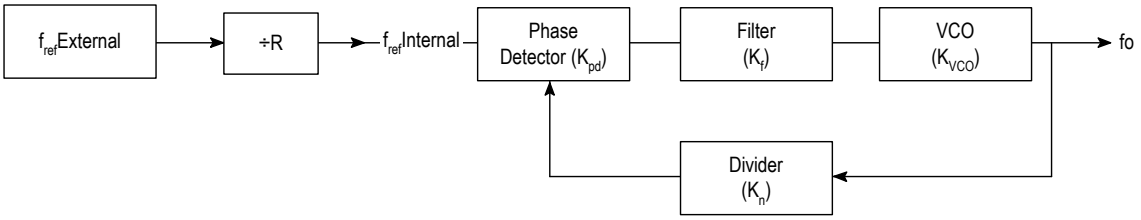


Figure 27. General Model for the PLL

Where:

K_{pd} = Phase Detector Gain Constant

K_f = Loop filter transfer function

K_{VCO} = VCO Gain Constant

K_n = Divide Ratio (1/N)

f_{ref}Internal = Input Frequency

fo = Output frequency

fo/N = Feedback frequency divided by N

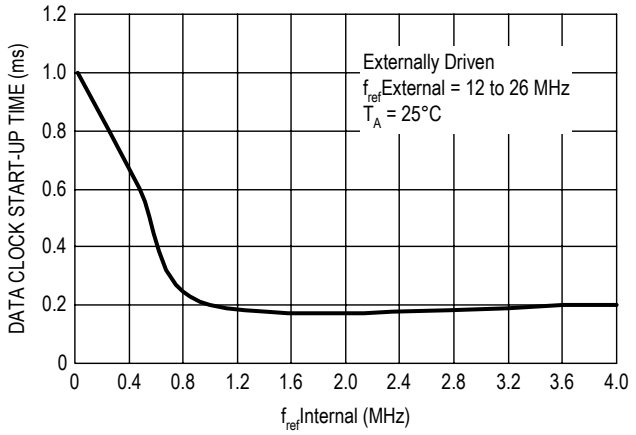


Figure 28. Data Clock Start-up Time vs. f_{ref} Internal

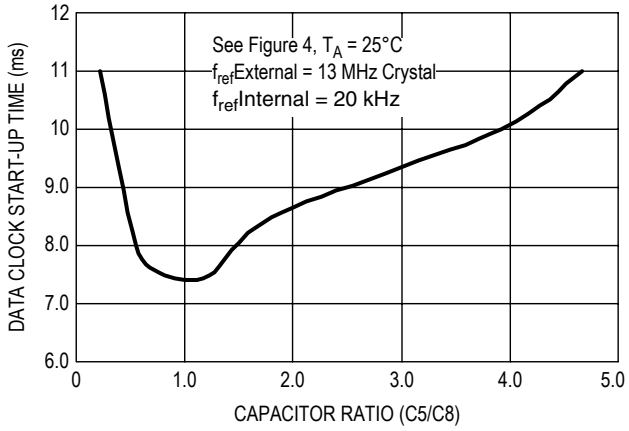


Figure 29. Data Clock Start-up Time vs. Capacitor Ratio for Crystal Reference

6.7 External Antenna Switch

An external antenna switch, shown in Figure 92, provides isolation between the PA output and the LNA input and subsequently enables transmit and receive cycles. The controls to the switch are GPO and EPAEN, pins 9 and 4 respectively, of the MC72000 device. When GPO is high, the switch is set to transmit mode. EPAEN serves as a complementary driver in this configuration. See Section 10, "Applications Information," for further information.

6.8 General Purpose Output (GPO) Pin

The MC72000 general purpose output (GPO) is located at Pin K5 of the device. Its output is programmed for general use by setting bit R2/8 in the Radio Register Map. The GPO can serve as a control line for an external antenna switch.

6.9 External Power Amplifier Enable (EPAEN) Pin

The External Power Amplifier Enable (EPAEN) output of MC72000 is located at Pin K2 of the device. EPAEN may be used in two applications. It may assist in Class 1 Operation by driving an external power amplifier; or it may serve as a complementary driver to a dual port antenna switch as shown in Figure 92. If EPAEN is not required for the desired application, it may be disabled by setting R11/6 to zero.

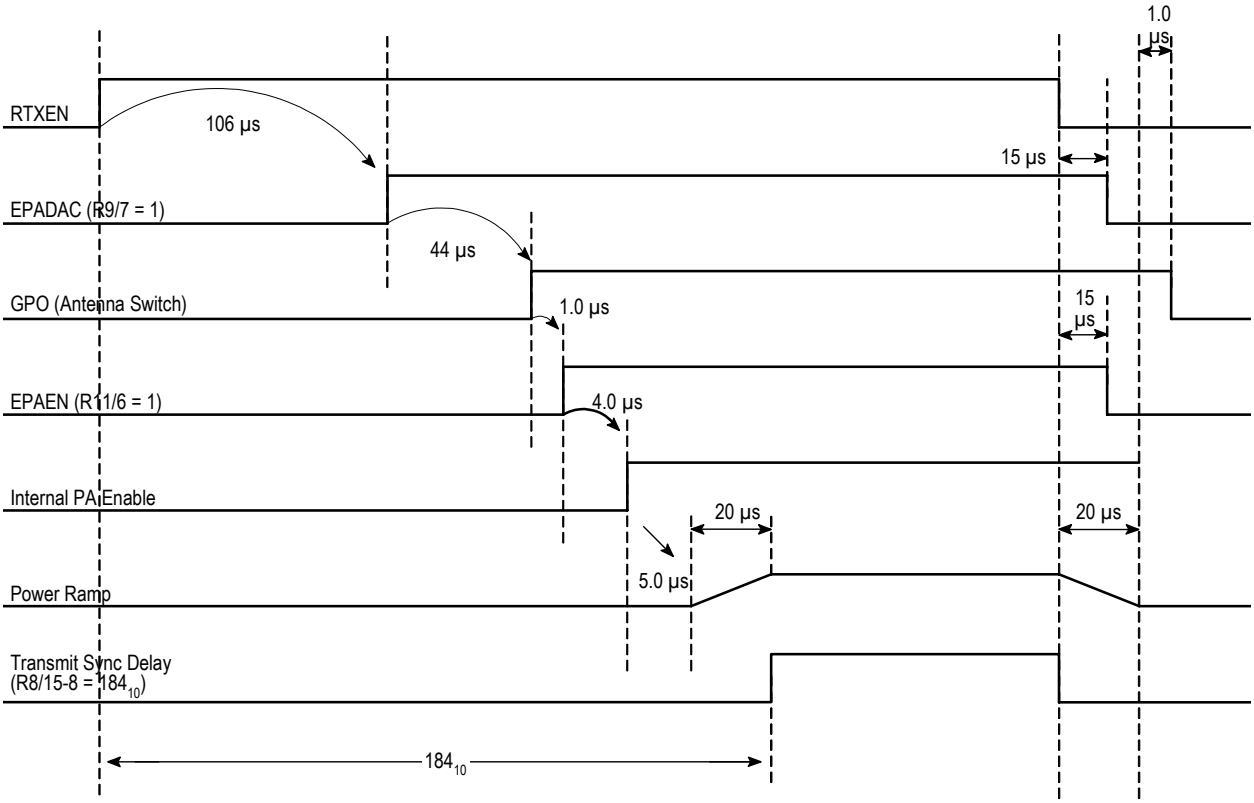


Figure 30. Ramp Generator (Transmit Cycle) Timing Diagram

7 Hardware Functional Description

These hardware blocks will be described in the following sections:

- Clock reset module (CRM)
- UART Interface
- SPI Interface
- SSI interface

7.1 Clock Reset Module (CRM)

The Clock Reset Module (CRM) is a dedicated module to handle all clock and reset functions in the MC72000. The CRM assures that different clock and reset signals are stable and synchronized before they are fed to the internal logic in the MC72000.

7.1.1 Features

The CRM has the following features:

- Controls system reset
- Sleep mode management
  - — Timer for recording sleep mode active period and initiating wake up

— Controlled recovery and clock restarts

- Watchdog (COP) surveillance
- Clock control and generation
- Software-initiated system reset

7.1.2 Modes of Operation

- Power Up

  After POR the CRM module will delay the release of the 32 kHz oscillator clock to the rest of the system until the oscillator has time to stabilize. After the ARM core begins operating, it will control the switch over to the REFCLK signal.

- Normal Operation

  The MC72000 system clock operates on the 12-32 MHz reference clock (REFCLK) from the radio.

- Sleep Operation

  During sleep mode, the high frequency reference clock from the radio will be turned off, and only the 32 kHz clock will be used to clock the vital parts of the CRM module. Sleep mode is initiated by setting the PDE bit in the Wake Up Control register. Sleep mode can be ended by either the internal wake up timer or one of the four external wake up interrupts.

7.1.2.1 External Clock Control Register

The CRM module generates two derivatives of REFCLK. The frequencies of these clocks are programmable in the range of ~500 kHz to REFCLK. The resulting clocks are named CLK0 (fractional divided), and CLK1 (integer divided) on the output pads. These clocks can be used to feed external devices such as a USB, CODEC, or whatever the final system application needs. The duty cycle of CLK0 and CLK1 cannot be expected to be 50/50 because of the nature of REFCLK from the RF IC as well as additional changes introduced by the clock divider circuitry. Any external device using CLK0 or CLK1 should be held in reset whenever the frequency of these clocks is changed because the periods may be unstable for some time immediately after the change request. Because the external clocks operate independently, there is no implied phase relationship between CLK0 and CLK1 if their divisors are the same or integer multiples. These clocks will be stopped in sleep mode because they are derivatives of REFCLK which is also stopped in sleep mode.

CLK1_DIV[3:0] — Clock1 Divisor

The CLK1_CNTRL register controls the integer division of the REFCLK to generate the CLK1 output signal. The CLK1 output will be low when CLK1_DIV is disabled.

Table 25. CLK1_DIV Values

Value	Divisor	@32 Mhz refclk	Duty Cycle
000	CLK1 Disabled (Low)		NA
001	divide 1	32 MHz	REFCLK dependent
010	divide 2	16 MHz	50/50
011	divide 4	8 MHz	50/50
100	divide 8	4 MHz	50/50
101	divide 16	2 MHz	50/50
110	divide 32	1 MHz	50/50
111	divide 64	500 kHz	50/50

7.2 Universal Asynchronous Receiver/Transmitter (UART)

7.2.1 Overview

Th UART transmits and receives a character length of eight bits. For transmission, data is passed to a transmitter FIFO (first in, first out), of 32 bytes/characters in depth, from the peripheral data bus. This data is passed to the shift register and shifted serially out on the TXD pin. For reception, data is received serially from the RXD pin and stored in a receiver FIFO of 32 bytes/characters in depth. The received data is retrieved from the receiver FIFO on the peripheral data bus. The receiver and transmitter FIFOs contain a maskable interrupt that can be configured to interrupt when it reaches a certain level.

The UART-generated baud rate is based upon a configurable divisor and the input clock. It can be configured to send one or two stop bits as well as odd, even, or no parity. The receiver detects framing errors, start bit errors, breaks, parity errors, and overrun errors.

The fractional divider is set up by writing an INCrement and MODulo value to registers. It is important that the UART is disabled (RXE and TXE equal 0) before writing new values to the INC/MOD registers. After writing to the registers, the receiver and/or transmitter can be enabled (RXE and TXE equal 1).

NOTE:

When the UART is disabled (RXE and TXE equal 0), both the RX and the TX buffers are flushed, and the status register is updated.

For test purposes, the RXD and TXD pins can be connected internally to each other for loop-back test.

7.2.2 Features

The UART provides the following features:

- 8 data bits
- 1 or 2 stop bits
- Programmable parity (even, odd, and none)
- Four-wire serial interface (RXD, TXD, RTS, and CTS)
- Hardware flow control support for RTS and CTS signals
- Sense programmable RTS/CTS pins (high true/low true)
- Status flags for various flow control and FIFO states
- Voting logic for improved noise immunity (16X/8X oversampling)
- Two maskable interrupts (IPI_RXRDY, IPI_TXRDY)
- Time-out interrupt timer, which times out after eight non-present characters (interrupt on RXRDY)
- 32-byte receive FIFO and 32-byte transmit FIFO
- Receiver and transmitter enable/disable
- Low-power modes
- Fractional divider to generate any baud rate between 1,200 baud and 1,843.2 kbaud
- Software reset

7.2.3 Fractional Divider

The high-speed UART is clocked with the IP bus clock (in the MC72000 typically 24 MHz). This high frequency clock plus an internal fractional divider enables a wide range of frequencies that is calculated using the following equations:

In 16 times oversampling mode (xTIM=0 in the UART control register), the following equation is used to calculate the baud rate.

$$\text{audrateX16} = \text{ipsclk} \times \left[\frac{\text{INC} + 1}{\text{MOD}}\right.$$

$$\text{baudrate} = \frac{\text{baudrateX16}}{16}$$

In 8 times oversampling mode (xTIM=1 in the UART control register), the following equation is used to calculate the baud rate.

$$\text{audrateX8} = \text{ipsclk} \times \left[\frac{\text{INC} + 1}{\text{MOD}}\right.$$

$$\text{baudrate} = \frac{\text{baudrateX8}}{8}$$

The internal baud rate generator is shown in Figure 31.

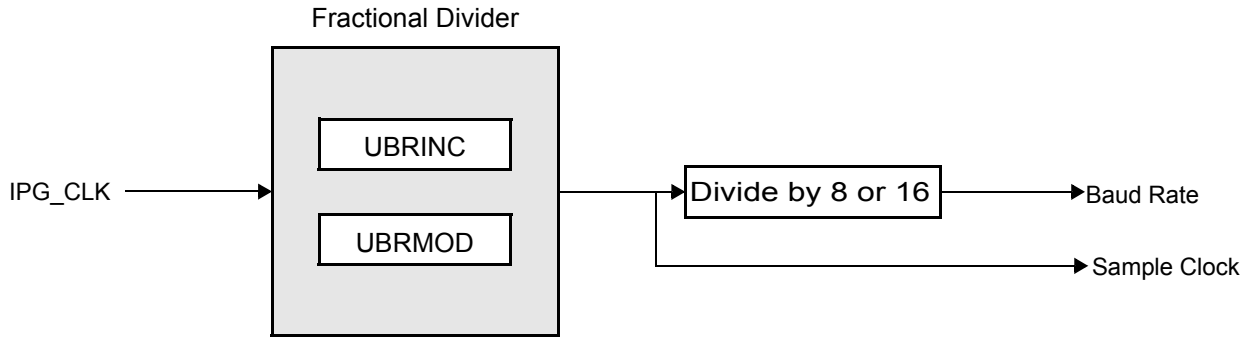


Figure 31. UART Baud Rate Generator

Values for INC and MOD that yield standard baud rates at an input clock of 24 MHz/12 MHz are shown in Table 26.

Table 26. Standard Baud Rates[1]

Baud Rate	IPSCLK = 12 Mhz			IPSCLK = 24 Mhz		
	MOD	INC	FREQ	MOD	INC	FREQ
1,200	10,000	15	1,200	10,000	7	1,200
2,400	10,000	31	2,400	10,000	15	2,400
4,800	10,000	63	4,800	10,000	31	4,800
9,600	10,000	127	9,600	10,000	63	9,600
19,200	10,000	255	19,200	10,000	127	19,200
28,800	10,000	383	28,800	10,000	191	28,800
38,400	10,000	511	38,400	10,000	255	38,400
57,600	10,000	767	57,600	10,000	383	57,600
115,200	10,000	1535	115,200	10,000	767	115,200
230,400	10,000	3071	230,400	10,000	1,535	230,400
460,800	10,000	6143	460,800	10,000	3,071	460,800
921,600	10,000	6143[2]	921,600	10,000	6,143	921600
1,843,200	10,000	—	—	14000	8601[3]	1843285.7

1. Fractional divider values are shown for the 16 times oversampling mode.
2. At this baud rate, only 8 x oversampling is possible because (12 MHz/921600) < 16.
3. At this baud rate, only 8 x oversampling is possible because (24 MHz/1843200) < 16.

7.2.4 General UART Definitions

These general UART definitions will help in understanding the following sections.

- Start Bit — A start bit is a bit of logic zero which indicates the beginning of a data frame. A start bit must begin with a one to zero transition and is preceded by at least one bit time of logic one.
- Stop Bit — A stop bit is a bit of logic one which indicates the end of a data frame. A stop bit follows the data and any parity bit. They mark the end of a unit of transmission (normally a byte or character).
- Break — A frame or longer with RX/TX held low at logic zero. This kind of frame is generally sent to signal the end of a message or the beginning of a new message.
- Frame — A frame consists of a start bit followed by a specified number of data or information bits terminated by a stop bit. The number of data or information bits depends on the format specified and must agree between the transmitting device and the receiving device. The most common frame format is one start bit followed by eight data bits (LSB first) terminated by one stop bit.
- Framing Error — An error condition in which the stop bit of the received frame was missing. A framing error results when the frame boundaries in the received bit stream are not synchronized with the receiver bit counter. Framing errors are not always detected: if a data bit in the expected stop bit time happens to be a logic one, the framing error may go undetected. A framing error is always present on the receiver side, when the transmitter is sending breaks. However, if the UART is set up to expect two stop bits, and only the first stop bit is received, then this is not a framing error.
- Parity Error — An error condition in which the calculated parity of the received data bits in the frame is different from the parity bit received on the RXD line. Parity error is only calculated after an entire frame is received.An additional stop bit and parity bit may also be included.

- Overrun Error — An error condition in which the latest character received is ignored to prevent overwriting an already existing character in the UART Receiver Buffer. An overrun error indicates that the software reading the buffer is not keeping up with the actual reception of characters on the RXD line.

NOTE:
The above signals assume control (FCe) = 0 (enabled and control) and (FCp) = 0 (active low RTS/CTS signals).

Figure 32. General UART Connection

7.2.4.1 $\overline{\text{RTS}}$ — Request to Send

This input is used to control the transmitter. By asserting $\overline{\text{RTS}}$, the far-end device signals to the UART that it is ready to receive. Normally, the transmitter waits until this signal is active (low) before a character is transmitted. If the Flow Control Enable (FCE) bit is disabled, the transmitter sends a character whenever a character is ready to transmit. When flow control is enabled, the $\overline{\text{RTS}}$ signal can be configured to either stop a transmission upon assertion or to enable a transmission upon deassertion.

7.2.4.2 $\overline{\text{CTS}}$ — Clear to Send

This output is used to control the transmitter of the remote device. Normally, the receiver indicates that it is ready to receive data by asserting this pin (low). When enabled, this signal is controlled by the watermarks in the RXFIFO.

7.2.4.3 Transmitter

The transmitter accepts a parallel character and transmits it serially. When the transmitter is enabled, the start, stop, and parity (if enabled) bits are added to the character. $\overline{\text{RTS}}$ is used to flow-control the serial data if desired. If $\overline{\text{RTS}}$ is negated (high), the transmitter finishes sending the character in progress (if any) then stops and waits for $\overline{\text{RTS}}$ to again become asserted (low).

7.2.4.4 Receiver

The receiver accepts a serial data stream and converts it into a parallel character.When enabled, it searches for a start bit, qualifies it, then samples the succeeding data bits at the bit-center. Jitter tolerance and noise immunity are provided by sampling at a 16x rate and using voting techniques to clean up the samples. Once the start bit has been found, the data bits, parity bit (if enabled), and stop bits are shifted in. If parity is enabled, it is checked and its status is reported in the USTAT register. Similarly, frame errors and breaks are checked and reported. If the CTS_LEVEL is set to zero, the receiver ready interrupt flag (RXRDY) will

be asserted as well and an interrupt is posted (if MRXR = 0). The RXRDY interrupt flag is cleared when the RXFIFO empties below the programmed trigger level.

7.2.4.5 Receiving a Break Condition

Receiving a break condition is detecting all zeros including a zero during the stop bit bit time. When a break condition is detected by the receiver, the UART will interpret this as a framing error.

7.2.4.6 Voting Logic

The vote logic block provides jitter tolerance and noise immunity by sampling with respect to the peripheral clock and using voting techniques to clean up the samples. The voting is implemented by sampling the incoming signal constantly on the rising edge of clock. The receiver is provided with the majority vote value, which is two out of the three samples.

Table 27. Majority Vote Results

Samples	Vote
000	0
101	1
001	0
111	1

The vote logic captures a sample on every rising edge of the clock, but the receiver takes its value in the middle of the sample frame using 16x oversampling. The idle character may be longer or shorter than 16 counts, but the receiver looks for a 1 to 0 transition. Then it starts to count the start bit but does not capture it in the FIFO. The start bit is validated upon receiving zeros for seven consecutive bit times following the 1 to 0 transition. Once the counter reaches F hex, it starts counting the next bit and captures it in the middle of the sampling frame. All data bits are captured in the same manner. Once the stop bit is detected, the receiver shift register data is parallel shifted to the receiver FIFO.

7.2.5 UART Registers

The following paragraphs provide detailed descriptions of UART registers.

7.2.5.1 UART Control Register (UCON)

UCON is used to specify transmission parameters, such as flow control, stop bits, parity, and so on.

UCONBase + $000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TST	MRXR	MTXR	FCE	FCP	XTIM	SEL	0	TX_OEN_B	CONTX	SB	ST2	EP	PEN	RXE	TXE
RST	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0

= writes have no effect and terminate without transfer error exception

TST—Test Loop-Back:

This bit sets whether the MC72000 is placed into test loop-back mode where the TXD and RXD signals are connected.

1 = Test (loop-back) mode
0 = Normal operation

MRXR—Mask RXRDY Interrupt

This active low bit enables an interrupt when the receiver has data in the RXFIFO above watermark, or there is data in the FIFO and the UART is idle for more than 8 frames. The fill level in the RXFIFO at which an interrupt is generated is controlled by the RXLEVEL bits. While negated, this interrupt is disabled (masked).

1 = RXRDY interrupt masked
0 = RXRDY interrupt enabled

MTXR—Mask TXRDY Interrupt

This active low bit enables an interrupt when the transmitter has data in the TXFIFO below the watermark or is completely empty. The fill level in the TXFIFO at which an interrupt is generated is controlled by the TXLEVEL bits. While negated, this interrupt is disabled (masked).

1 = TXRDY interrupt masked
0 = TXRDY interrupt enabled

FCE—Flow Control Enable

This bit controls whether the MC72000 will use flow control. When flow control is disabled, the UART will ignore the $\overline{\text{RTS}}$ input and assert the $\overline{\text{CTS}}$ pin low.

1 = Enabled
0 = Disabled

FCP—Flow Control

When flow control is used, this bit indicates the polarity of the RTS/CTS bits.

1 = Assert RTS to stop transmission
0 = Deassert RTS to enable transmission

xTIM—Times of Oversampling

The xTIM bit indicates how much oversampling will be used.

1 = 8 times oversampling
0 = 16 times oversampling

SEL—GPIO Input Select

The SEL bit indicates which of the MC72000 GPIO pins will be used as the RTS/RXD output signals from the UART.

1 = RTS_2/RXD_2
0 = RTS_1/RXD_1

TX_OEN_B— Tri-state enable for TXD/CTS

The bit indicates:

1 = Tri-state TXD and CTS output pads
0 = Enable TXD and CTS output pads

CONTX—Continuous TX (Test Mode)

Only used in test mode, when this bit is enabled, the UART will continuously transmit characters.

1 = Enable
0 = Disable

SB—Set Break

When set, TXD is pulled low to signal a break.

1 = Set break
0 = No break

ST2—Stop Bits

This bit controls the number of stop bits transmitted after a character. While HIGH, two stop bits are sent. While LOW, one stop bit is sent. This bit has no effect on the receiver which expects one or more stop bits.

1 = Two stop bits
0 = One stop bit

EP—Even Parity

This bit controls the sense of the parity generator and checker. While LOW, odd parity is generated and expected. While HIGH, even parity is generated and expected. This bit has no function if PEN is low.

1 = Even parity
0 = Odd parity

PEN—Parity Enable

This active HIGH bit controls the parity generator in the transmitter and parity checker in the receiver. While asserted, they are enabled. While negated, they are disabled.

1 = Enable parity
0 = Disable parity

RXE—RX Enable

This active HIGH bit enables the receiver. When the receiver is enabled, if the RXD line is already low, the receiver does not recognize break characters, since it requires a valid one-to-zero transition before it can accept any character. If disabled during a reception, the receiver will complete the current reception then disable.

1 = Receiver enabled
0 = Receiver disabled

TXE—TX Enable

This active HIGH bit enables the transmitter. If disabled during a transmission, the UART will immediately return TXD to idle (1). The transmitter FIFO cannot be written to when this bit is cleared.

1 = Transmitter enabled
0 = Transmitter disabled

NOTE:

The SEL bit is used to select between using the RTS_2/RXD_2 and RTS_1/RXD_1 ports on the UART module. In the MC72000, these ports are connected to the GPIO ports B and C. RTS_2/RXD_2 are connected as alternate functions to GPIO port B (GPIO_B11 and GPIO_B12) and are called UART-RTS/UART-RXD. GPIO_B11 and GPIO_B12 must be set to alternate function 2 mode in order to use RTS_2/RXD_2. RTS_1/RXD_1 are connected to pins RTS_/RXD on GPIO port C and no configuration is necessary to use these pins.

7.2.5.2 UART Status Register (USTAT)

USTAT indicates interrupts and any errors that have been detected during transmission, such as FIFO buffer overflow or underflow, parity error, and frame, start, or stop bit error.

NOTE:

Bits[7:6] are cleared when the respective condition allows it. Status bits[5:0] are cleared when the register is read.

USTATBase + $004

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	TXRDY	RXRDY	RUE	ROE	TOE	FE	PE	SE
W																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= writes have no effect and terminate without transfer error exception

TXRdy—Transmitter is Causing an Interrupt

1 = Interrupt pending
0 = No interrupt

RXRDY—Receiver is Causing an Interrupt

1 = Interrupt pending
0 = No interrupt

RUE—RX FIFO Underrun Error

This read-only bit indicates, while HIGH, that the RXFIFO underrun error occurred. This occurs when software reads more from the FIFO than is actually present. This bit is updated and valid for each received character. This bit is set for the last character written to the FIFO indicating that all characters following this character will be ignored if a write is not performed by software. The RUE bit is cleared by UART reset or by reading the USTAT register.

1 = Error occurred
0 = No error

ROE—RX FIFO Overrun Error

This read-only bit indicates, while HIGH, that the RXFIFO ignored data to prevent overwriting the data in the FIFO. Under normal circumstances, this bit should never be set. It indicates that the user's software is not keeping up with the incoming data rate. This bit is updated and valid for each received character. This bit is set for the last character written to the FIFO indicating that all characters following this character will be ignored if a read is not performed by software. The ROE bit is cleared by UART reset or by reading the USTAT register.

1 = Error occurred
0 = No error

TOE—TX FIFO Overrun Error

This flag bit is set when the UDATA register is filled and ready to transfer to the TXFIFO register and the register is already full. This error occurs when the software writes more data than is room for in the FIFO. The transmit data is not transferred in this case. A transmit overrun error does not cause any interrupts. The TOE bit is cleared by UART reset or by reading the USTAT register.

1 = Error occurred
0 = No error

FE—Frame/Stop Bit Error

This read-only bit indicates, while HIGH, that the current character had a framing error (missing stop bit or break condition). The data is possibly corrupted. This bit is updated for each character read from the FIFO. The FE bit is cleared by UART reset or by reading the USTAT register.

1 = Framing error occurred
0 = No framing error

PE—Parity Error

This read-only bit indicates, while HIGH, that the current character was detected with a parity error. The data is possibly corrupted. This bit is updated for each character read from the FIFO. While parity is disabled, this bit always reads zero. The PE bit is cleared by UART reset or by reading the USTAT register.

1 = Parity error occurred
0 = No parity error

SE—Start Bit Error

This read-only bit indicates, while HIGH, that the current character had a framing error (missing start bit.) The data is possibly corrupted. This can occur when a start bit (RXD = 0) is found, but is not verified at the center of the bit (for example, glitch). This bit is updated for each character read from the FIFO. The SE bit is cleared by UART reset or by reading the USTAT register.

1 = Start bit error occurred
0 = No start bit error

7.2.5.3 UART Data Register (UDATA)

UDATA fills the UART transmit FIFO buffer with bytes that are to be transmitted, and to read the received bytes from the UART receive FIFO buffer.

It is possible to read/write 1 byte per access.

UDATABase + $008

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	RXDATA							
W									TXDATA							
RST	0	0	0	0	0	0	0	0	Undefined							

= writes have no effect and terminate without transfer error exception

RXDATA[7:0]—Received Byte

This bit field contains the 8-bit data that has been received.

TXDATA[7:0]—Byte To Transmit

This bit field contains the 8-bit data to be transmitted.

7.2.5.4 UART Buffer Control Registers

The UART buffers use threshold values to generate interrupts. These thresholds can be used to specify that an interrupt should be generated before the transmit FIFO has become completely empty, or some time

before the receive FIFO has been completely filled. These early warnings allow relaxed interrupt response times.

7.2.5.4.1 UART RXBUFFER Control Register (URXCON)

The RXLEVEL register is used to set the threshold for the interrupt that is generated when the receive buffer is full. The RXFULLCNT register contains the number of bytes that are currently buffered in the receive FIFO.

URXCONBase + $00C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	RXFULLCNT					
W											RXLEVEL					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= writes have no effect and terminate without transfer error exception

RXFULLCNT[5:0]—Receive buffer full level

This value indicates the number of bytes currently buffered in the receive FIFO buffer. The number of bytes is between 0 (empty) and 32 (full) bytes.

RXLEVEL[5:0]—Receive buffer level

When the number of bytes in the receive FIFO exceeds the value specified by RXLEVEL, an interrupt is generated.

7.2.5.4.2 UART TXBUFFER Control Register (UTXCON)

UTXCON sets the threshold for the interrupt that is generated when the transmit buffer becomes empty. The TXEMPTYCNT register contains the number of bytes that can still be written to the UART transmit FIFO. Data can be written to the transmit buffer while this number is non-zero.

UTXCON Base + $010

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	TXEMPTYCNT					
W											TXLEVEL					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= writes have no effect and terminate without transfer error exception

TXEMPTYCNT[7:0]—Transmit Buffer Empty Level

This value indicates the number of empty bytes currently available in the transmit FIFO buffer. The number of free bytes is between 0 (full) and 32 (empty) bytes.

TXLEVEL[7:0]—Transmit Buffer Level

When the number of free bytes in the transmit FIFO buffer exceeds the value specified by TXLEVEL, an interrupt is generated.

7.2.5.4.3 UART CTS Level Control Register (UCTS)

UCTS sets the threshold for the CTS control flow signal. If the remote UART continues to send limited amounts of data after detecting the deasserted CTS signal, the local receive buffer can handle the additional data if CTS_LEVEL is set to a suitable value.

UCTSBase + $014

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
RST																

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	CTS_LEVEL							
W									CTS_LEVEL							
RST									0	0	0	0	0	0	0	0

= writes have no effect and terminate without transfer error exception

CTS_LEVEL[7:0]—CTS Buffer Level

When the number of bytes in the receiver (RX) FIFO exceeds this value, the CTS signal is deasserted.

7.2.5.5 UART Baud Rate Divider Register (UBR)

The fractional divider registers are used to select the receive and transmit baud rate. The following sections describe the fractional divider registers.

The FRACDIV_DIV register is used to select the divisor for the fractional division divider. See Section 7.2.3, “Fractional Divider,” for an explanation of the value to be written to the register.

The FRACDIV_INC register is used to select the modulus value for the fractional division divider. See Section 7.2.3, “Fractional Divider,” for an explanation of the value to be written to the register.

UBR Base + $018

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	UBRINC															
W	UBRINC															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	UBRMOD															
W	UBRMOD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= writes have no effect and terminate without transfer error exception

UBRINC — INC Value

This value is used to select the baud rate. See Section 7.2.3, “Fractional Divider,” for more information.

UBRMOD — MOD Value

This value is used to select the baud rate. See Section 7.2.3, “Fractional Divider,” for more information.

7.2.6 FIFO Operation

The operation of the transmit and receive FIFOs is shown in Figure 33.

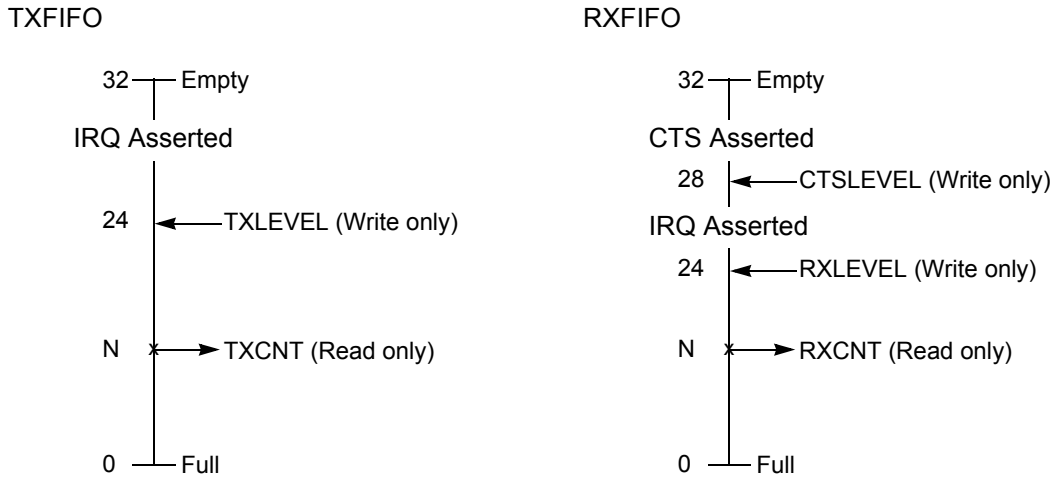


Figure 33. RX and TX FIFO-Related Levels

7.2.7 Flow Control

The operation of the transmit and receive Flow Control is shown in Figure 34.

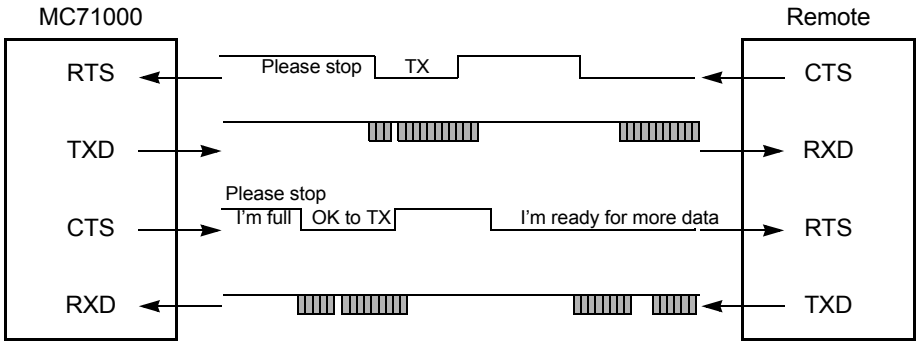
NOTE:

Ready To Send (RTS) means that the MC72000 is allowed to send because the remote unit is ready.

Clear To Send (CTS) means that the MC72000 is ready to accept new data, so the remote unit can transmit when it has data.

The polarity of RTS/CTS can be changed by changing the control [FCP] bit.

When the control[FCE]=0, the flow control is disabled. This causes the UART to ignore the RTS input and asserting the CTS pin (that is, the CTS pin is 0 when control[FCP]=0).



NOTE:
The above signals assume control (FCe) = 0 (enabled and control) and (FCp) = 0 (active low RTS/CTS signals).

Figure 34. Flow Control

7.3 Configurable Serial Peripheral Interface (CSPI)

The CSPI is a master/slave configurable serial peripheral interface module which allows full-duplex, synchronous, serial communications with other peripheral devices. The CSPI is equipped with an 8 x 16 RXFIFO and an 8 x 16 TXFIFO. The CSPI incorporates the DATAREADY_B and SS_B control signals and enables fast data communication with a fewer number of software interrupts.

7.3.1 Features

The CSPI has the following features:

- Full-duplex operation
- Master and slave modes
- Separate 8 x 16 transmit and receive FIFO registers
- Eight master mode frequencies
  - — Maximum frequency = bus frequency ÷ 4
  - — Minimum frequency = bus frequency ÷ 512
- Slave mode frequencies
  - — Maximum frequency = less than bus frequency ÷ 4
  - — Minimum frequency = 0
- Selectable transmit and receive word lengths from 1 to 16 bits
- Serial clock with programmable polarity and phase
- Interrupts
  - — Receiver full (programmable level)
  - — Transmitter empty (programmable level)
  - — Overflow error, RXFIFO, and bit count

7.3.2 Modes of Operation

- Master mode

— Transfer control
— Immediate
— Data ready input signal
— Period control (baud rate clock or 32 kHz clock)

- Slave mode

7.3.3 Block Diagram

Figure 35 shows the CSPI block diagram.

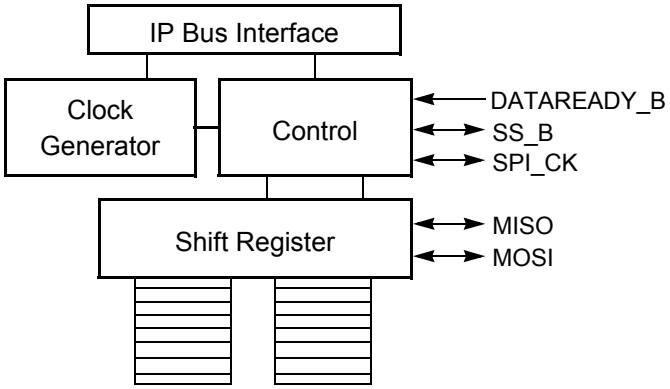


Figure 35. CSPI Block Diagram

7.3.4 Signal Description

Table 28 shows the signals used to control the serial peripheral interface master.

Table 28. Serial Peripheral Interface Master Control Signals

Signal	Description	Function
MOSI	Master out slave in	This bidirectional signal is the TXD output signal from the data shift register in master mode. In slave mode, MOSI is the RXD input to the data shift register.
MISO	Master in slave out	This bidirectional signal is the RXD input signal to the data shift register in master mode. In slave mode, MISO is the TXD output from the data shift register.
SPI_CK	CSPI clock	This bidirectional signal is the CSPI clock output in master mode. In slave mode, SPI_CK is an input clock signal to the CSPI.
SS_B	Slave select	This bidirectional signal is an output in master mode and an input in slave mode.
DATAREADY_B	SPI ready	This input signal is used only in master mode. It will edge or level trigger a CSPI burst if used.

7.3.5 Detailed Signal Descriptions

The following section provides detailed signal descriptions.

7.3.5.1 SPI_CK — SPI CLOCK

The serial clock synchronizes data transmission between master and slave devices. In a master MCU, the SPI_CK pin is the clock output. In a slave MCU, the SPI_CK pin is the clock input. In full duplex operation, the master and slave CSPIs exchange data in BITCOUNT serial clock cycles.

When enabled in the GPIO function select register, the CSPI controls data direction of the SPI_CK pin regardless of the state of the GPIO data direction register of the shared I/O port.

7.3.5.2 MISO — SPI Master In/Slave Out

MISO is one of the two CSPI module pins that transmits serial data. In full duplex operation, the MISO pin of the master CSPI module is connected to the MISO pin of the slave SPI module. The master CSPI simultaneously receives data on its MISO pin and transmits data from its MOSI pin.

Slave output data on the MISO pin is enabled only when the SPI is configured as a slave. The CSPI is configured as a slave when its MODE bit is logic zero and its SS_B pin is at logic zero. To support a multiple-slave system, a logic one on the SS_B pin puts the MISO pin in a high-impedance state.

When enabled in the GPIO function select register the CSPI controls data direction of the MISO pin regardless of the state of the GPIO data direction register of the shared I/O port.

7.3.5.3 MOSI — SPI Master Out/Slave In

MOSI is one of the two CSPI module pins that transmit serial data. In full duplex operation, the MOSI pin of the master CSPI module is connected to the MOSI pin of the slave CSPI module. The master CSPI simultaneously transmits data from its MOSI pin and receives data on its MISO pin.

When enabled in the GPIO function select register the CSPI controls data direction of the MOSI pin regardless of the state of the GPIO data direction register of the shared I/O port.

7.3.5.4 SS_B — SPI Slave Select

The SS_B pin has various functions depending on the current state of the CSPI CONTROLREG. For a CSPI configured as a slave, the SS_B pin is used to select a slave. When a CSPI is configured as a slave, the SS_B pin is always configured as an input. It cannot be used as a general purpose I/O.

When a CSPI is configured as a master, for PHA = 1, the SS_B is used to define the start of a new word transmission. However, it can remain low between word transmissions for the PHA = 0 format.

When enabled in the GPIO function select register, the CSPI controls data direction of the SS_B pin regardless of the state of the GPIO data direction register of the shared I/O port.

7.3.5.5 DATAREADY_B — SPI Data Ready

The DATAREADY_B pin is used in master mode to allow a slave device to signal the master that the slave is ready to deliver some new data to the master.

When enabled in the GPIO function select register, the CSPI controls data direction of the DATAREADY_B pin regardless of the state of the GPIO data direction register of the shared I/O port.

7.3.6 Memory Map and Registers

Table 29 shows the CSPI memory map. There are 8 user programmable registers which are 16 bits. All registers are aligned to the 32-bit word address width and always return zeros in the upper 16 bits whenever read. The AIPI can be set to enable the CRM for either 32- or 16- bit transfers. All registers are byte and halfword accessible. The base address of the CSPI0 and CSPI1 modules on the MC72000 is 32'h8000_8000 and 32'h8000_9000.

Table 29. CSPI Memory Map

Address	Use	Access
Base + 0x00	RX Data Register (RXDATAREG)	R
Base + 0x04	TX Data Register (TXDATAREG)	R/W
Base + 0x08	Control Register (CONTROLREG)	R/W
Base + 0x0C	Interrupt Control/Status Register (INTREG)	R/W
Base + 0x10	CSPI Test Register (TESTREG)	R/W
Base + 0x14	CSPI Sample Period Control Register (PERIODREG)	R/W
Base + 0x18	Reserved	N/A
Base + 0x1c	CSPI Soft Reset Register (RESETREG)	R/W

The following sections provide detailed descriptions of each of the CSPI registers. All readable registers will return 0x0 after reset unless otherwise specifically stated. All reserved bits are read as zero and should be written with zero for future compatibility.

7.3.7 Register Descriptions

7.3.7.1 RX Data Register (RXDATAREG)

Register address: BASE + 0x00

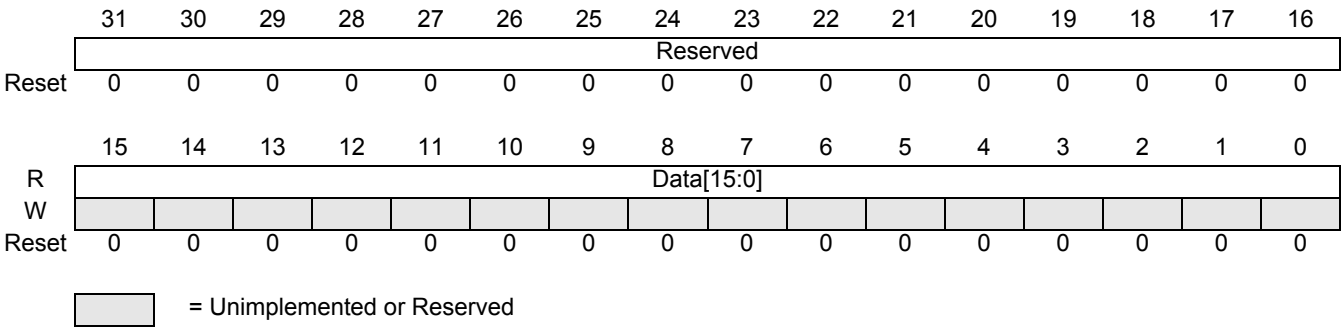


Figure 36. RX Data Register (RXDATAREG)

RXDATAREG is 32-bit read-only register. The lower 16 bits hold the top of the 8 x 16 RXFIFO received from an external CSPI device during a data transaction. The upper 16 bits are reserved bits and are always read as 0. Bits beyond the current setting of the BITCOUNT register are invalid and should be masked by the user software.

DATA[15:0] — CSPI Data in the RXFIFO

DATA has no meaning if the RR bit in the interrupt control/status register is clear.

7.3.7.2 TX Data Register (TXDATAREG)

Register address: Base + 0x04

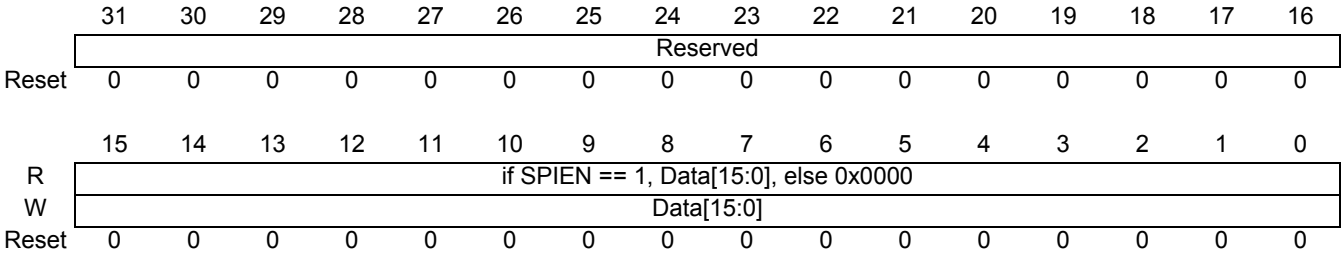


Figure 37. TX Data Register (TXDATAREG)

TXDATAREG is a 32-bit write-only data register. The lower 16 bits is the top of the 8 x 16 TXFIFO. Writing to TXFIFO is permitted as long as it is not full, even though the XCH bit is set, that is, the user could write to TXFIFO during CSPI data exchange process. Writes to this register are ignored while the SPIEN bit is clear. The upper 16 bits are reserved bits and are always read as 0.

DATA[15:0] — CSPI data to be loaded to the 8x16 TXFIFO

In master or slave mode, a maximum of eight data words are loaded. Data writes to this register can be either 8-bit or 16-bit size. The number of bits to be shifted out of the 16-bit transmit FIFO element is determined by the BIT COUNT value in the control register. The unused MSBs are don't cares. For example, to transfer 10-bit data, a 16-bit word is written to this register and the six MSBs are don't cared and are not shifted out. In slave mode, if no data is loaded in the TXFIFO, 0s are shifted out on the TXD signal.

7.3.7.3 Control Register (CONTROLREG)

Register address: Base + 0x08

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DRCTL[2:0]			SPIRDY[1:0]		MODE	SPIEN	0 XCH	SSPOL	SSCTL	PHA	POL	BITCOUNT[3:0]			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 38. Control Register (CONTROLREG)

CONTROLREG is a 32-bit register. The high 16 bits are reserved bits and are always read as 0. The control registers, DRCTL, SPIRDY, MODE, SSPOL, SSCTL, PHA, POL, and BITCOUNT should not be changed when SPIEN = 1 to ensure that the internal counters and control logic are properly reset.

DRCTL[2:0]—Data Rate Control

This bit field selects the bit rate of the SCLK based on the division of the CPU clock.Table 30 shows the DRCTL[2:0] bit rate encoding.

Table 30. DRCTL[2:0] Bit Rate Encoding

DRCTL[2:0]	Function
000	Divide by 4
001	Divide by 8
010	Divide by 16
011	Divide by 32
100	Divide by 64
101	Divide by 128
110	Divide by 256
111	Divide by 512

SPIRDY[1:0]—DATAREADY_B Control

In master mode, these two bits select the wave form of the DATAREADY_B input signal. In slave mode they are don't care. Table 31 shows the SPIRDY[1:0] encoding.

Table 31. SPIRDY Control Encoding

SPIRDY[1:0]	Function
00	Don't care DATAREADY_B
01	Falling edge trigger input
10	Active low level trigger input
11	Reserved

MODE—CSPI Mode Select

This bit selects the CSPI mode.

1 = CSPI is master mode
0 = CSPI is slave mode

SPIEN — CSPI Module Enable

This bit enables the serial peripheral interface. This bit must be asserted before an exchange is initiated. Writing a 0 to this bit clears the RX and TX FIFO data and control registers along with the internal counters and state machine. Changing any of the other CONTROLREG bits, except XCH, when SPIEN is set is not allowed and may cause the CSPI to enter an invalid state.

1 = The serial peripheral interface is enabled
0 = The serial peripheral interface is disabled

XCH—Exchange

In master mode, writing a 1 to this bit triggers a data exchange. This bit remains set while either the exchange is in progress, or the CSPI is waiting for an active DATAREADY_B input when SPIRDY is enabled. This bit is cleared automatically when all data in the TXFIFO and shift register is shifted out. In slave mode, this bit must be clear.

1 = Initiates exchange (write) or busy (read)
0 = Idle

SSPOL — SS_B Polarity Select

This bit selects the polarity of SS_B signal in both master and slave mode.

1 = Active high
0 = Active low

SSCTL — SS_B Wave Form Select

This bit selects the output waveform for SS_B signal in master mode.

1 = Insert pulse between CSPI bursts
0 = SS_B stays low between CSPI bursts

This bit controls RXFIFO advancement in slave mode.

1 = RXFIFO is advanced by SS_B rising edge
0 = RXFIFO is advanced by BITCOUNT[3:0]

PHA—Phase

This bit controls the clock/data phase relationship.

1 = Phase 1 operation
0 = Phase 0 operation

POL—Polarity

This bit controls the polarity of the SCLK signal.

1 = Active low polarity (1 = idle)
0 = Active high polarity (0 = idle)

BITCOUNT[3:0]—Bit Count

This bit field selects the length of the transfer. A maximum of 16 bits can be transferred.

In master mode a 16-bit data word is loaded from the TXFIFO to the shift register and only the least n bits (n = BITCOUNT) are shifted out. The next 16-bit word is then loaded to shift register.

In slave mode when the SSCTL bit is 0 this field controls the number of bits received as a data word loaded to the RXFIFO. When the SSCTL bit is 1, this field is a don’t care.

Table 32 shows the BITCOUNT[3:0] encoding.

Table 32. BITCOUNT[3:0] Encoding

BITCOUNT[3:0]	Function
0000	1-bit transfer

Table 32. BITCOUNT[3:0] Encoding (Continued)

BITCOUNT[3:0]	Function
0001	2-bit transfer
. . .	. . .
1110	15-bit transfer
1111	16-bit transfer

7.3.7.4 Interrupt Control/Status Register (INTREG)

Register address: Base + 0x0C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BOEN	ROEN	RFEN	RHEN	RREN	TFEN	THEN	TEEN	BO	RO	RF	RH	RR	TF	TH	TE
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 39. Interrupt Control/Status Register (INTREG)

INTREG is a 32-bit register. The high 16 bits are reserved bits and are always read as 0.

TE—TXFIFO Empty Status

The TE bit is forced to 0 when the SPIEN is zero and will change to 1 after SPIEN is set.

1 = The TXFIFO is empty but data shifting may still be on-going
To make sure no data transaction is on-going, read the XCH bit in the CONTROLREG.

0 = At least one data word is in the TXFIFO

TH—TXFIFO Half Status

The TH bit is forced to 0 when the SPIEN is zero and will change to 1 after SPIEN is set.

1 = More than or equal to 4 empty slots in the TXFIFO

0 = Less than 4 empty slots in the TXFIFO

TF—TXFIFO Full Status

1 = 8 data words in the TXFIFO

0 = Less than 8 data words in the TXFIFO

RR—RXFIFO Data Ready Status.

1 = At least one data word is ready in the RXFIFO

0 = The RXFIFO is empty

RH—RXFIFO Half Status

1 = More than or equal to 4 data words in the RXFIFO

0 = Less than 4 data words in the RXFIFO

RF—RXFIFO Full Status

1 = 8 data words in the RXFIFO

0 = Less than 8 data words in the RXFIFO

RO—RXFIFO Overflow

This bit indicates that the RXFIFO has overflowed. At least one new written data word is lost. The RO flag is automatically cleared after a data read.

1 = RXFIFO has overflowed
At least one data word in the RXFIFO is overwritten
0 = RXFIFO has not overflowed

BO—Bit Count Overflow

This bit is set when the CSPI is in Slave CSPI FIFO advanced by SS_B rising edge mode and the slave is receiving more than 16 bits in one burst. This bit is cleared after a data read from the SPIRXD register. Because there are no error bits associated with individual RXFIFO data words this means that the entire RXFIFO contents are suspect.

1 = At least one data word in the RXFIFO had a bit count overflow error
0 = No bit count overflow

TEEN—TXFIFO Empty Interrupt Enable
1 = Enable
0 = Disable

THEN—TXFIFO Half Interrupt Enable
1 = Enable
0 = Disable

TFEN—TXFIFO Full Interrupt Enable
1 = Enable
0 = Disable

RREN—RXFIFO Data Ready Interrupt Enable
1 = Enable
0 = Disable

RHEN—RXFIFO Half Interrupt Enable
1 = Enable
0 = Disable

RFEN—RXFIFO Full Interrupt Enable
1 = Enable
0 = Disable

ROEN—RXFIFO Overflow Interrupt Enable
1 = Enable
0 = Disable

BOEN—Bit Count Overflow Interrupt Enable
1 = Enable
0 = Disable

7.3.7.5 CSPI Test Register (TESTREG)

Register address: Base + 0x10

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	TEST	LOOP	INIT	SYN	SSTATUS[3:0]				RXCNT[3:0]				TXCNT[3:0]			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 40. CSPI Test Register (TESTREG)

TESTREG is a 32-bit register that controls how the serial peripheral interface operates and reports status. The high 16 bits are reserved bits and are always read as 0.

TEST—Test

1 = Sample period counter increment value set to 0x0421
0 = Sample period counter increment value set to 0x1

LOOP—Internal Loop Back

1 = Internal loop back enabled
0 = Internal loop back disabled

INIT—Initialize State Machine and Edge Detect

This bit is used for test purposes only.

SYN—Synchronous Transfer

This bit is used for test purposes only.

SSTATUS[3:0]—State Machine Status

This bit field indicates the state machine status. These bits are used for test purposes only.

Table 33. SSTATUS[3:0] Encoding

SSTATUS[3:0]	Function	Description
0000	IDLE	waiting for EXCH or SLAVE_ENABLE
0001	EXCH	Waiting for DATAREADY_B
0010	SSB0	Set SS_B active
0011	T2	SS_B output low to first SPI_CK edge
0100	BUSY	Delay SPI_CK edge
0101	ACTIVE	Start data
0110	WAITCNT	Count data bits
0111	CK2SSB1	Last SCLK edge to SS_B output high delay
1000	T3	Insert SS_B high value
1001	SSB1	Slave Select is disabled
1010	WAITCNT2	SS_B output pulse width
1011	READY	Wait for DATAREADY_B active

RXCNT[3:0]—RXFIFO Counter

This bit field indicates the number of data words in the RXFIFO.Table 34 shows RXCNT[3:0] bit field encoding.

Table 34. RXCNT[3:0] Encoding

RXCNT[3:0]	Function
0000	RXFIFO is empty
0001	1 Data word in RXFIFO
0010	2 Data words in RXFIFO
0011	3 Data words in RXFIFO
0100	4 Data words in RXFIFO
0101	5 Data words in RXFIFO
0110	6 Data words in RXFIFO
0111	7 Data words in RXFIFO
1000	8 Data words in RXFIFO

TXCNT[3:0]—TXFIFO Counter

This bit field indicates the number of data words in TXFIFO. Table 35 shows TXCNT[3:0] bit field encoding.

Table 35. TXCNT[3:0] Encoding

TXCNT[3:0]	Function
0000	TXFIFO is empty
0001	1 Data word in TXFIFO
0010	2 Data words in TXFIFO
0011	3 Data words in TXFIFO
0100	4 Data words in TXFIFO
0101	5 Data words in TXFIFO
0110	6 Data words in TXFIFO
0111	7 Data words in TXFIFO
1000	8 Data words in TXFIFO

7.3.7.6 CSPI Sample Period Control Register (PERIODREG)

Register address: Base + 0x14

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CSRC	WAIT														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 41. CSPI Sample Period Control Register (PERIODREG)

PERIODREG is a 32-bit register that controls the time inserted between data transactions in master mode. The time inserted between samples can be from 0 to about 1 second at the resolution of bit clock or 32.768 kHz clock. The high 16 bits are reserved bits and will always be read as 0. The value of WAIT should be chosen to be greater than the total time to transmit one word of data (approximate BITCOUNT * DRCTL

* IPbus clock period). If this constraint is violated, new transmissions will be synchronized to the 32 kHz clock but each 32 kHz clock will not produce a new transmitted data word.

CSRC—Clock source for period counter
1 = 32.68 kHz
0 = Bit clock

WAIT—Number of Clocks Inserted between Data Transactions

Table 36 shows WAIT bit field encoding.

Table 36. WAIT Encoding

WAIT	Function
0x0000	0 Clock
0x0001	1 Clock
0x0002	2 Clocks
. . .	. . .
0x7FFF	32768 Clocks

7.3.7.7 CSPI Soft Reset Register (RESETREG)

Register address: Base + 0x1C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																START
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 42. CSPI Soft Reset Register (RESETREG)

RESETREG is a 32-bit register. Writing a 1 to the START bit resets the CSPI module. All registers in the CSPI are reset including the CONTROLREG.

START — Soft Reset

The soft reset is extended by two clock cycles so there must be at least three IP_BUS clocks before any attempt is made to write the CONTROLREG to initiate CSPI operation after the START bit is written.
1 = Soft reset
0 = No soft reset

7.3.8 Functional Description

7.3.8.1 General

The CSPI module allows full-duplex, synchronous, serial communication between the MC72000 and peripheral devices. Software can poll the CSPI status flags or CSPI operation can be interrupt-driven. Figure 43 shows the generic CSPI timing.

Configure the CSPI modules as master or slave before enabling them. The master CSPI should be enabled before enabling the slave CSPI. The slave CSPI should be disabled before disabling the master CSPI. See Section 7.3.7.3, "Control Register (CONTROLREG)." SPI_CK must be in the proper idle state before the slave is enabled to prevent SPI_CK from appearing as a clock edge.

The following section describes the operation of the CSPI module.

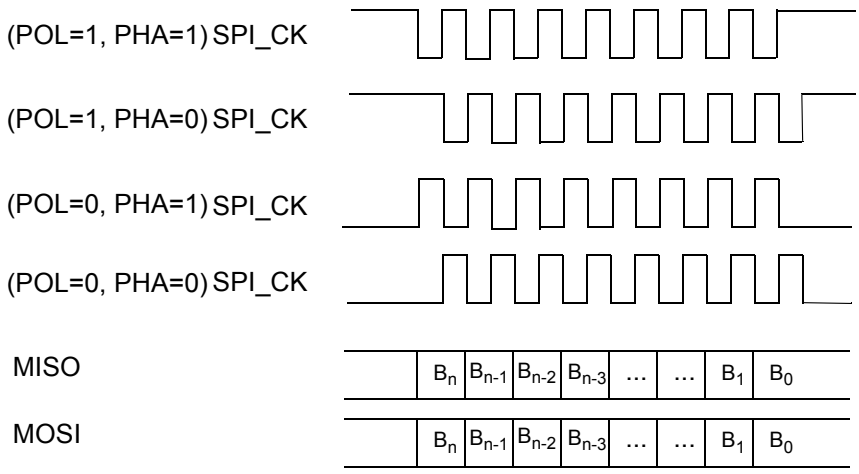


Figure 43. CSPI Generic Timing

The CSPI does not consume any power when it is disabled.

7.3.8.2 Phase/Polarity Configurations

The serial peripheral interface master uses the SPI_CK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity variations. In phase 0 operation, output data changes on the falling clock edges and input data is shifted in on rising edges. The most significant bit (MSB) is output when the ARM7 loads the transmitted data. In phase 1 operation, output data changes on the rising edges of the clock and input data is shifted in on falling edges. The MSB is output on the first rising SPI_CK edge. Polarity inverts SPI_CK, but does not change the edge-triggered events that are internal to the serial peripheral interface master. This flexibility allows the CSPI to operate with most serial peripheral devices on the market.

7.3.8.3 Master Mode Operation

When the CSPI is configured as a master, in order to utilize the internal TXFIFO and RXFIFO, two auxiliary output signals—SS_B and DATAREADY_B—are used for data transfer rate control. The user can also program the sample period control register to a fixed data transfer rate.

Only a master SPI module can initiate transmissions. Software begins the transmission from a master SPI module by writing to the XCH bit. If SPIRDY[1:0] is set to zero and the PERIODREG[14:0] is set to zero, then the first word in the TX FIFO immediately transfers to the shift register and begins shifting out on the MOSI pin under the control of the serial clock.

The DRCTL[2:0] bits control the baud rate generator and determine the speed of the shift register. Through the SPI_CK pin, the baud rate generator of the master also controls the shift register of the slave peripheral.

As the byte shifts out on the MOSI pin of the master, another byte shifts in from the slave on the master's MISO pin. The transmission ends when the receive FIFO full bit, RF, becomes set. Software clears the RF bit by reading the RX data register.

7.3.8.4 Slave Mode Operation

The CSPI operates in slave mode when the MODE bit is clear. In slave mode, the SPI_CK pin is the input for the serial clock from the ARM7. Before a data transmission occurs, the SS_B pin of the slave CSPI must be at logic zero. SS_B must remain low until the transmission is complete.

If the CSPI is configured as slave, the user can set the CSPI control register to match the external CSPI master's setting for PHA and POL. SS_B becomes an input signal and is used for capturing data in the internal receive shift register and for loading data to the internal transmit data shift register. This also increments the TXFIFO and RXFIFO.

In a slave CSPI module, data enters the shift register under the control of the serial clock from the master CSPI module. After a word enters the shift register of a slave CSPI, it transfers to the receive FIFO data register, and the receive FIFO count is incremented. To prevent an overflow condition, slave software then must read the receive data FIFO register before another full word enters the shift register.

The maximum frequency of the SPI_CK for a CSPI configured as a slave must be less than one-fourth the bus clock speed. The frequency of the SPI_CK for a CSPI configured as a slave does not have to correspond to any CSPI baud rate. The baud rate only controls the speed of the SPI_CK generated by a CSPI configured as a master. Therefore, the frequency of the SPI_CK for a CSPI configured as a slave can be any frequency less than one-fourth the bus speed.

When the master CSPI starts a transmission, the data in the slave shift register begins shifting out on the MISO pin. The slave can load its shift register with a new word for the next transmission by writing to its transmit data FIFO register. The slave must write to its transmit data FIFO register at least eight bus cycles before the master ends the last word transmission. Otherwise, the word already in the slave shift register shifts out on the MISO pin.

7.3.9 Timing Diagrams

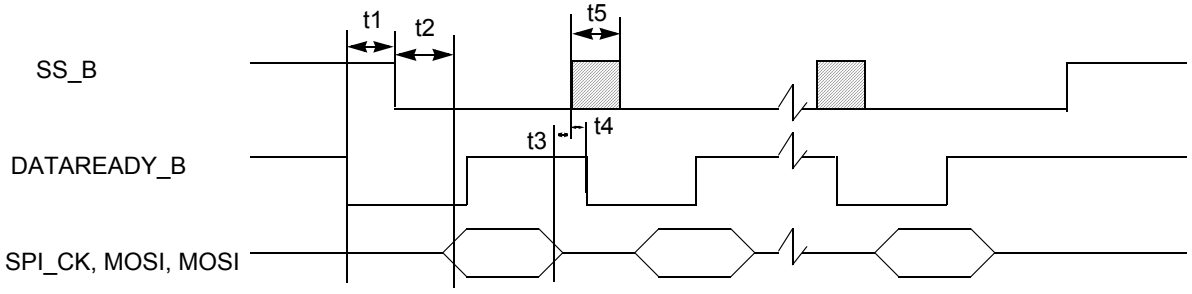


Figure 44. Master CSPI Timing Using DATAREADY_B Edge Trigger

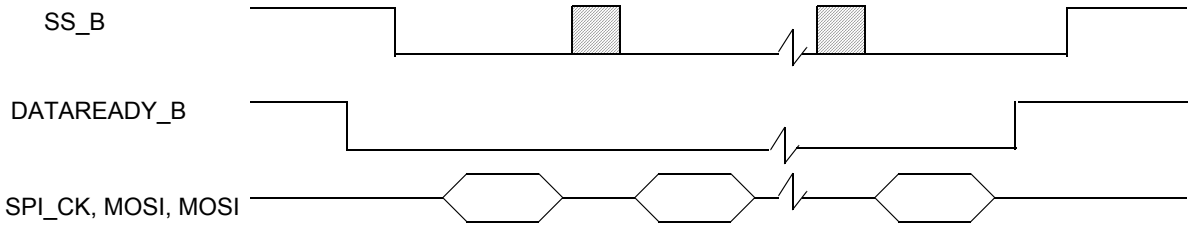


Figure 45. Master CSPI Timing Using DATAREADY_B Level Trigger

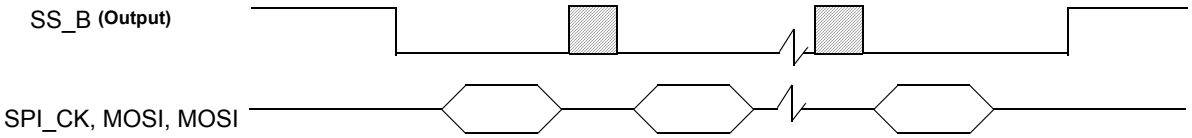


Figure 46. Master CSPI Timing Don't Care DATAREADY_B Level Trigger

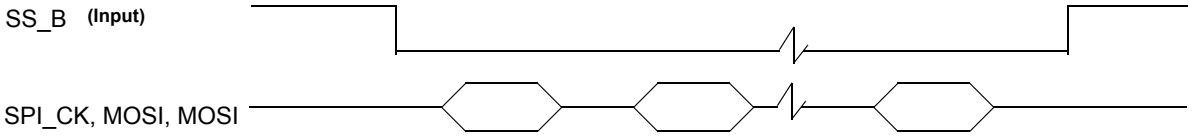


Figure 47. Slave CSPI Timing FIFO Advanced by BITCOUNT

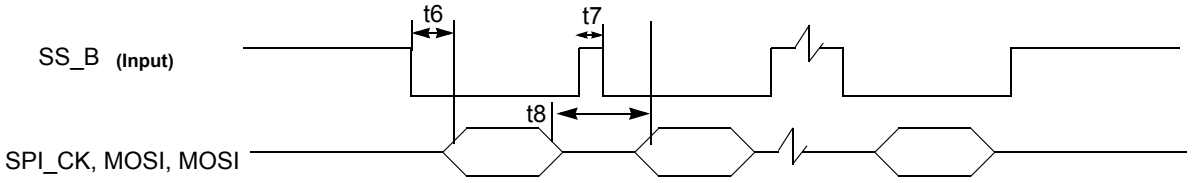


Figure 48. Slave CSPI Timing FIFO Advanced by SS_B Rising Edge

Table 37. CSPI Timing

Num	Characteristic	3.3V		Unit
		Minimum	Maximum	
	DATAREADY_B to SS_B output low	—	?	ns
	SS_B output low to first SPI_CK edge	$2T^1$	—	ns
	Last SCLK edge to SS_B output high	$2T^2$	—	ns
	SS_B output high to DATAREADY_B low	?	—	ns
	SS_B output pulse width	$2T^3$ + $WAIT^4$	—	ns
	SS_B input low to first SPI_CK edge	?	—	ns
	SS_B input pulse width	0	—	ns

Table 37. CSPI Timing

Num	Characteristic	3.3V		Unit
		Minimum	Maximum	
	Pause between data word	0	—	ns

1.T = CSPI clock period
2.T = CSPI clock period
3.T = CSPI clock period
4.WAIT = Number of sysclk or 32.768 kHz clocks per sample period control register.

7.4 Synchronous Serial Interface (SSI)

7.4.1 Overview

This section describes the Synchronous Serial Interface (SSI), and discusses the architecture, the programming model, the operating modes, and initialization of the SSI. The SSI is a full-duplex, serial port that allows the MC72000 to communicate with a variety of serial devices, including industry-standard CODECs, other MCUs, and peripheral devices that implement the Motorola Serial Peripheral Interface (SPI). It is typically used to transfer samples in a periodic manner. The SSI consists of independent transmitter and receiver sections with independent clock generation and frame synchronization.

The first-time reader should read Section 7.4.2, “Features,” and then Section 7.4.6, “Functional Description.”

7.4.2 Features

SSI features include the following:

- Independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/external clocks and frame syncs
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as thirty-two time slots
- Gated clock mode operation requiring no frame sync
- Programmable internal clock divider
- Programmable word length (8, 10, 12, or 16 bits)
- Program options for frame sync and clock generation
- SSI power-down feature

7.4.3 Block Diagram

NOTE:

The MC72000 only supports synchronous mode, which limits the number of pins available.

Figure 49 shows a block diagram of the SSI. It consists of three control registers to set up the port, one status/control register, separate transmit and receive circuits with FIFO registers, and separate serial clock and frame sync generation for the transmit and receive sections.

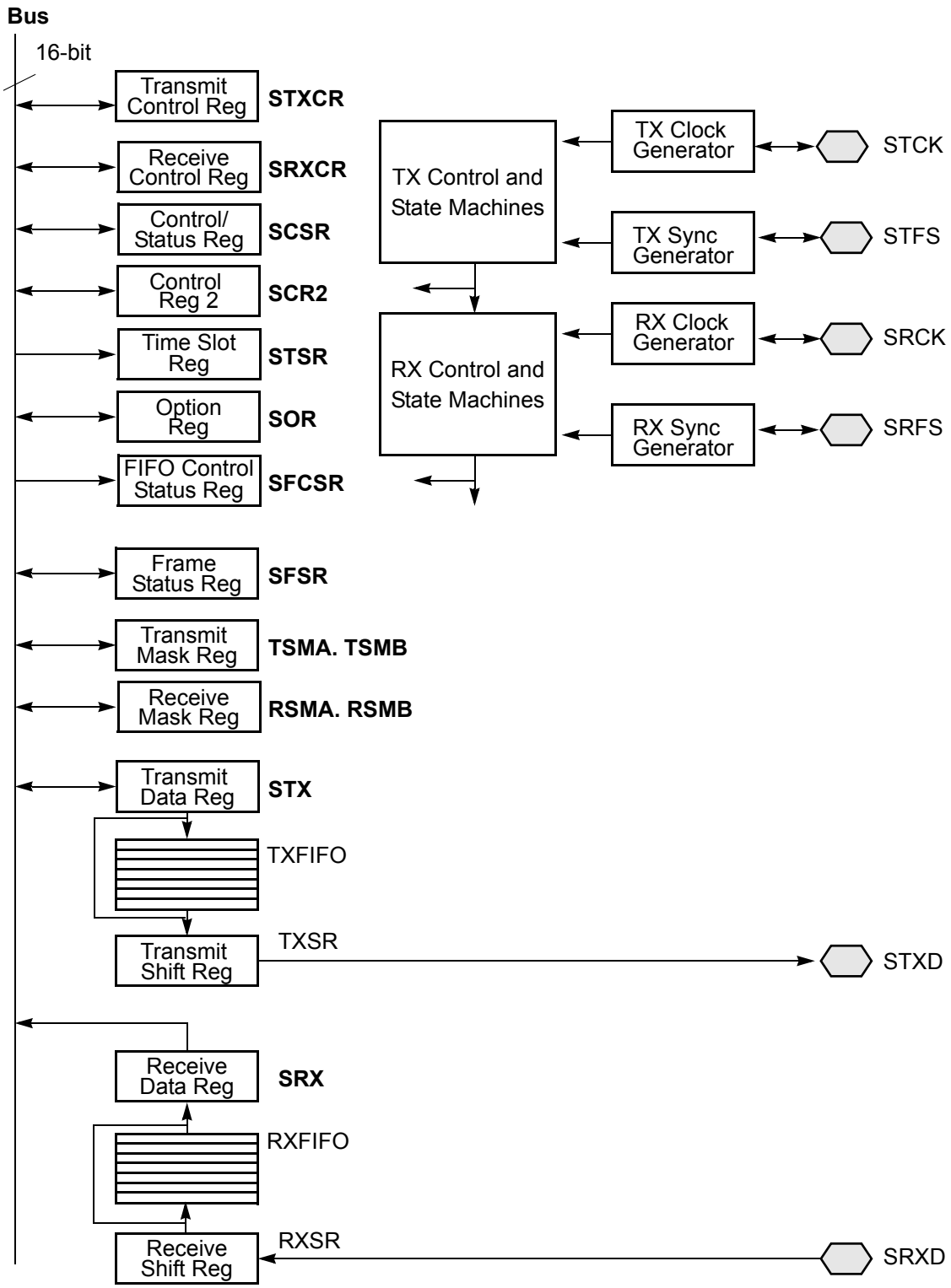


Figure 49. SSI Block Diagram

7.4.4 Signal Descriptions

Table 38. Signal Properties

Name	I/O Type	Function	Reset State	Notes
STCK	I/O	SSI Transmit Clock	input	Controlled by reset state of TXDIR bit in STXCR register
STFS	I/O	SSI Transmit Frame Sync	input	Controlled by reset state of TFDIR bit in SOR register
STXD	output	SSI Transmit Data	high-Z	Since SSIEN bit of STXCR register is reset to 0.
SRXD	input	SSI Receive Data	-	

7.4.4.1 External Signals

7.4.4.1.1 STCK — SSI Transmit Clock

This pin can be configured as either an input or an output pin. This clock signal is used by the transmitter and can be either continuous or gated. During gated clock mode, the STCK pin is active only during the transmission of data, otherwise, it is inactive (low). In synchronous mode, this pin is used by both the transmit and receive sections.

7.4.4.1.2 STFS — SSI Transmit Frame Sync

This pin can be configured as either an input or an output pin. The frame sync is used by the transmitter to synchronize the transfer of data. The frame sync signal can be one bit or one word in length. The start of the frame sync can occur one bit before the transfer of data or right at the start of the data transfer.

In synchronous mode, this pin is used by both the transmit and receive sections. In gated clock mode, frame sync signals are not used.

7.4.4.1.3 SRCK — SSI Receive Clock

This pin can be configured as either an input or an output pin. This clock signal is used by the receiver and can be either continuous or gated. During gated clock mode, the SRCK pin is active only during the reception of data, otherwise, it is inactive (low).

In synchronous mode, this pin is not used and can be configured as a GPIO pin.

7.4.4.1.4 SRFS — SSI Receive Frame Sync

This pin can be configured as either an input or an output pin. The frame sync is used by the receiver to synchronize the transfer of data. The frame sync signal can be one bit or one word in length. The start of the frame sync can occur one bit before the transfer of data or right at the start of the data transfer.

In synchronous mode, this pin is not used and can be configured as a GPIO pin.

7.4.4.1.5 STXD — SSI Transmit Data

This pin transmits data from the serial transmit shift register (STSR). The STXD pin is an output pin when data is being transmitted and is inactive (high-Z) between data word transmissions.

7.4.4.1.6 SRXD — SSI Receive Data

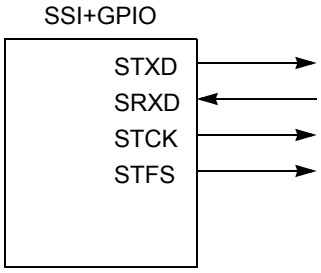
This pin is used to bring serial data into the receive data shift register (RXSR).

7.4.4.2 SSI Configurations

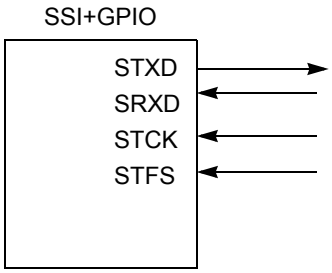
Figure 50 shows the main SSI configurations. These pins support all transmit and receive functions with continuous or gated clock as shown. Section 7.4.6, “Functional Description,” describes the clock, frame sync, and data timing relationships in each of the modes available. Note that gated clock implementations do not require the use of the frame sync pins. In this case, these pins can be used as GPIO pins, if needed.

NOTE:

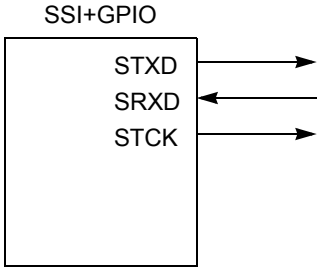
The GPIO is a separate module which alternatively controls the function and state of the I/O pins. See the GPIO module definition for alternate functions of the I/O pins defined here.



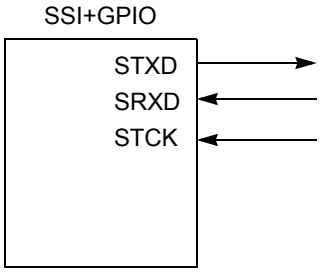
SSI Internal Continuous Clock (RXDIR=0, TXDIR=1, RFDIR=X, TFDIR=1, SYN=1)



SSI External Continuous Clock (RXDIR=0, TXDIR=0, RFDIR=X, TFDIR=0,SYN=1)



SSI Internal Gated Clock (RXDIR=1, TXDIR=1, SYN=1)



SSI External Gated Clock (RXDIR=1, TXDIR=0, SYN=1)

Figure 50. Synchronous SSI Configurations—Continuous and Gated Clock

7.4.5 Memory Map and Registers

7.4.5.1 SSI Memory Map

Table 39 shows the SSI memory map. Note there are four registers that are not accessible.

Table 39. SSI Memory Map

Address	Reg Name	Description
Base + 0x00	SSI Transmit Data Register (STX)	write only
—	SSI Transmit FIFO Register (TXFIFO)	
—	SSI Transmit Shift Register (TXSR)	
Base + 0x02	SSI Receive Data Register (SRX)	read only
—	SSI Receive FIFO Register (RXFIFO)	
—	SSI Receive Shift Register (RXSR)	
Base + 0x04	SSI Control/Status Register (SCSR)	lower byte read-only
Base + 0x06	SSI Control Register 2 (SCR2)	
Base + 0x08	SSI Transmit Control Register (STXCR)	
Base + 0x0A	SSI Receive Control Register (SRXCR)	
Base + 0x0C	SSI Time Slot Register (STSR)	write only
Base + 0x0E	SSI FIFO Control/Status Register (SFCSR)	
Base + 0x10	SSI Test Register (STR)	
Base + 0x12	SSI Option Register (SOR)	
Base + 0x14	SSI Transmit Slot Mask A (TSMA)	
Base + 0x16	SSI Transmit Slot Mask B (TSMB)	
Base + 0x18	SSI Receive Slot Mask A (RSMA)	
Base + 0x1A	SSI Receive Slot Mask B (RSMB)	
Base + 0x1C	SSI Frame Status Register (SFSR)	read only

All registers in the SSI are 16-bit accessible only.

7.4.5.2 Register Descriptions

The following sections describe the SSI registers.

7.4.5.2.1 SSI Transmit Data Register (STX)

The STX register is a 16-bit, read-write register. Data to be transmitted is written into this register. If the transmit FIFO is enabled, data is transferred from this register to the transmit FIFO register when the FIFO can accommodate the data. Otherwise, data written to this register is transferred to the transmit shift register (TXSR) when shifting of previous data is completed. The data written occupies the most significant portion of the STX register. The unused bits (least significant portion) of the STX register are ignored.

If the transmit interrupt is enabled, the interrupt is asserted when the STX register becomes empty (TDE=1). If the transmit FIFO is also enabled, the transmit FIFO must be below its watermark for the interrupt to assert.

NOTE:

Enable SSI (SSIEN=1) before writing to STX.

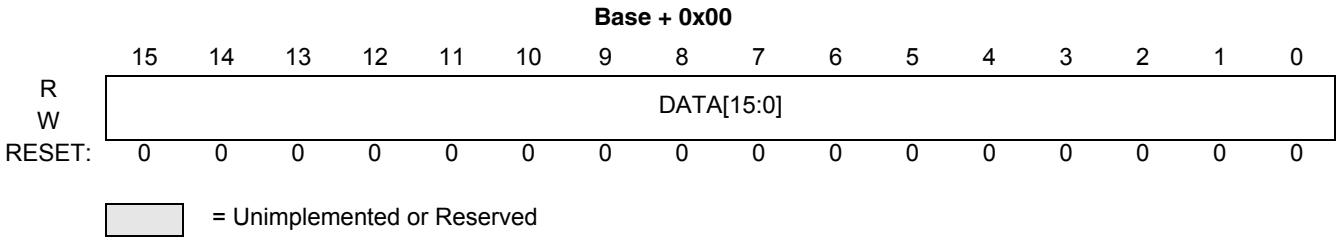


Figure 51. STX Register Diagram

7.4.5.2.2 SSI Transmit FIFO Register (TXFIFO)

The TXFIFO is a 7 x 16 bit register used to buffer samples written to the transmit data register (STX). It is written by the contents of STX whenever the transmit FIFO feature is enabled. When enabled, the transmit shift register (TXSR) receives its values from this FIFO register. If the transmit FIFO feature is not enabled, this register is bypassed and the contents of STX are transferred into the TXSR.

When the transmit interrupt enable (TIE) bit in the SCR2 and transmit data register empty (TDE) bit in the SCSR are set, the transmit interrupt is asserted whenever STX is empty and the data level in the SSI transmit FIFO falls below the selected threshold.

When both TXFIFO and STX are full, any further write will overwrite the contents of TXFIFO and STX.

NOTE:

Enable SSI before writing to TXFIFO and STX.

7.4.5.2.3 SSI Transmit Shift Register (TXSR)

TXSR is a 16-bit shift register that contains the data being transmitted. When a continuous clock is used, data is shifted out to the serial transmit data (STXD) pin by the selected (internal/external) bit clock when the associated (internal/external) frame sync is asserted. When a gated clock is used, data is shifted out to the STXD pin by the selected (internal/external) gated clock. The word length control bits (WL[1:0]) in the SSI transmit control register (STXCR) determine the number of bits to be shifted out of the TXSR before it is considered empty and can be written to again. See Section 7.4.5.2.7, “SSI Transmit and Receive Control Registers (STXCR, SRXCR),” for more information. This word length can be 8, 10, 12, or 16 bits. The data to be transmitted occupies the most significant portion of the shift register. The unused portion of the register is ignored. Data is always shifted out of this register with the most significant bit (MSB) first when the SHFD bit of the SCR2 is cleared. If this bit is set, the least significant bit (LSB) is shifted out first.

See Figure 52 and Figure 53 for more information.

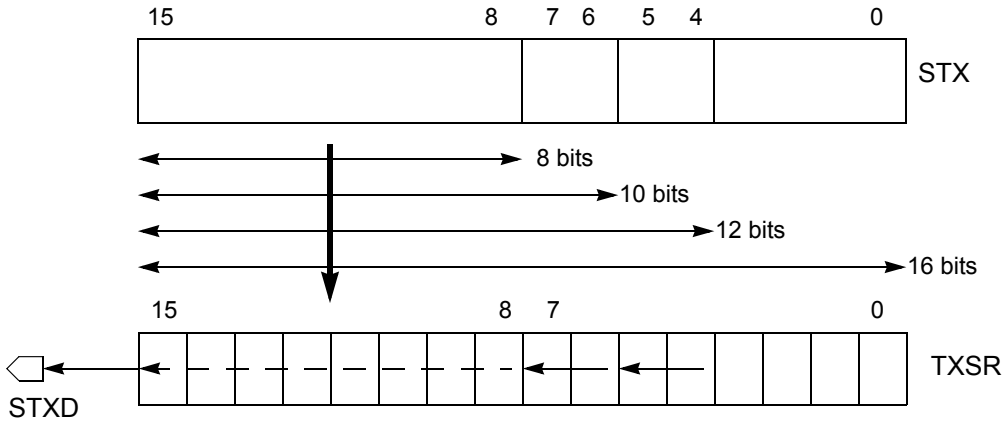


Figure 52. Transmit Data Path (TSHFD=0)

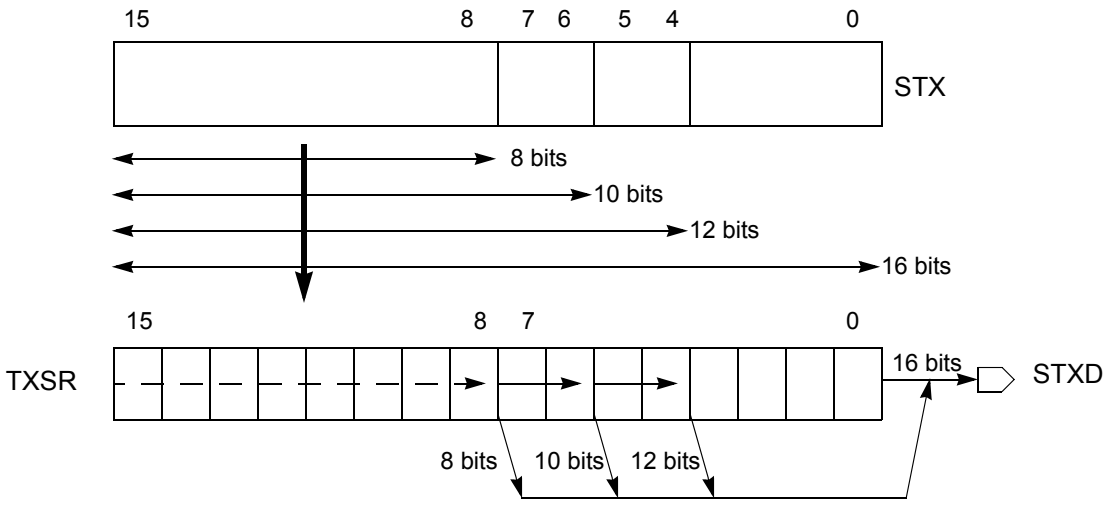


Figure 53. Transmit Data Path (TSHFD=1)

7.4.5.2.4 SSI Receive Data Register (SRX)

The SRX is a 16-bit, read-only register. It always accepts data from the receive shift register (RXSR) as it becomes full. The data read occupies the most significant portion of the SRX register. The unused bits (least significant portion) are read as 0s.

If the receive data full interrupt is enabled, the interrupt is asserted whenever the SRX register becomes full. If the receive FIFO is also enabled, the receive FIFO must be above its watermark before the interrupt is asserted.

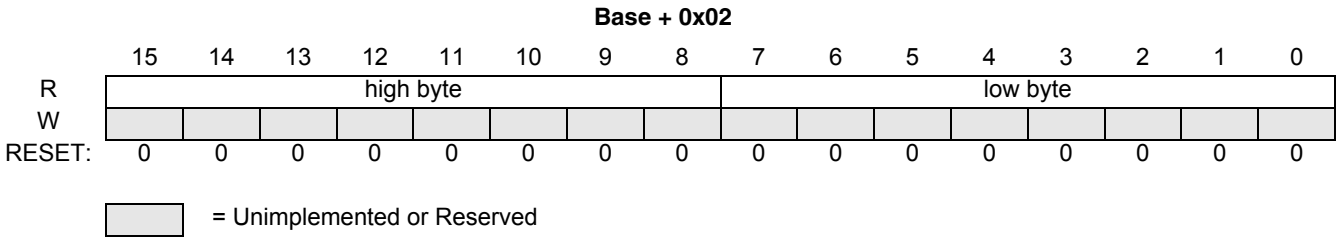


Figure 54. SRX Register Diagram

7.4.5.2.5 SSI Receive FIFO Register (RXFIFO)

The RXFIFO is a 7 x 16-bit FIFO register used to buffer samples received in the SSI receive data register (SXR). The receive FIFO is enabled by setting the RFEN bit of the SCR2 control register. Received data is then held in the FIFO if the data in the SRX has not yet been read.

If the receive interrupt is enabled, it is asserted whenever the SRX is full and the data level in the SSI receive FIFO reaches the selected threshold. If the receive FIFO feature is not enabled, this register is bypassed and the receive shift register (RXSR) data is automatically transferred into the SRX.

7.4.5.2.6 SSI Receive Shift Register (RXSR)

RXSR is a 16-bit shift register that receives incoming data from the serial receive data SRXD pin. When a continuous clock is used, data is shifted in by the selected (internal/external) bit clock when the associated (internal/external) frame sync is asserted. When a gated clock is used, data is shifted in by the selected (internal/external) gated clock. Data is assumed to be received MSB first if the SHFD bit of the SCR2 is cleared. If this bit is set, the data is received LSB first. Data is transferred to the SSI receive data register (SRX) or receive FIFO (if the receive FIFO is enabled and SRX is full) after 8, 10, 12, or 16 bits have been shifted in depending on the WL[1:0] control bits. For receiving 8, 10, or 12 bits data, LSB bits are set to zero.

See Figure 55 and Figure 56 for more information.

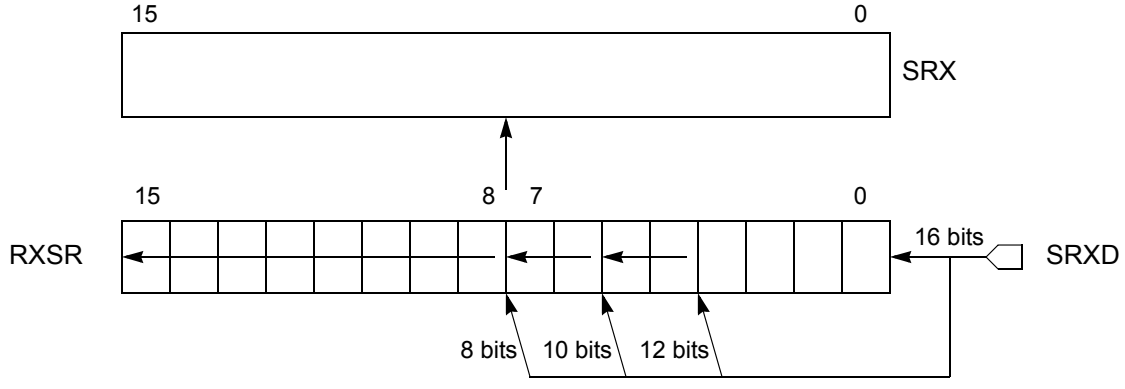


Figure 55. Receive Data Path (RSHFD=0)

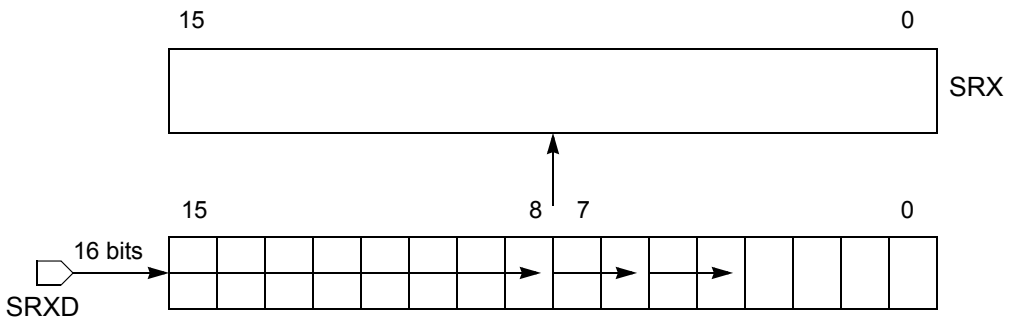


Figure 56. Receive Data Path (RSHFD=1)

7.4.5.2.7 SSI Transmit and Receive Control Registers (STXCR, SRXCR)

STXCR and SRXCR are 16-bit, read/write control registers used to direct the operation of the SSI. These registers control the SSI clock generator bit and frame sync rates, word length, and number of words per frame for the serial data. The STXCR register is dedicated to the transmit section. The SRXCR register is dedicated to the receive section except in synchronous mode, where the STXCR register controls both the receive and transmit sections. Power-on reset clears all STXCR and SRXCR bits. SSI reset does not affect the STXCR and SRXCR bits. The control bits are described in the following paragraphs. Although the bit patterns of the SRXCR and SCTRX registers are the same, the contents of these two registers can be programmed differently.

Base + 0x08

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PSR	WL[1:0]		DC[4:0]					PM[7:0]							
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 57. STXCR Register Diagram

Base + 0x0A

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PSR	WL[1:0]		DC[4:0]					PM[7:0]							
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 58. SRXCR Register Diagram

PSR—Prescaler Range

This bit controls a fixed divide-by-8 prescaler in series with the variable prescaler. It extends the range of the prescaler for those cases where a slower bit clock is desired.

1 = When the PSR bit is set, the fixed divide-by-eight prescaler is operational. This allows a 128 kHz master clock to be generated for Motorola MC1440x series CODECs. The maximum internally generated bit clock frequency is $F_{IP\_CLK}/(2x2)$ and the minimum internally generated bit clock frequency is $F_{IP\_CLK}/(4 \times 2 \times 8 \times 256 \times 2)$.

0 = When the PSR bit is cleared, the fixed prescaler is bypassed.

WL[1:0]—Word Length Control

This bit field is used to select the length of the data words being transferred by the SSI. Word lengths of 8, 10, 12, or 16 bits can be selected. Table 40 shows WL[1:0] bit field encoding.

Table 40. WL[1:0] Encoding

WL[1:0]	Number of Bits/Word
00	8
01	10
10	12
11	16

These bits control the word length divider shown in the SSI clock generator. The WL control bits also control the frame sync pulse length when the TFSL bit is cleared.

DC[4:0]—Frame Rate Divider Control

This bit field controls the divide ratio for the programmable frame rate dividers. The divide ratio operates on the word clock.

In normal mode, this ratio determines the word transfer rate. The divide ratio ranges from 1 to 32 (DC[4:0] = 00000 to 11111) in normal mode. A divide ratio of one (DC=00000) provides continuous periodic data word transfer. A bit-length sync must be used in this case.

In network mode, this ratio sets the number of words per frame. The divide ratio ranges from 2 to 32 (DC[4:0] = 00001 to 11111) in network mode. A divide ratio of one (DC=00000) in network mode is a special case (on demand mode) that is not supported in this implementation.

PM[7:0]—Prescale Modulus Select

This bit field specifies the divide ratio of the prescale divider in the SSI clock generator. This prescaler is used only in internal clock mode to divide the internal clock of the core. A divide ratio from 1 to 256 (PM[7:0] = $00 to $FF) can be selected. The bit clock output is available at the STCK or SRCK clock pins. The bit clock on the SSI can be calculated from the peripheral clock value using the following equation:

$f_{FIX\_CLK} = f_{IP\_bus\_CLK}$/4if DIV4DIS = 0

$f_{FIX_CLK} = f_{IP_bus_CLK}$if DIV4DIS = 1

$f_{INT\_BIT\_CLK} = f_{FIX\_CLK}/[4 \times (7 \times PSR + 1) \times (PM + 1)]$

where PM = PM[7:0]

$f_{FRAME\_SYN\_CLK} = (f_{INT\_BIT\_CLK})/[(DC + 1) \times WL]$

where DC = DC[4:0] and WL = 8, 10, 12, or 16

For example, with 8-bit words operating in normal mode, if an 8 kHz sampling rate is desired the following parameters can be used:

$f_{IP\_bus\_CLK} = f_{SYSTEM\_CLK} / 2$ = 120 MHz / = 60 mhz

$f_{FIX\_CLK} = f_{IP\_bus\_CLK}$ = 60 MHzDIV4DIS = 1

$f_{INT\_BIT\_CLK} = f_{FIX\_CLK}/[4 \times (7 \times PSR + 1) \times (PM + 1)]$

= 60 MHz / [4 x 1 x 117] = 128.2 kHzPS = 0, PM = 116

$f_{FRAME_SYN_CLK} = (f_{INT_BIT_CLK})/[(DC + 1) \times WL]$DC = 1

= 128 kHz / [2 x 8] = 8.012 kHz

The bit clock output is also available internally for use as the bit clock to shift the transmit and receive shift registers. Careful choice of the crystal oscillator frequency and the prescaler modulus allows the telecommunication industry standard CODEC master clock frequencies of 2.048 MHz, 1.544 MHz, and 1.536 MHz to be generated. For example, a 24.576 MHz clock frequency can be used to generate the standard 2.048 MHz and 1.536 MHz rates, and a 24.704 MHz clock frequency can be used to generate the standard 1.544 MHz rate. Table 41 gives examples of PM[7:0] values that can be used in order to generate different bit clocks.

Table 41. SSI Bit Clock as a Function of Peripheral Clock and Prescale Modulus

IPG_CLK (MHz) DIV4DIS = 1	Max Bit Clock, FIX_CLK/4 (MHz)	PM[7:0] Values For Different SCK			
		2.048 MHz	1.544 MHz	512 kHz (PSR=0)	64 kHz (PSR=0)
32	8	1	—	16	128
24	6	—	4	12	96
16	4	2	—	8	64
12	3			6	48

7.4.5.2.8 SSI Control/Status Register (SCSR)

The SCSR is a 16-bit register used to set up and monitor the SSI. The top half of the register (bits [15:8]) is the read/write portion and is used for SSI setup. The bottom half of the register (bits [7:0]) is read-only and is used to interrogate the status and serial input flags of the SSI. The control and status bits are described in the following paragraphs.

NOTE:

SSI Status flag is updated when SSI is enabled.

NOTE:

All the flags in the status portion of the SCSR are updated after the first bit of the next SSI word has completed transmission or reception. Some status bits (ROE and TUE) are cleared by reading the SCSR followed by a read or write to either the SRX or STX register.

Base + 0x04

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DIV4DIS	RSHFD	RSCKP	RDMAE	TDMAE	RFSI	RFSL	REFS	RDR	TDE	ROE	TUE	TFS	RFS	RFF	TFE
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 59. SCSR Register Diagram

DIV4DIS—Divider 4 Disable

1 = FIX_CLK is equal to IP_CLK

0 = FIX_CLK = IP_CLK/4 for both transmitter and receiver clock generator circuits

RSHFD—Receive Shift Direction

This bit controls whether the MSB or LSB is received first for the receive section. If the RSHFD bit is cleared, data is received MSB first. If the RSHFD bit is set, the LSB is received first.

NOTE:

The CODEC device labels the MSB as bit 0, whereas the SSI labels the LSB as bit 0. Therefore, when using a standard CODEC, the SSI MSB (or CODEC bit 0) is shifted out first, and the RSHFD bit should be cleared.

RSCKP—Receive Clock Polarity

This bit controls which bit clock edge is used to latch in data for the receive section.

1 = The rising edge of the clock is used to latch the data in
0 = The data is latched in on the falling edge of the clock

RDMAE—Receive DMA Enable

This bit is Reserved and should always be written 0.

TDMAE—Transmit DMA Enable

This bit is Reserved and should always be written 0.

RFSI—Receive Frame Sync Invert

This bit selects the logic of frame sync I/O for the receive section.

1 = The frame sync is active low
0 = The frame sync is active high

RFSL—Receive Frame Sync Length

This bit selects the length of the frame sync signal to be generated or recognized for the receive section. See Figure 60 for an example timing diagram of the FS options.

1 = A one clock bit-long frame sync is selected
0 = A one word-long frame sync is selected

The length of a word-long frame sync is the same as the length of the data word selected by WL[1:0].

REFS—Receive Early Frame Sync

This bit controls when the frame sync is initiated for the receive section. See Figure 60 for an example timing diagram of the FS options.

1 = The frame sync is initiated one bit before the data is received
The frame sync is disabled after one bit-for-bit length frame sync and after one word-for-word length frame sync.

0 = When the REFS bit is cleared, the frame sync is initiated as the first bit of data is received

RDR—Receive Data Ready Flag

This flag bit is set when receive data register (SRX) or receive FIFO (RXFIFO) is loaded with a new value.

RDR is cleared when the CPU reads the SRX register. If RXFIFO is enabled, RDR is cleared when receive FIFO is empty.

If the RIE bit is set, a receive data interrupt request is issued when the RDR bit is set. The interrupt request vector depends on the state of the receiver overrun (ROE) bit (in the SCSR). The RDR bit is cleared by POR and SSI reset.

TDE—Transmit Data Register Empty

This flag bit is set when there is no data waiting to be transferred to the TXSR register. If the transmit FIFO (TXFIFO) is enabled, this occurs when there is at least one empty slot in STX or TXFIFO. If the TXFIFO is not enabled, this occurs when the STX is empty, that is, when the contents of the STX register are transferred into the transmit shift register (TXSR). When set, the TDE bit indicates that data should be written to the STX register or to the STSR before the transmit shift register becomes empty, or an underrun error will occur.

The TDE bit is cleared when data is written to the STX register or to the STSR to disable transmission of the next time slot. If the TIE bit is set, an SSI transmit data interrupt request is issued when the TDE bit is set. The vector of the interrupt depends on the state of the TUE bit (in the SCSR). The TDE bit is set by power-on and SSI reset.

ROE—Receive Overrun Error

This flag bit is set when the receive shift register (RXSR) is filled and ready to transfer to the SRX register or the RXFIFO register (when enabled), and these registers are already full. If the receive FIFO is enabled, this is indicated by the receive FIFO full (RFF) bit else this is indicated by the receive data ready (RDR) bit being set. The RXSR is not transferred in this case.

NOTE:

When using the RXFIFO with a watermark other than 8, the ROE bit does not mean that data has been lost. The RXCNT field of the SFCSR should be checked to determine the likelihood of actual data loss.

A receive overrun error does not cause any interrupts. However, when the ROE bit is set, it causes a change in the interrupt vector used, allowing the use of a different interrupt handler for a receive overrun condition. If a receive interrupt occurs with the ROE bit set, the receive data with exception status interrupt is generated. If a receive interrupt occurs with the ROE bit cleared, the receive data interrupt is generated. The ROE bit is cleared by power-on or SSI reset and is cleared by reading the SCSR with the ROE bit set, followed by reading the SRX register. Clearing the RE bit does not affect the ROE bit.

TUE—Transmitter Underrun Error

This flag bit is set when the TXSR is empty (no data to be transmitted), as indicated by the TDE bit being set, and a transmit time slot occurs. When a transmit underrun error occurs, the previously sent data is retransmitted.

A transmit time slot in the normal mode occurs when the frame sync is asserted. In network mode, each time slot requires data transmission and, therefore, may cause a TUE error.

The TUE bit does not cause any interrupts. However, the TUE bit does cause a change in the interrupt vector used for transmit interrupts so that a different interrupt handler can be used for a transmit underrun condition. If a transmit interrupt occurs with the TUE bit set, the transmit data with exception status interrupt is generated. If a transmit interrupt occurs with the TUE bit cleared, the transmit data interrupt is generated.

The TUE bit is cleared by power-on or SSI reset. The TUE bit is also cleared by reading the SCSR with the TUE bit set, followed by writing to the STX register or to the STSR.

TFS—Transmit Frame Sync

When set, this flag bit indicates that a frame sync occurred during transmission of the last word written to the STX register. As shown in Figure 60b, data written to the STX register during the time slot when the TFS bit is set is transmitted during the second time slot (in network mode) or in the next first time slot (in normal mode). In network mode, the TFS bit is set during transmission of the first slot of the frame. It is then cleared when starting transmission of the next slot. The TFS bit is cleared by power-on or SSI reset.

RFS—Receive Frame Sync

When set, this flag bit indicates that a frame sync occurred during receiving of the next word into the SRX register, as shown in Figure 60c. In network mode, the RFS bit is set while the first slot of the frame is being received. It is cleared when the next slot of the frame begins to be received. The RFS bit is cleared by power-on or SSI reset.

RFF—Receive FIFO Full

This flag bit is set when the receive section is programmed with the receive FIFO enabled, and the data level in the RXFIFO reaches the selected receive FIFO watermark (RFWM) threshold. When set, RFF indicates that data can be read via the SRX register.

NOTE:

An interrupt is only generated if both the RFF and RIE bits are set if RXFIFO is enabled.

The RFF bit is cleared in normal operation by reading the SRX register. The RFF is also cleared by power-on reset or disabling the SSI.

When RXFIFO is completely full, all further received data is ignored until data is read.

TFE—Transmit FIFO Empty

This flag bit is set when the transmit section is programmed with the TXFIFO enabled and the data level in the TXFIFO falls below the selected transmit FIFO watermark (TFWM) threshold. When set, the TFE bit indicates that data can be written to the TXFIFO register. The TFE bit is cleared by writing data to the STX register until the TXFIFO data content level reaches the watermark level.

NOTE:

An interrupt is generated only if both the TFE and the TIE bits are set if transmit FIFO is enabled.

The TFE bit is set by power-on reset and when SSI is disabled.

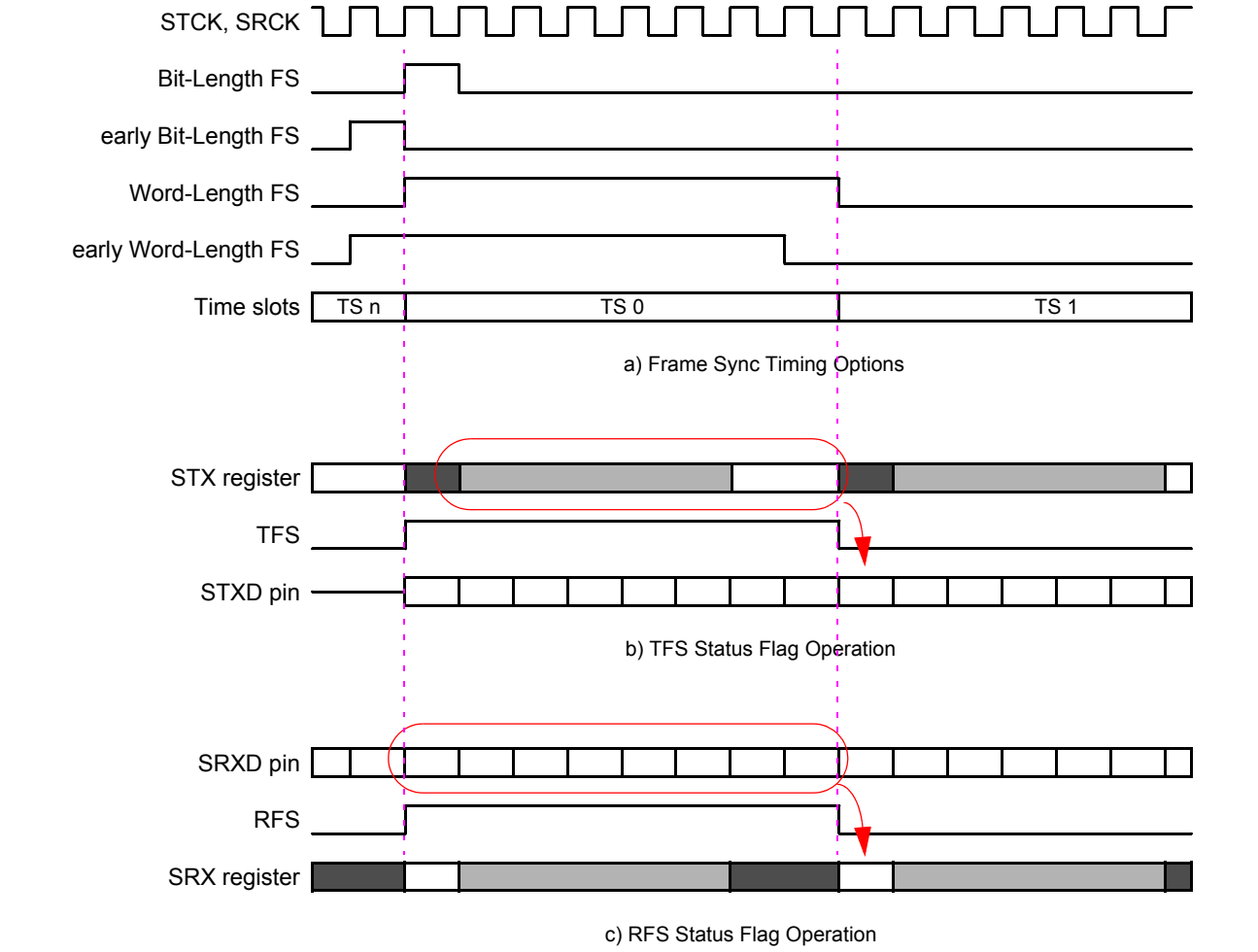


Figure 60. Frame Sync Timing Options

7.4.5.2.9 SSI Control Register 2 (SCR2)

The SSI Control Register 2 (SCR2) is one of three 16-bit control registers that select the operating mode for the SSI.

Interrupt enable bits for the receive and transmit sections are provided in this control register. Before they can function, the chip level interrupt priority register (IPR) must be set to enable SSI interrupts.

Power-on reset clears all SCR2 bits. However, SSI reset does not affect the SCR2 bits. The SCR2 bits are described in the following sections.

Base + 0x06

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	RIE	TIE	RE	TE	RFEN	TFEN	RXDIR	TXDIR	SYN	TSH-FD	TSCKP	SS-IEN	NET	TFSI	TFSL	TEFS
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 61. SCR2 Register Diagram

RIE—Receive Interrupt Enable

This control bit allows interrupting the program controller. When the RIE and RE bit are set, the program controller is interrupted when the SSI receives data. As shown in Table 42, the interrupt trigger depends on whether the receive FIFO is enabled or not.

If the receive FIFO is disabled:

1 = An interrupt is generated when the RDR flag (in the SCSR) is set
One value can be read from the SRX register. Reading the SRX register clears the RDR bit, thus clearing the interrupt

0 = No interrupt is generated

If the receive FIFO is enabled:

1 = An interrupt is generated when the RFF flag (in the SCSR) is set
A maximum of eight values are available to be read from the SRX register. Reading the SRX register to remove data from the receive FIFO such that the level falls below the watermark clears the RFF bit, thus clearing the interrupt.

0 = No interrupt is generated

Two receive data interrupts with separate interrupt vectors are available: receive data with exception status, and receive data without exception. Table 42 shows these vectors and the conditions under which these interrupts are generated.

Table 42. SSI Receive Data Interrupts[1]

Interrupt	RIE	Selection Control		ROE
		RFEN = 0	RFEN = 1	
Receive Data with Exception Status	1	RDR = 1	RFF = 1	1
Receive Data (without exception)	1	RDR = 1	RFF = 1	0

1.See Table 37 for a complete list of interrupts.

TIE—Transmit Interrupt Enable

This control bit allows interrupting the program controller. When the TIE and TE bits are set, the program controller is interrupted when the SSI needs more transmit data. As shown in Table 43, the interrupt trigger depends on whether the transmit FIFIO is enabled or not.

If the transmit FIFO is disabled:

1 = An interrupt is generated when the TDE flag (in the SCSR) is set
One value can be written to the STX register when this interrupt occurs.

0 = No interrupt is generated

If the transmit FIFO is enabled:

1 = An interrupt is generated when the TFE flag (in the SCSR) is set
When this interrupt occurs, up to eight values can be written to the STX, depending on the level of the TXFIFO watermark.

0 = No interrupt is generated

The TDE bit always indicates the STX register empty condition, even when the transmitter is disabled by the transmit enable (TE) bit in the SCR2. Writing data to the STX or STSR clears the TDE bit, thus clearing the interrupt. Two transmit data interrupts with separate interrupt vectors are available: transmit data with exception status and transmit data without exceptions. Table 43 shows the conditions under which these interrupts are generated and lists the interrupt vectors.

Table 43. SSI Transmit Data Interrupts[1]

Interrupt	TIE	Selection Control		TUE
		TFEN = 0	TFEN = 1	
Transmit Data with Exception Status	1	TDE = 1	TFE = 1	1
Transmit Data (without exception)	1	TDE = 1	TFE = 1	0

1.See Table 37 for a complete list of interrupts.

RE—Receive Enable

This control bit enables the receive portion of the SSI.

1 = Receive portion of the SSI is enabled and receive data will be processed starting with the next receive frame sync

0 = Receiver is disabled by inhibiting data transfer into the SRX
If data is being received when this bit is cleared, the rest of the word is not shifted in nor is it transferred to the SRX register. If the RE bit is re-enabled during a time slot before the second to last bit, then the word will be received.

It is recommended to clear this bit when clearing SSIEN.

TE—Transmit Enable

This control bit enables the transfer of the contents of the STX register to the transmit shift register (TXSR) and also enables the internal gated clock.

1 = On the next frame boundary, the transmit portion of the SSI is enabled.
With internally generated clocks, the frame boundary will occur within a word time. If the TE bit is cleared and then set again during the same transmitted word, the data continues to be transmitted. If the TE bit is set again during a different time slot, data is not transmitted until the next frame boundary.

0 = Transmitter continues to send the data currently in the TXSR and then disables the transmitter.
The serial output enable signal is disabled and any data present in the STX register is not transmitted. In other words, data can be written to the STX register with the TE bit cleared, and the TDE bit is cleared but data is not transferred to the TXSR.

The normal transmit enable sequence is to write data to the STX register or to the STSR before setting the TE bit. The normal transmit disable sequence is to clear the TE bit and the TIE bit after the TDE bit is set.

When an internal gated clock is being used, the gated clock runs during valid time slots if the TE bit is set. If the TE bit is cleared, the transmitter continues to send the data currently in the TXSR until it is empty. Then the clock stops. When the TE bit is set again, the gated clock starts immediately and runs during any valid time slots.

This bit should be cleared when clearing SSIEN.

RFEN—Receive FIFO Enable

This control bit enables the FIFO register for the receive section.

1 = Allows for eight samples (depending on the receive watermark set in the SFCSR) to be received by the SSI (a ninth sample can be shifting in) before the RFF bit is set and an interrupt request generated when enabled by the RIE bit.

0 = FIFO register is not used, and an interrupt request is generated when a single sample is received by the SSI (interrupts need to be enabled).

TFEN—Transmit FIFO Enable

This control bit enables the FIFO register for the transmit section.

1 = A maximum of eight samples can be written to the STX (a ninth sample can be shifting out)

0 = FIFO register is not used.

RXDIR—Receive Clock Direction

This control bit selects the direction and source of the clock signal used to clock the receive shift register (RXSR).

1 = Clock is generated internally and output to the SRCK pin.

0 = Internal clock generator is disconnected from the SRCK pin and an external clock source can drive this pin to clock the RXSR.

Table 44 shows the clock pin configuration options.

NOTE:

RXDIR and SYN must both be high for the SSI to be in gated clock mode.

Table 44. Clock Pin Configuration

SYN	RXDIR	TXDIR	RFDIR	TFDIR	SRFS	STFS	SRCK	STCK
Asynchronous Mode								
0	0	0	0	0	RFS in	TFS in	RCK in	TCK in
0	0	1	0	1	RFS in	TFS out	RCK in	TCK out
0	1	0	1	0	RFS out	TFS in	RCK out	TCK in
0	1	1	1	1	RFS out	TFS out	RCK out	TCK out
Synchronous Mode								
1	0	0	x	0	GPIO	FS in	GPIO	CK in
1	0	1	x	1	GPIO	FS out	GPIO	CK out
1	1	0	x	x	GPIO	GPIO	GPIO	Gated in
1	1	1	0	x	GPIO	GPIO	GPIO	Gated out

TXDIR—Transmit Clock Direction

This control bit selects the direction and source of the clock used to clock the TXSR.

1 = Clock is generated internally and is output to the STCK pin.

0 = Internal clock generator is disconnected from the STCK pin and an external clock source can drive this pin to clock the TXSR.

Table 44 shows the clock configuration options.

SYN—Synchronous Mode

This control bit enables the synchronous mode of operation. In this mode, the transmit and receive sections share a common clock pin and frame sync pin.

SYN and RXDIR control gated clock mode. The SSI is in gated clock mode when both SYN and RXDIR are high.

Table 44 shows the clock configuration options.

TSHFD—Transmit Shift Direction

This bit controls whether the MSB or LSB is transmitted first for the transmit section.

1 = LSB is transmitted first.

0 = Data is transmitted MSB first.

NOTE:

The CODEC device labels the MSB as bit 0, whereas the SSI labels the LSB as bit 0. Therefore, when using a standard CODEC, the SSI MSB (or CODEC bit 0) is shifted out first, and the TSHFD bit should be cleared.

TSCKP—Transmit Clock Polarity

This control bit determines which bit clock edge is used to clock out data in the transmit section.

1 = Falling edge of the bit clock is used to clock the data out.

0 = Data is clocked out on the rising edge of the bit clock.

SSIEN—SSI Enable

This control bit enables and disables the SSI.

1 = SSI is enabled.

When enabled, causes an output frame sync to be generated when set up for internal frame sync or causes the SSI to wait for the input frame sync when set up for external frame sync.

0 = SSI is disabled and held in a reset condition.

When disabled, all output pins are tri-stated, the status register bits are preset to the same state produced by the power-on reset, and the control register bits are unaffected. The contents of the STX, TXFIFO, and RXFIFO are cleared when this bit is reset. When SSI is disabled, all internal clocks are disabled except clocks required for register access. When clearing SSIEN, it is recommended to also clear RE and TE.

NET—Network Mode

This control bit selects the operational mode of the SSI.

1 = Network mode is selected.

0 = Normal mode is selected.

TFSI—Transmit Frame Sync Invert

This control bit selects the logic of frame sync I/O.

1 = Frame sync is active low.

0 = Frame sync is active high.

TFSL—Transmit Frame Sync Length

This control bit selects the length of the frame sync signal to be generated or recognized. See Figure 60 for an example timing diagram of the FS options.

1 = A one-clock-bit-long frame sync is selected.

0 = A one-word-long frame sync is selected.

The length of this word-long frame sync is the same as the length of the data word selected by WL[1:0].

The frame sync is deasserted after one bit for bit length frame sync and after one word for word length frame sync.

TEFS—Transmit Early Frame Sync

This bit controls when the frame sync is initiated for the transmit and receive sections. See Figure 60 for an example timing diagram of the FS options.

1 = Frame sync is initiated one bit before the data is transmitted.
The frame sync is disabled after one bit-for-bit length frame sync and after one word-for-word length frame sync.

0 = Frame sync is initiated as the first bit of data is transmitted.

7.4.5.2.10 SSI Time Slot Register (STSR)

The STSR is used when data is not to be transmitted in an available transmit time slot. For the purposes of timing, the time slot register is a write-only register that behaves like an alternate transmit data register, except that instead of transmitting data, the STXD signal is tri-stated. Using this register is important for avoiding overflow/underflow during inactive time slots.

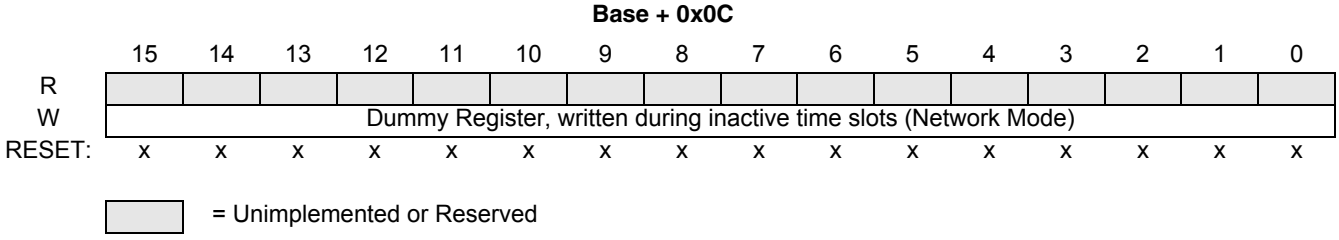


Figure 62. STSR Register Diagram

7.4.5.2.11 SSI FIFO Control/Status Register (SFCSR)

This register provides for configuration of the transmit and receive FIFO registers and allows for reporting of the amount of data contained in each FIFO.

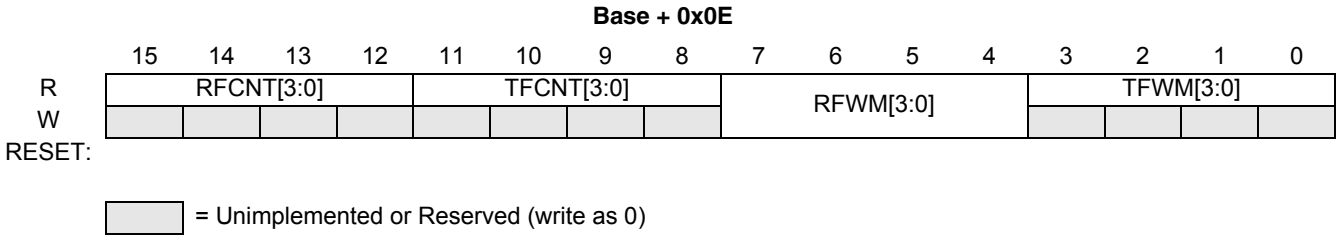


Figure 63. SFCSR Register Diagram

RFCNT[3:0]—Receive FIFO Counter

This read-only bit field indicates the number of data words in the RXFIFO. Table 45 shows the RFCNT[3:0] bit field encoding.

Table 45. RFCNT[3:0] Encoding

Bits	Description
0000	0 data words in RXFIFO
0001	1 data words in RXFIFO
0010	2 data words in RXFIFO
0011	3 data words in RXFIFO
0100	4 data words in RXFIFO
0101	5 data words in RXFIFO

Table 45. RFCNT[3:0] Encoding (Continued)

Bits	Description
0110	6 data words in RXFIFO
0111	7 data words in RXFIFO
1000	8 data words in RXFIFO

TFCNT[3:0]—Transmit FIFO Counter

This read-only bit field indicates the number of data words in the TXFIFO. Table 46 shows the TFCNT[3:0] bit field encoding.

Table 46. TFCNT[3:0] Encoding

Bits	Description
0000	0 data words in TXFIFO
0001	1 data words in TXFIFO
0010	2 data words in TXFIFO
0011	3 data words in TXFIFO
0100	4 data words in TXFIFO
0101	5 data words in TXFIFO
0110	6 data words in TXFIFO
0111	7 data words in TXFIFO
1000	8 data words in TXFIFO

RFWM[3:0]—Receive FIFO Full WaterMark

This bit field controls the threshold at which the receive FIFO full flag (RFF) will be set. RFF is set whenever the data level in the RXFIFO reaches the selected threshold. For example, if RFWM=1, RFF will be set after the SSI received 2 data words (one in SRX and the other in RXFIFO). Table 47 shows RFWM[3:0] bit field encoding and Table 48 shows the status of RFF for all data levels of the RXFIFO.

Table 47. RFWM[3:0] Encoding

Bits	Description
0000	Reserved
0001	RFF set when at least one data word has been written to the RXFIFO. Set when RXFIFO = 1, 2, 3, 4, 5, 6, 7, or 8 data words
0010	RFF set when 2 or more data words have been written to the RXFIFO. Set when RXFIFO = 2, 3, 4, 5, 6, 7, or 8 data words
0011	RFF set when 3 or more data words have been written to the RXFIFO. Set when RXFIFO = 3, 4, 5, 6, 7, or 8 data words
0100	RFF set when 4 or more data words have been written to the RXFIFO. Set when RXFIFO = 4, 5, 6, 7, or 8 data words
0101	RFF set when 5 or more data words have been written to the RXFIFO. Set when RXFIFO = 5, 6, 7, or 8 data words
0110	RFF set when 6 or more data words have been written to the RXFIFO. Set when RXFIFO = 6, 7, or 8 data words
0111	RFF set when 7 or more data words have been written to the RXFIFO. Set when RXFIFO = 7 or 8 data words
1000	RFF set when 8 data words have been written to the RXFIFO. Set when RXFIFO = 8 data words

Table 48. Status of Receive FIFO Full Flag

Receive FIFO Watermark (RFWM)	Number of data in RXFIFO								
	0	1	2	3	4	5	6	7	8
1	0	1	1	1	1	1	1	1	1
2	0	0	1	1	1	1	1	1	1
3	0	0	0	1	1	1	1	1	1
4	0	0	0	0	1	1	1	1	1
5	0	0	0	0	0	1	1	1	1
6	0	0	0	0	0	0	1	1	1
7	0	0	0	0	0	0	0	1	1
8	0	0	0	0	0	0	0	0	1

TFWM[3:0]—Transmit FIFO Empty WaterMark

This bit field controls the threshold at which the transmit FIFO empty flag (TFE) is set. TFE is set whenever the data level in the TXFIFO falls below the selected threshold. Table 49 shows TFWM[2:0] bit field encoding and Table 50 shows the status of TFE for all data levels of the TXFIFO.

Table 49. TFWM[3:0] Encoding

Bits	Description
0000	Reserved
0001	TFE set when there is 1 empty slot in TXFIFO (default). Transmit FIFO empty is set when TXFIFO <= 7 data.
0010	TFE set when there are 2 or more empty slots in TXFIFO. Transmit FIFO empty is set when TXFIFO <= 6 data.
0011	TFE set when there are 3 or more empty slots in TXFIFO. Transmit FIFO empty is set when TXFIFO <= 5 data.
0100	TFE set when there are 4 or more empty slots in TXFIFO. Transmit FIFO empty is set when TXFIFO <= 4 data.
0101	TFE set when there are 5 or more empty slots in TXFIFO. Transmit FIFO empty is set when TXFIFO <= 3 data.
0110	TFE set when there are 6 or more empty slots in TXFIFO. Transmit FIFO empty is set when TXFIFO <= 2 data.
0111	TFE set when there are 7 or more empty slots in TXFIFO. Transmit FIFO empty is set when TXFIFO = 1 data.
1000	TFE set when there are 8 empty slots in TXFIFO. Transmit FIFO empty is set when TXFIFO = 0 data.

Table 50. Status of Transmit FIFO Empty Flag

Transmit FIFO Watermark (TFWM)	Number of data in TXFIFO								
	0	1	2	3	4	5	6	7	8
1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	1	1	0	0
3	1	1	1	1	1	1	0	0	0
4	1	1	1	1	1	0	0	0	0
5	1	1	1	1	0	0	0	0	0
6	1	1	1	0	0	0	0	0	0
7	1	1	0	0	0	0	0	0	0

Table 50. Status of Transmit FIFO Empty Flag (Continued)

Transmit FIFO Watermark (TFWM)	Number of data in TXFIFO								
	0	1	2	3	4	5	6	7	8
8	1	0	0	0	0	0	0	0	0

7.4.5.2.12 SSI Test Register (STR)

This register controls test features and is not normally used.

Base + 0x10

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	TEST	RCK2 TCK	RFS2 TFS	RXSTATE[4:0]					TXD2 RXD	TCK2 RCK	TFS2 RFS	TXSTATE[4:0]				
W																
RESET:	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

= Unimplemented or Reserved

Figure 64. STR Register Diagram

TEST—SSI Test Features
1 = SSI test features enabled.
0 = SSI test features disabled.

RCK2TCK—Receive Clock to Transmit Clock Loop Back
1 = Enables RX_CLK loop back to RX_CLK.
0 = Loop back is disabled.

RFS2TFS—Receive Frame to Transmit Frame Loop Back
1 = Enables RX_FRM loop back to TX_FRM.
0 = Loop back is disabled.

RXSTATE[4:0]—Receiver State Machine Status
These bit field indicates the receiver state machine status. These bits are used for test purpose only.

TXD2RXD—Transmit Data to Receive Data Loop Back
1 = Enables TXD loop back to RXD.
0 = Loop back is disabled.

TCK2RCK—Transmit Clock to Receive Clock Loop Back
1 = Enables TX_CLK loop back to RX_CLK.
0 = Loop back is disabled.

TFS2RFS—Transmit Frame to Receive Frame Loop Back
1 = Enables TX_FRM loop back to RX_FRM.
0 = Loop back is disabled.

TXSTATE[4:0]—Transmitter State Machine Status
This bit field indicates the transmitter state machine status. These bits are used for test purposes only.

7.4.5.2.13 SSI Option Register (SOR)

Base + 0x12

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									Reserved (write as 0)		RFDIR	TFDIR	INIT	WAIT[1:0]		SYN RST
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 65. SOR Register Diagram

RFDIR—Receive Frame Direction

This control bit selects the direction and source of the receive frame sync signal.

1 = Receive frame sync is generated internally and output to the SRFS pin.

0 = Receive frame sync is external, meaning that the receive frame sync is supplied from an external source.

TFDIR—Transmit Frame Direction

This control bit selects the direction and source of the transmit frame sync signal.

1 = Transmit frame sync is generated internally and output to the STFS pin.

0 = Transmit frame sync is external, meaning that the transmit frame sync is supplied from an external source.

INIT—Initialize State Machine

This bit is used to initialize the state machine to reset state.

1 = Reset the TX and RX state machines.
Setting this bit must be followed by a write of zero before the state machine with operate.

0 = State machine is allowed to operate.

WAIT[1:0]—Wait State

This bit field controls the number of wait states to be added to the transaction between the CPU and SSI. The MC72000 does not use wait states and as such these should always be written 0.

SYNRST—Frame Sync Reset

1 = Resets the accumulation of data in SRX and RXFIFO on frame synchronization.

0 = Data must be read to be cleared from the registers.

7.4.5.2.14 Transmit Slot Mask Registers (TSMA, TSMB)

Base + 0x14

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	TSMA[15:0]															
W																
RESET:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

= Unimplemented or Reserved

Figure 66. TSMA Register Diagram

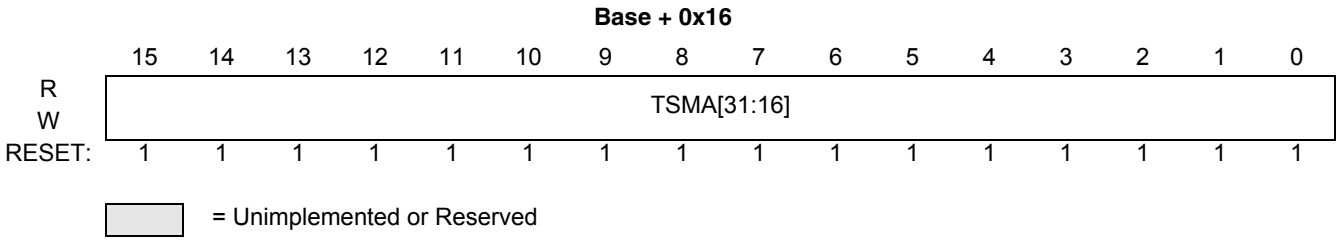


Figure 67. TSMB Register Diagram

The transmit slot mask registers are two 16-bit read/write registers. In network mode, these registers are used by the transmitter to determine which action to take in the current transmission slot. Depending on the setting of the bits, the transmitter either tri-states the transmitter data signal or transmits a data word and generates the appropriate transmit status.

TSMA and TSMB can be viewed as a single 32-bit register, TSM. Bit n in TSM (TSMn) is an enable/disable control bit for transmission in slot number N.

1 = Transmit sequence proceeds normally.
Data is transferred from the STX register (or TXFIFO, if enabled) to the shift register during slot number N and flags are set appropriately.

0 = Transmit data signal of the transmitter is tri-stated during transmit time slot number N.
Data is not transferred to the TXSR and, therefore, transmit status flags are not changed.

The DSP is interrupted only for enabled slots. Data written to the STX register when the transmitter empty (or transmit FIFO empty) interrupt request is being serviced is transmitted in the next enabled transmit time slot.

The TSM slot mask does not conflict with the STSR. Even if a slot is enabled in the TSM, the user may choose to write to the STSR to tri-state the signals of the enabled transmitters during the next transmission slot. Setting the bits in the TSM affects the next frame transmission. The frame currently being transmitted is not affected by the new TSM setting. If the TSM is read, it shows the current setting.

After a hardware RESET signal or executing a DSP software RESET instruction, the TSM register is reset to $FFFFFFFF; that value enables all 32 slots for data transmission. The transmit DC setting determines how many of these control bits are actually used.

7.4.5.3 Receive Slot Mask Registers (RSMA, RSMB)

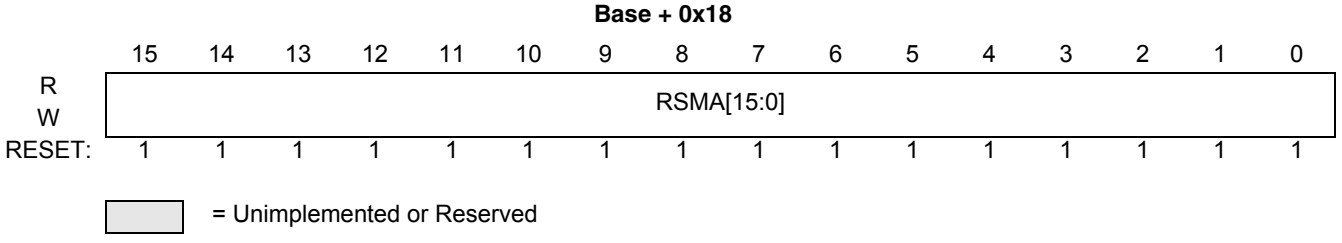


Figure 68. RSMA Register Diagram

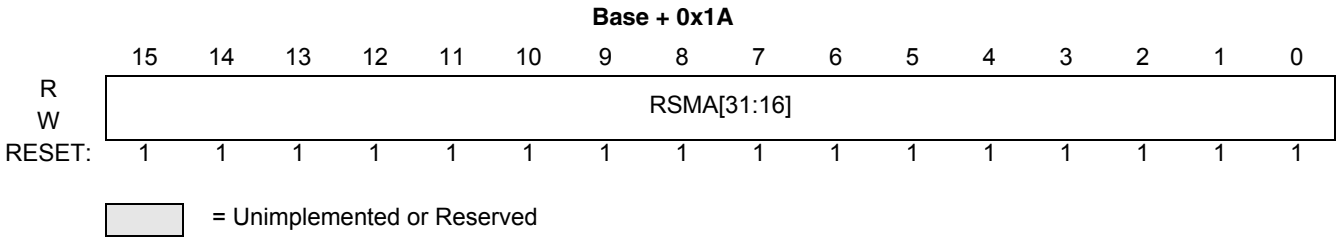


Figure 69. RSMB Register Diagram

The receive slot mask registers are two 16-bit read/write registers. In network mode, these registers are used by the receiver to determine which action to take in the current time slot. Depending on the setting of the bits, the receiver either ignores the receiver data signal(s) or receives a data word and generates the appropriate receive status.

RSMA and RSMB can be viewed as one 32-bit register, RSM. Bit n in RSM (RSMn) is an enable/disable control bit for time slot number N.

1 = Receive sequence proceeds normally.
Data is received during slot number N, and the RDR flag is set.

0 = Data is not transferred from the receive shift register (RXSR) to the receive data register (SRX) and, therefore, the RDR and ROE flags are not set.

During a disabled slot, no receiver full interrupt is generated. The DSP is interrupted only for enabled slots.

When the bits in the RSM are set, their settings affect the next frame reception. The frame currently being received is not affected by the new RSM setting. If the RSM is read, it shows the current setting.

After a hardware RESET signal or executing a DSP software RESET instruction, the RSM register is reset to $FFFFFFFF; that value enables all 32 time slots for data reception. The receive DC setting determines how many of these control bits are actually used.

7.4.5.3.1 SSI Frame Status Register (SFSR)

This register can be read at any time to determine the current time slot of the frame. This register is only useful for network mode.

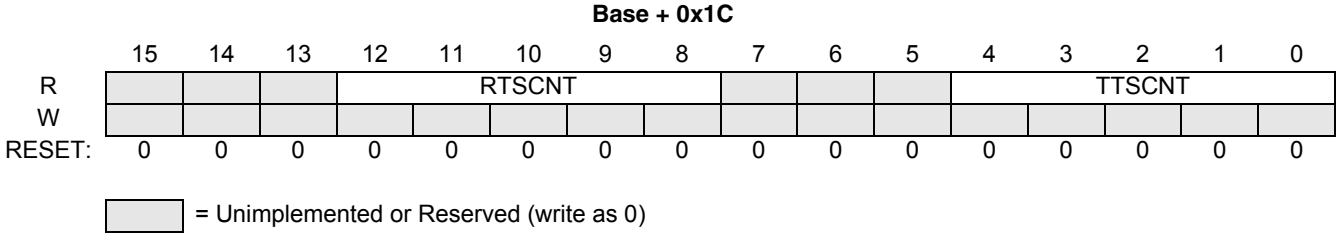


Figure 70. SFSR Register Diagram

RTSCNT — Receive Time-Slot Count

This read-only bit field indicates the current time-slot number within the receive frame. This count will indicate the specific bit of the RSM that is currently active. The value of this field will change with the receive word count clock (see Figure 78).

TTSCNT — Transmit Time-Slot Count

This read-only field indicates the current time-slot number within the transmit frame. This count will indicate the specific bit of the TSM that is currently active. The value of this field will change with the transmit word count clock (see Figure 77).

7.4.6 Functional Description

7.4.6.1 General

The SSI has two basic operating modes. Table 51 lists these operating modes and some of the typical applications in which they can be used. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices. These modes can be programmed by several bits in the SSI control registers (see Section 7.4.5.2, “Register Descriptions”).

Table 51. SSI Operating Modes

TX, RX Sections[1]	Serial Clock[2]	Mode[3]	Typical Application
Asynchronous	Continuous	Normal	Multiple synchronous CODECs (No Support)
Asynchronous	Continuous	Network	TDM CODEC or DSP networks (No Support)
Synchronous	Continuous	Normal	Multiple synchronous CODECs
Synchronous	Continuous	Network	TDM CODEC or DSP network
Synchronous	Gated[4]	Normal	SPI-type devices; DSP to MCU

1. In synchronous mode, the transmitter and receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver operate independently, on their own clocks and frame syncs.
2. In continuous mode the clocks run all the time. In gated clock mode, the clock operates only when there is data to exchange.
3. In normal mode, the SSI only transmits during the first time-slot of each I/O frame. In network mode, any number from 1 to 32 data words of I/O per frame can be used. Network mode is typically used in star or ring time division multiplex networks with other processors or CODECs, allowing interface to TDM networks without additional logic.
4. Use of gated clock is not allowed in network mode.

The SSI supports both normal and network modes, and these can be selected independently of whether the transmitter and receiver are synchronous or asynchronous. Typically, these protocols are used in a periodic manner, where data is transferred at regular intervals, such as at the sampling rate of an external CODEC. Both modes use the concept of a frame. The beginning of the frame is marked with a frame sync when programmed with continuous clock. The frame sync occurs at a periodic interval. The length of the frame is determined by the DC[4:0] and WL[1:0] bits in either the SRXCR or STXCR register, depending on whether data is being transmitted or received.

7.4.6.1.1 Normal Mode

Normal mode is the simplest mode of the SSI. It is used to transfer one word per frame. In continuous clock mode, a frame sync occurs at the beginning of each frame. The length of the frame is determined by the following factors:

- The period of the serial bit clock (PSR, PM[7:0] bits for internal clock or the frequency of the external clock on the STCK or SRCK pin).
- The number of bits per sample (WL[1:0] bits).
- The number of time slots per frame (DC[4:0] bits).

If normal mode is configured to provide more than one time slot per frame, data is transmitted only in the first time slot. No data is transmitted in subsequent time slots. Figure 71 and Figure 72 show sample timing of normal mode transfers.

7.4.6.1.1.1 Normal Mode Transmit

The conditions for data transmission from the SSI in normal mode are as follows:

1. Set the SCSR, STXCR, SCR2, and SOR registers to select normal mode operation, define the transmit clock, transmit frame sync, and frame structure required for proper system operation.
2. Enable SSI enabled (SSIEN = 1).
3. Enable TXFIFO (TFEN=1) and configure the transmit watermark (TFWM=n) if this TXFIFO is used.
4. Write data to transmit data register (STX).
5. Enable transmit interrupts.
6. Set the TE bit (TE = 1) to enable the transmitter on the next frame sync boundary.

Figure 71 and Table 52 describe the functions performed during transmit operation in this mode.

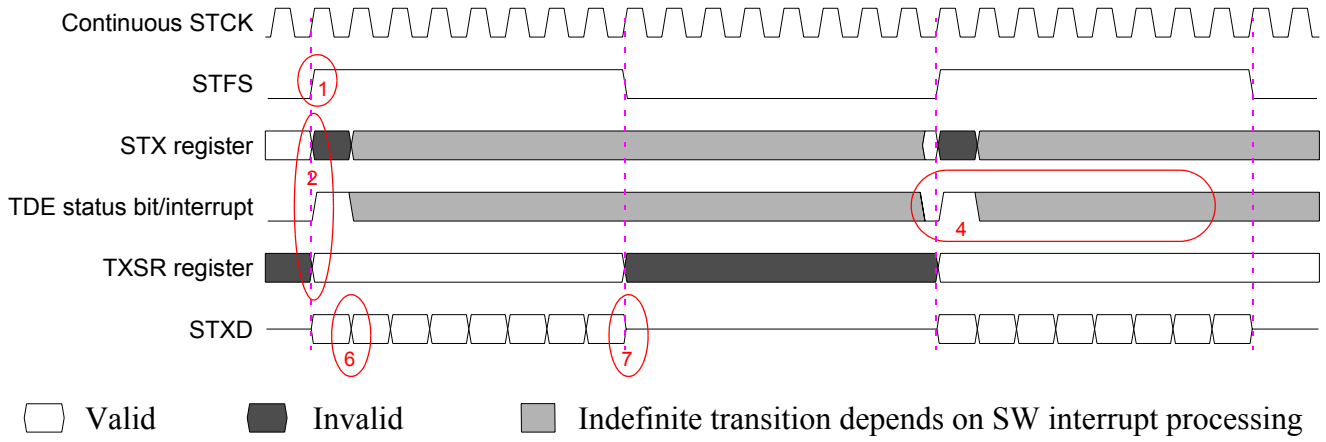


Figure 71. Normal Mode Transmit Timing—Continuous Clock (WL=8-bit words, DC=1)

Table 52. Normal Mode Transmit Operations

Step		TXFIFO Disabled (See Figure 71)	TXFIFO Enabled (No Figure Available)
1	Rising edge of STFS *Note: A word length frame sync is shown. This only works if DC>0.*		
2	Data transferred to TXSR	From STX	From TXFIFO
3	STXD output pin is enabled[1] and the first bit of the TXSR register appears on the output		
4	Flag status update	The TDE bit is set	The TFE bit is set if the level of data in the TXFIFO falls below the watermark level

Table 52. Normal Mode Transmit Operations

Step		TXFIFO Disabled (See Figure 71)	TXFIFO Enabled (No Figure Available)
5	If the TIE bit is set, enabling transmit interrupts, then: (Other options for processing the data transfer are either polling or DMA transfers.)	Transmit interrupt occurs when TDE set	Transmit interrupt occurs when TFE set
6	The TXSR is shifted on the next rising edge of STCK and the next bit appears on the STXD pin		
7	When WL bits (see Section 7.4.5.2.7, “SSI Transmit and Receive Control Registers (STXCR, SRXCR)”) have been sent, the STXD is tri-stated		
8	Transmit under-run (setting the TUE bit of the SCSR register) is prevented by[2]:	New data is written to the STX before the TXSR tries to obtain new transmit data at the next frame sync	New data is written to the STX before the TXSR tries to obtain data from an empty TXFIFO (this can be several frame times)
9	Repeat at step 1 on the next frame sync[3]		

1.The STXD output signal is disabled except during the data transmission period.
2.See the description of the TUE bit in Section 7.4.5.2.8, “SSI Control/Status Register (SCSR),” for a description of what happens when the TUE bit is set.
3.The frame sync must not occur earlier than what is configured in the STXCR as documented in Section 7.4.5.2.7, “SSI Transmit and Receive Control Registers (STXCR, SRXCR).”

7.4.6.1.1.2 Normal Mode Receive

The conditions for data reception from the SSI are as follows:

1. Set the SCSR, SRXCR, SCR2, and SOR registers to select normal mode operation, define the receive clock, receive frame sync and frame structure required for proper system operation.
2. Enable SSI (SSIEN = 1).
3. Enable RXFIFO (RFEN=1) and configure receive watermark (RFWM=n) if RXFIFO is used.
4. Enable receive interrupts.
5. Set the RE bit (RE = 1) to enable the receiver operation on the next frame sync boundary.

Figure 72 and Table 53 describes the functions performed during receive operation in this mode.

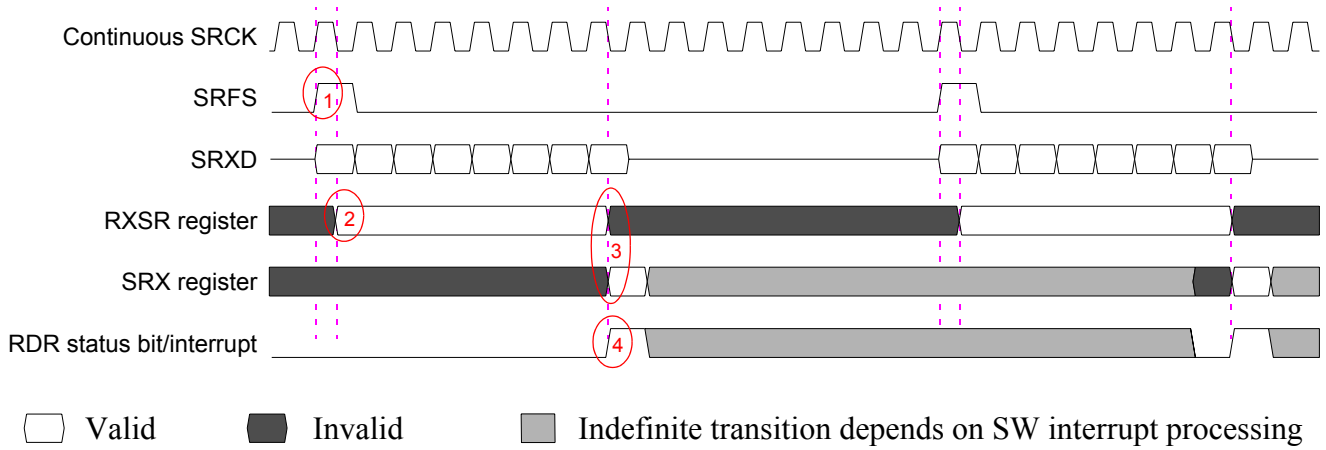


Figure 72. Normal Mode Receive Timing—Continuous Clock (WL=8-bit words, DC=1)

Table 53. Normal Mode Receive Operations

Step		RXFIFO Disabled (See Figure 72)	RXFIFO Enabled (No Figure Available
1	Leading edge of frame sync occurs on the SRFS pin		
2	Falling edge of receive clock occurs on the SRCK pin and the next bit of data is shifted into the RXSR register		
3	When WL bits (see Section 7.4.5.2.7, “SSI Transmit and Receive Control Registers (STXCR, SRXCR)”) have been received RXSR contents are transferred to the SRX register on the next falling edge of the receive clock *Note: The SRX register is actually loaded during the middle of the last receive bit.*		
4	Flag status update	The RDR bit is set	The RFF bit is set if the level of data in the RXFIFO rises above the watermark level
5	If the RIE bit is set, enabling receive interrupts, then: (Other options for processing the data transfer is either polling or DMA transfers.)	Receive interrupt occurs when RDR set	Receive interrupt occurs when RFF set
6	Receive over-run (setting the ROE bit of the SCSR register) is prevented by[1]:	Data is read from the SRX before the RXSR tries to write new transmit data at the next frame sync	Data is read from the SRX before the RXSR tries to provide more data to a full RXFIFO (it can take several frame times to fill the RXFIFO)
7	Repeat at step 1 on the next frame sync[2]		

1.See the description of the ROE bit in Section 7.4.5.2.8, “SSI Control/Status Register (SCSR)” for a description of what happens when the ROE bit is set.
2.The frame sync must not occur earlier than what is configured in the SRXCR as documented in Section 7.4.5.2.7, “SSI Transmit and Receive Control Registers (STXCR, SRXCR).”

7.4.6.1.1.3 Gated Clock Operation

Gated clock mode is often used to hook up to SPI-type interfaces on microcontroller units (MCUs) or external peripheral chips. In gated clock mode, the presence of the clock indicates that valid data is on the STXD or SRXD pins. For this reason, no frame sync is needed in this mode. Once transmission of data has completed, the clock is stopped.

Since gated clock mode is a synchronous mode (see Table 51), only the STCK is used. This clock can be generated internally (master mode) or externally (slave mode). Several operating modes are possible as detailed in Table 54.

Table 54. Transmit and Receive Enables in Gated Clock Mode

Enables		Possible Clock Source	Operating Mode
TE	RE		
0	0		Not operational
0	1	External	Receive only -- receiver gets data when clocks occur
1	0	Internal or external	Transmit only -- data transfer as clocks occur
1	1	Internal or external	Transmit and receive operate synchronously -- data is transferred as clocks occur

For the case of internally generated clock, all internal bit clocks, word clocks, and frame clocks continue to operate (although frame clock is ignored). When data is written to the STX register, the clock will operate starting when the next word clock (time-slot) occurs. This allows data to be transferred out in periodic intervals in gated clock mode.

With an external clock, the SSI waits for a clock signal to be received. Once the clock begins, valid data is shifted in/out.

NOTE:

The bit clock pins must be kept free of timing glitches. If a single glitch occurs, all ensuing transfers will be out of synchronization.

Figure 73 shows a gated clock timing diagram with comments in Table 55.

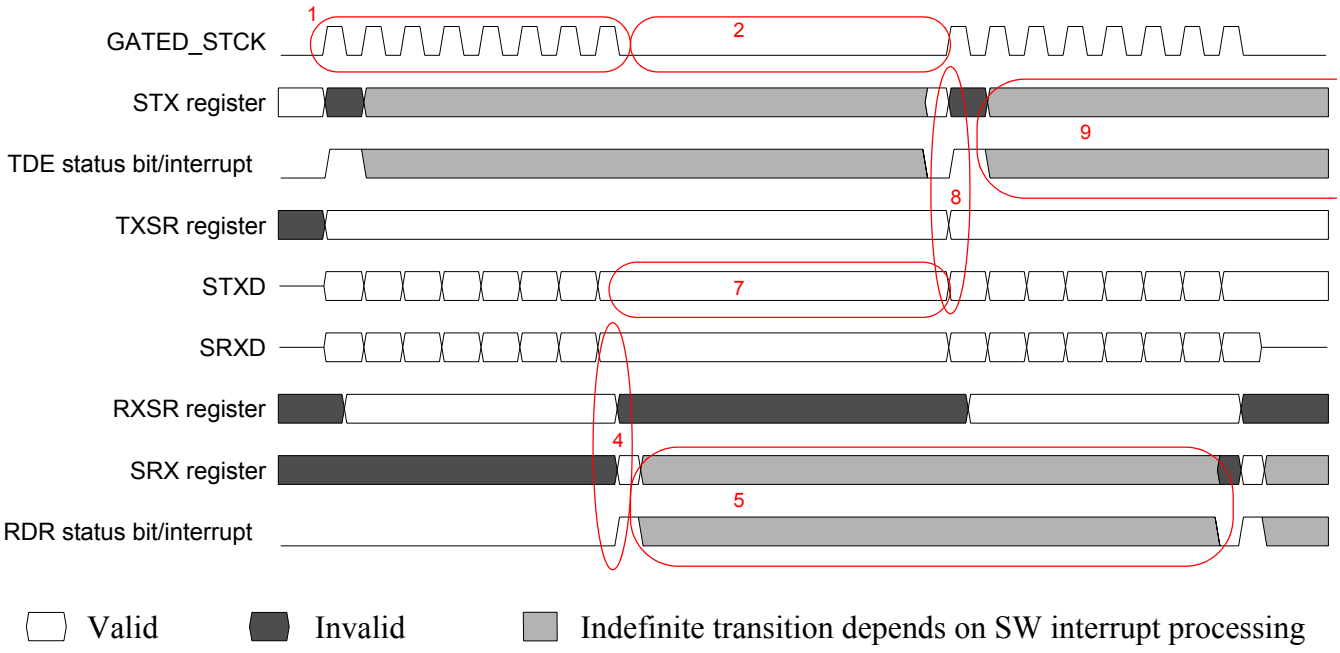


Figure 73. Normal Mode Timing—Gated Clock

Table 55. Gated Clock Operations

Step		FIFOs Disabled (See Figure 73)	FIFOs Enabled (No Figure Available
1	Clocks occur on STCK to clock data out on the STXD pin and in on the SRXD pin		
2	Clocks stop on STCK and no data is transferred *Note: The idle time is a multiple of word times, when the clock is generated internally.*		
3	All other timing of transmit and receive functions continue as in Normal mode		
4	Receive flag status update The last bit of the receive data is captured on the last falling clock edge before the clock is gated off. The receive interrupt does not occur at the same time as the transmit interrupt, if both are enabled.	The RDR bit is set	The RFF bit is set if the level of data in the RXFIFO rises above the watermark level
5	If the RIE bit is set, enabling receive interrupts, then: (Other options for processing the data is either polling or DMA transfers.)	Receive interrupt occurs when RDR set	Receive interrupt occurs when RFF set
6	Receive overrun (setting the ROE bit of the SCSR register) is prevented by[1]:	Data is read from the SRX before the RXSR tries to write new transmit data at the next frame sync	Data is read from the SRX before the RXSR tries to provide more data to a full RXFIFO (it can take several frame times to fill the RXFIFO)

Table 55. Gated Clock Operations (Continued)

Step		FIFOs Disabled (See Figure 73)	FIFOs Enabled (No Figure Available
7	At the end of the transmit word, the STXD pin continues to drive In the general case where STCK is driven externally, the transmitter does not know when the normal end of the list bit time is.		
8	Transmit status flag update	TDE bit is set	The TFE bit is set if the level of data in the TXFIFO falls below the watermark level
9	If the TIE bit is set, enabling transmit interrupts, then: (Other options for processing the data is either polling or DMA transfers.)	Transmit interrupt occurs when TDE set	Transmit interrupt occurs when TFE set
	Repeat at step 1 on the next frame sync[2]		

1.See the description of the ROE bit in Section 7.4.5.2.8, “SSI Control/Status Register (SCSR),” for a description of what happens when the ROE bit is set.

2.The frame sync must not occur earlier than what is configured in the SRXCR as documented in Section 7.4.5.2.7, “SSI Transmit and Receive Control Registers (STXCR, SRXCR).”

7.4.6.1.2 Network Mode

Network mode is used for creating a time division multiplexed (TDM) network, such as a TDM CODEC network or a network of DSPs. This mode only operates with continuous clock mode. A frame sync occurs at the beginning of each frame. In this mode, the frame is divided into more than one time slot. During each time slot, one data word can be transferred. Each time slot is then assigned to an appropriate CODEC or DSP on the network. The DSP can be a master device that controls its own private network, or a slave device that is connected to an existing TDM network and occupies a few time slots.

The frame sync signal indicates the beginning of a new data frame. Each data frame is divided into time slots and transmission and/or reception of one data word can occur in each time slot (rather than in just the frame sync time slot as in normal mode). The frame rate dividers, controlled by the DC[4:0] bits, select two to thirty-two time slots per frame. The length of the frame is determined by the following factors:

- The period of the serial bit clock (PSR, PM[7:0] bits for internal clock, or the frequency of the external clock on the STCK and/or SRCK pins).
- The number of bits per sample (WL[1:0] bits).
- The number of time slots per frame (DC[4:0] bits).

In network mode, data can be transmitted in any time slot. The distinction of the network mode is that each time slot is identified with respect to the frame sync (data word time). This time slot identification allows the option of transmitting data during the time slot by writing to the STX register or ignoring the time slot by writing to STSR. The receiver is treated in the same manner, except that data is always being shifted into the RXSR and transferred to the SRX register. The core reads the SRX register and either uses it or discards it.

Figure 74 and Figure 75 show sample timing of network mode transfers. The figures show receive and transmit frames of 5 time-slots for each. The numbered circles and arrows in the figure identify discussion notes which are contained in Table 56 and Table 57.

7.4.6.1.2.1 Network Mode Transmit

The transmit portion of the SSI is enabled when the SSIEN and the TE bits in the SCR2 are both set. However, when the TE bit is set, the transmitter is enabled only after detection of a new frame boundary. Software has to find the start of the next frame (by checking the TFS bit of the SCSR register). Do the following steps for a normal start-up sequence for transmission:

1. Set the SCSR, STXCR, SCR2, and SOR registers to select network mode operation, define the transmit clock, transmit frame sync, and frame structure required for proper system operation.
2. Enable SSI (SSIEN = 1).
3. Enable TXFIFO (TFEN=1) and configure the transmit watermark (TFWM=n) if this TXFIFO is used.
4. Write data to transmit data register (STX).
5. Enable transmit interrupts.
6. Set the TE bit (TE = 1) to enable the transmitter on the next frame sync boundary.

The transmitter timing for an 8-bit word with continuous clock, FIFO disabled, five words per frame sync, in network mode is shown in Figure 74. The explanatory notes for the transmit portion of the figure are shown in Table 56.

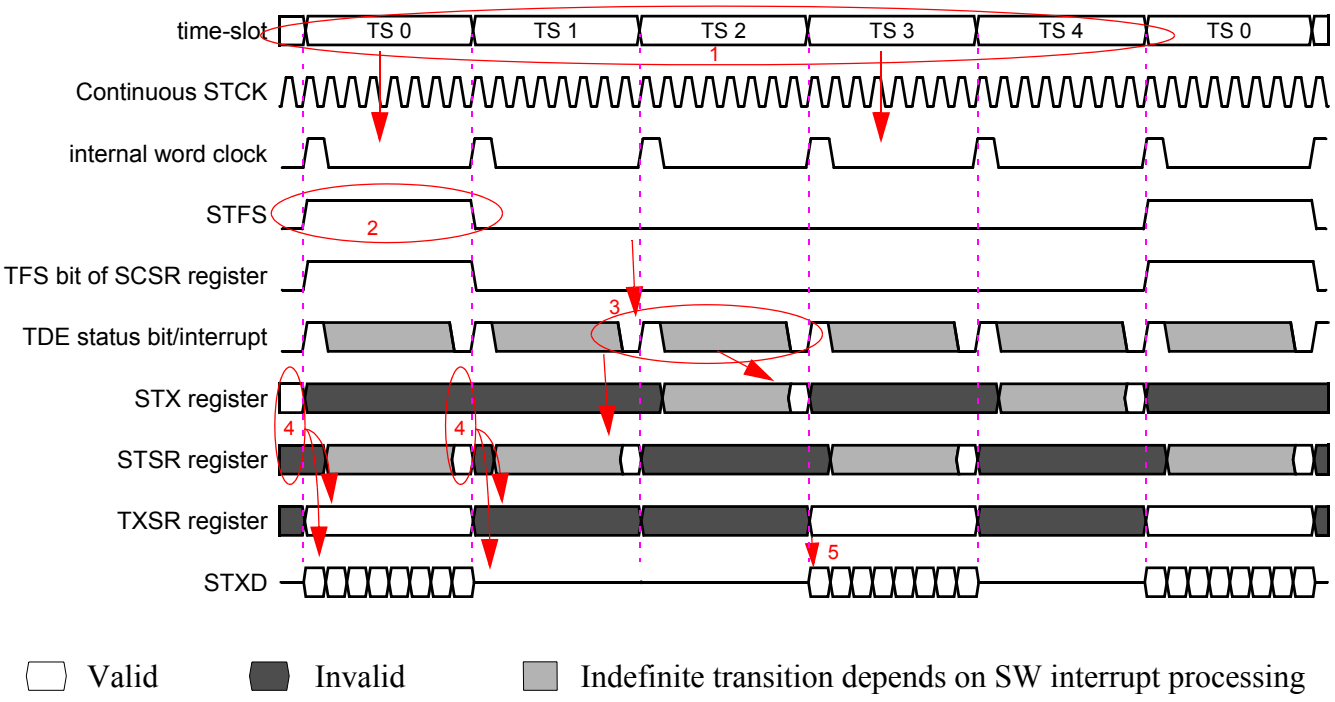


Figure 74. Network Mode Transmit Timing

Table 56. Notes for Transmit Timing in Figure 74

Note	Source Signal	Destination Signal	Description
1			Example of a 5 time-slot frame, transmitting in time-slots 0 and 3.
2	STFS		Example with word-length frame sync and standard timing (TFSI=0, TFSL=0, TEFS=0). Frame timing begins with the rising edge of STFS.
3		TDE status flag and interrupt	This flag is set at the beginning of each word to indicate that another data word should be supplied by the software. If the transmit interrupt is enabled, the processor is interrupted to request the data. The flag (and interrupt) are cleared when data is written to either the STX or STSR registers (see Section 7.4.9.2, “Description of Interrupt Operation” for a complete description of interrupt processing).
4	STX/STSR register	TXSR register	On each word clock boundary a decision is made concerning what to transmit on the next time-slot. If the STSR register was written during the previous time-slot, the STXD pin is tri-stated. If the STSR register was NOT written during the previous time-slot, the contents of the STX register is transferred to the TXSR register and this data is shifted out. If the STX register has not been written in the previous time-slot, the previous data is reused. If neither of these registers were written in the previous time-slot, the TUE status bit will be set and the hardware will operate as if the STX register had been written. The STXD pin will be enabled and the contents of the STX will be transmitted again. Note that this may lead to drive conflicts on the transmit data line.
5	TXSR register	STXD pin	On active time-slots, the TXSR register contents are shifted out on the STXD pin, one bit per rising edge of STCK. On inactive time-slots, the STXD pin is tri-stated so it can be driven by another device.

The operation of clearing the TE bit disables the transmitter after completion of transmission of the current data word. Setting the TE bit again enables transmission of the next word. During the time that TE=0, the STXD signal is tri-stated. The TE bit should be cleared after the TDE bit is set to ensure that all pending data is transmitted.

To summarize, the network mode transmitter generates interrupts every time slot (unless the TSM registers are used) and requires the DSP program to respond to each time slot. These responses may be one of the following:

- Write the data register with data to enable transmission in the next time slot.
- Write the time slot register to disable transmission in the next time slot.
- Do nothing—transmit underrun occurs at the beginning of the next time slot and the previous data is re-transmitted.

7.4.6.1.2.2 Network Mode Receive

The receiver portion of the SSI is enabled when both the SSIEN and the RE bits in the SCR2 are set. However, when the RE bit is set, the receiver is enabled only after detection of a new frame boundary. Software has to find the start of the next frame (by checking the RFS bit in the SCSR register). A normal start-up sequence for receive operation is to do the following steps:

1. Set the SCSR, SRXCR, SCR2, and SOR registers to select network mode operation, define the receive clock, receive frame sync, and frame structure required for proper system operation.
2. Enable SSI (SSIEN = 1).

3. Enable RXFIFO (RFEN=1) and configure receive watermark (RFWM=n) if RXFIFO is used.
4. Enable receive interrupts.
5. Set the RE bit (RE = 1) to enable the receiver operation on the next frame sync boundary.

The receiver timing for an 8-bit word with continuous clock, FIFO disabled, five words per frame sync, in network mode is shown in Figure 75. The explanatory notes for the receive portion of the figure are shown in Table 57.

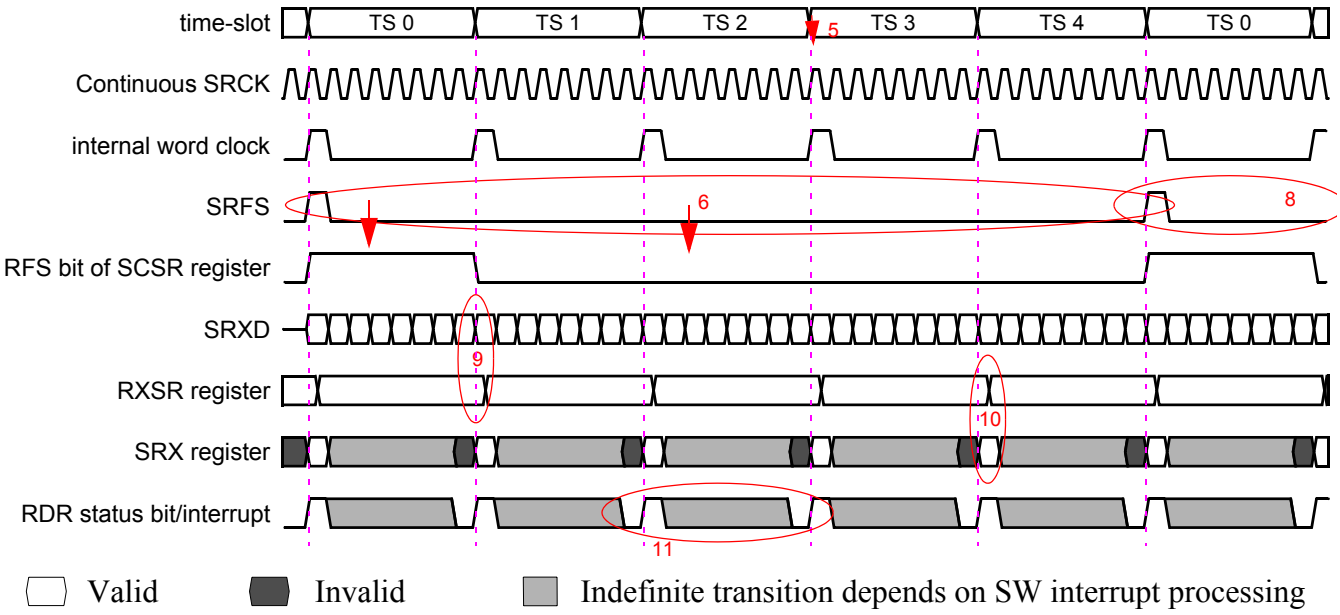


Figure 75. Network Mode Receive Timing

Table 57. Notes for Receive Timing in Figure 75

Note	Source Signal	Destination Signal	Description
1			Example of a 5 time-slot frame, receiving data from time-slots 0 and 2. Note that the receive hardware will obtain data on the SRXD pin every bit time. The software must determine which data belongs to each time-slot and discard the unwanted time-slot data.
2	SRCK		The figure shows the transmit and receive timing as the same, although this is not the general case.
3	SRFS		Example with bit-length frame sync and standard timing (RFSI=0, RFSL=1, REFS=0). Frame timing begins with the rising edge of SRFS.
4	SRXD	RXSR register	Data on the SRXD pin is sampled on the falling edge of SRCK and shifted into the RXSR register.
5	RXSR register	SRX register	At the word clock, the data in the RXSR register is transferred to the SRX register.

Table 57. Notes for Receive Timing in Figure 75 (Continued)

Note	Source Signal	Destination Signal	Description
6	RDR status flag and receive interrupt		This flag is set for each word clock (time-slot) to indicate that data is available to be processed. The software must keep track of the time-slots as they occur so it knows which data to keep. If the receive interrupts are enabled (RIE=1), an interrupt will be generated when this status flag is set. The software reads the SRX register to clear the interrupt (see Section 7.4.9.2, "Description of Interrupt Operation," for a complete description of interrupt processing).

An interrupt can occur after the reception of each data word or the programmer can poll the RDR flag. The SSI program response can be one of the following:

- Read SRX and use the data.
- Read SRX and ignore the data.
- Do nothing—the receiver overrun exception occurs at the end of the current time slot.

7.4.6.1.3 Synchronous/Asynchronous Operating Modes

The transmit and receive sections of the SSI may be synchronous or asynchronous. During asynchronous operation, the transmitter and receiver have their own separate clock and sync signals. When operating in synchronous mode, the transmitter and receiver use common clock and synchronization signals, as specified by the transmitter configuration. The SYN bit in SCR2 selects synchronous or asynchronous operation.

Since the SSI is designed to operate either synchronously or asynchronously, separate receive and transmit interrupts are provided. During synchronous operation, the receiver and transmitter operate in lock step with each other and the software designer may want to reduce overhead by eliminating either the receive or transmit interrupts, driving both channels from the same set of interrupts. If this decision is made, the software designer needs to be aware of the specific timing of the receive and transmit interrupts since the interrupts are not generated at the exact same point in the frame timing, as shown in Figure 76. If it is desired to run off a single set of interrupts, the TX interrupts should be used. If RX interrupts are used, there may be timing problems with the transmit data since this interrupt occurs a half-bit time before the transmit data is used by the hardware.

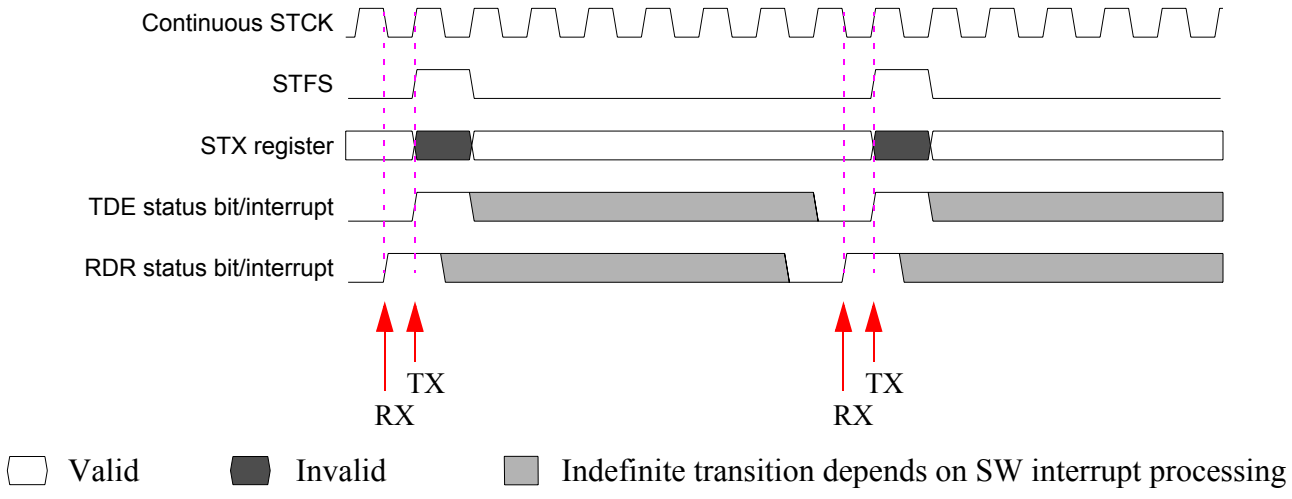


Figure 76. Synchronous Mode Interrupt Timing

7.4.6.1.4 Network Mode with Mask Registers Implemented

In order to reduce interrupt overhead, a number of enhancements can be made to the SSI module. The enhancements incorporate the mask registers (TSM and RSM) and the frame status register (SFSR).

Figure 77 and Figure 78 show sample timing of network mode transfers, using the mask registers. These figures duplicate the frame structure of Figure 74 to show the reduced amount of interrupt processing required. The numbered circles and arrows in the figures identify discussion notes which are contained in Table 58 and Table 59.

7.4.6.1.4.1 Operation with TSM Register

The TSM register is included in the design so that interrupt overhead can be reduced. If all bits of the TSM register are set, the SSI transmitter will continue to operate as previously described. The TSM register is used to disable the STXD pin on specific time-slots. This is accomplished by writing the TSM with 0 in the time-slot bit location. Disabling a time-slot in this manner causes the time-slot to be ignored by the SSI. This means no data is transferred to the transmit shift register (TXSR) and no interrupts are generated for this time-slot.

The transmitter timing, using the TSM registers, for an 8-bit word with continuous clock, FIFO disabled, five words per frame sync, in network mode is shown in Figure 77. The explanatory notes for the transmit portion of the figure are shown in Table 58.

NOTE:

In this example there are only two transmit interrupts per frame instead of five as in the previous example where the TSM register is not used.

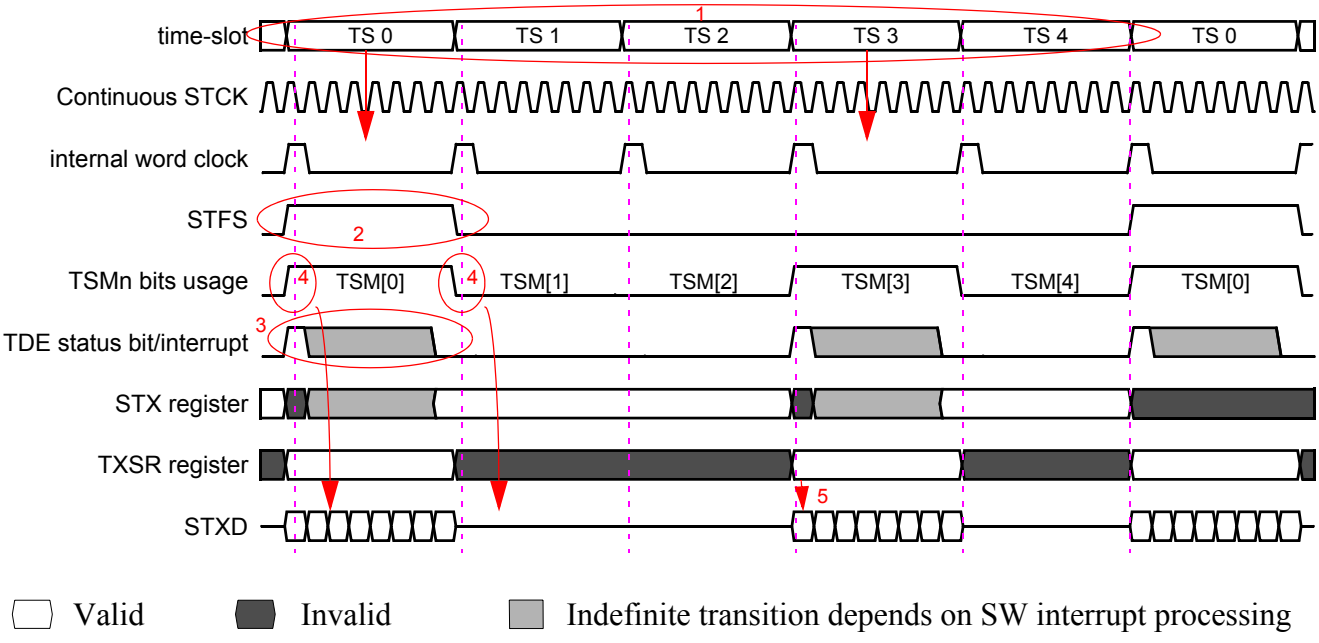


Figure 77. Network Mode Transmit Timing with Mask Register

Table 58. Notes for Transmit Timing with Mask Register in Figure 77

Note	Source Signal	Destination Signal	Description
1			Example of a 5 time-slot frame, transmitting in time-slots 0 and 3.
2	STFS		Example with word-length frame sync and standard timing (TFSI=0, TFSL=0, TEFS=0). Frame timing begins with the rising edge of STFS.
3		TDE status flag and interrupt	This flag is set at the beginning of each word (for enabled time-slots) to indicate that the STX data has been used and another data word should be supplied by the software. If the transmit interrupt is enabled, the processor is interrupted to request the data. The flag (and interrupt) are cleared when data is written to either the STX or STSR registers (see Section 7.4.9.2, “Description of Interrupt Operation,” for a complete description of interrupt processing).
4	STX\STSR register	TXSR register	On each word clock boundary, a decision is made concerning what to transmit on the next time-slot. If the TSMn register bit is a 0 for the next time-slot, the STXD pin is tri-stated and the time-slot is ignored. If the TSMn register bit is a 1 for the next time-slot, the contents of the STX register are transferred to the TXSR register and this data is shifted out. If the STX register has not been written in the previous time-slot, the previous data is reused. **NOTE:** If the STSR is written instead of the STX, the STXD pin is tri-stated as documented in Section 7.4.6.1.2, “Network Mode.” If neither of these registers were written in the previous time-slot (where TSMn=1), the TUE status bit will be set and the hardware will operate as if the STX register had been written. The STXD pin will be enabled and the contents of the STX will be transmitted again. Note that this may lead to drive conflicts on the transmit data line, if another device is transmitting data during this time-slot.
5	TXSR register	STXD pin	On active time-slots, the TXSR register contents are shifted out on the STXD pin, one bit per rising edge of STCK. On inactive time-slots, the STXD pin is tri-stated so it can be driven by another device.

7.4.6.1.4.2 Operation with RSM Register

The RSM register is included in the design so that interrupt overhead can be reduced. If all bits of the RSM register are set, the SSI receiver will continue to operate as previously described. The RSM register is used to automatically discard data from selected time-slots. This is accomplished by writing the RSM with 0 in the selected time-slot bit location. This means no data is transferred from the receive shift register (RXSR) on the 0 time-slots, no status flags change, and no interrupts are generated.

The receiver timing, using the RSM registers, for an 8-bit word with continuous clock, FIFO disabled, five words per frame sync, in network mode is shown in Figure 78. The explanatory notes for the receive portion of the figure are shown in Table 59.

NOTE:

In this example there are only two receive interrupts per frame instead of five as in the previous example where the RSM register is not used.

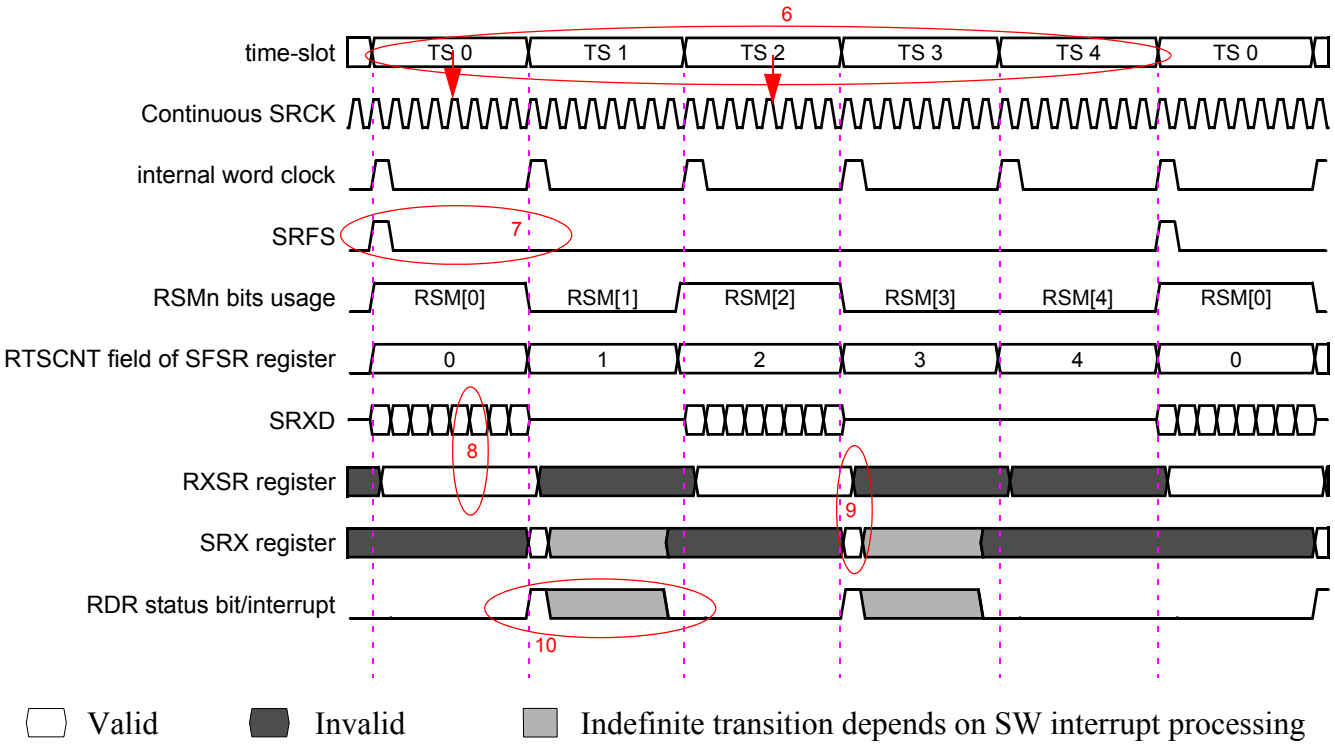


Figure 78. Network Mode Receive Timing with Mask Register

Table 59. Notes for Receive Timing with Mask Register in Figure 78

Note	Source Signal	Destination Signal	Description
6			Example of a 5 time-slot frame, receiving data from time-slots 0 and 2. Note that the receive hardware will only obtain data on the SRXD pin when the RSMn bit is set to 1.
7	SRFS		Example with bit-length frame sync and standard timing (RFSI=0, RFSL=1, REFS=0). Frame timing begins with the rising edge of SRFS.
8	SRXD	RXSR register	Data on the SRXD pin is sampled on the falling edge of SRCK and shifted into the RXSR register.
9	RXSR register	SRX register	At the word clock, the data in the RXSR register is transferred to the SRX register, for enabled time-slots.
10	RDR status flag and receive interrupt		This flag is set for each word clock (time-slot) where the RSMn bit is set, to indicate that data is available to be processed. The software must keep track of the time-slots as they occur so it knows which data it is processing. If the receive interrupts are enabled (RIE=1), an interrupt will be generated when this status flag is set. The software reads the SRX register to clear the interrupt (see Section 7.4.9.2, “Description of Interrupt Operation,” for a complete description of interrupt processing).

7.4.7 Resets

7.4.7.1 General

The SSI is affected by power-on reset and SSI reset.

Power-on reset is generated by asserting either the RESET pin or the computer operating properly (COP) timer reset. The power-on reset initializes all control registers, which clears the SSIEN bit in SCR2 and disables the SSI.

The SSI reset is generated when the SSIEN bit in the SCR2 is cleared. The SSI status bits are preset to the same state produced by the power-on reset. The SSI control bits are unaffected. The control bits in the top half of the SCSR are also unaffected. The SSI reset is useful for selective reset of the SSI without changing the present SSI control bits and without affecting the other peripherals.

The correct sequence to initialize the SSI is as follows:

1. Issue a power-on or SSI reset.
2. Program the SSI control registers.
3. Set the SSIEN bit in SCR2.

To ensure proper operation of the SSI, the programmer should use the power-on or SSI reset before changing any of the following control bits listed in Table 60.

NOTE:

These control bits should not be changed during SSI operation.

NOTE:

The SSI bit clock must go low for at least one complete period to ensure proper SSI reset.

Table 60. SSI Control Bits Requiring Reset before Change

Control Register	Bit
SRXCR STXCR	PSR WL[1:0] DC[4:0] PM[7:0]
SCR2	TEFS TFSL TFSI NET TSCKP TSHFD SYN
SCSR	REFS RFSL RFSI RSCKP RSHFD DIV4DIS

7.4.8 Clocks

The SSI uses the following three clocks (as shown in Figure 79 and Figure 80):

- Bit clock—Used to serially clock the data bits in and out of the SSI port.
- Word clock—Used to count the number of data bits per word (8, 10, 12, or 16 bits).
- Frame clock—Used to count the number of words in a frame.

The bit clock is used to serially clock the data. It is visible on the serial transmit clock (STCK) and serial receive clock (SRCK) pins. The word clock is an internal clock used to determine when transmission of an 8-, 10-, 12-, or 16-bit word has completed. The word clock in turn then clocks the frame clock, which marks the beginning of each frame. The frame clock can be viewed on the STFS and SRFS pins. The bit clock can be received from an SSI clock pin or can be generated from the peripheral clock passed through a divider, as shown in Figure 81.

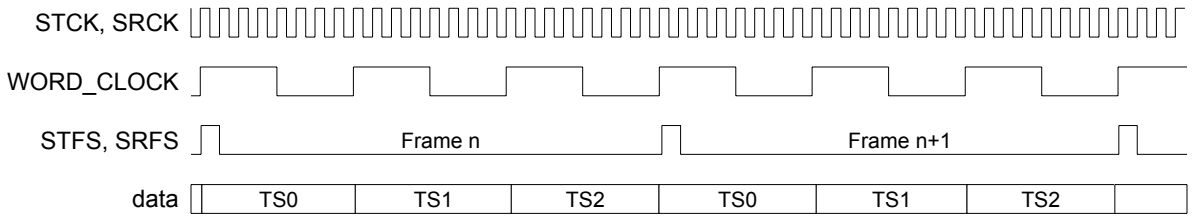


Figure 79. SSI Clocking (8-bit words, 3 time-slots/frame)

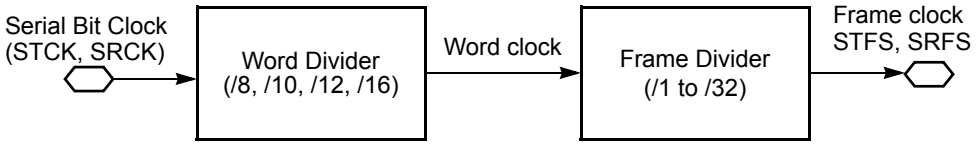


Figure 80. SSI Clock Generation

Table 61. Clock Summary

Clock	Priority	Source	Characteristics
STCK		Internal/External	Transmit data is changed on the rising edge of this clock. The TSCKP bit of the SCR2 register can invert the clock if needed.
SRCK		Internal/External	Receive data is captured on the falling edge of this clock. The RSCKP bit of the SCSR register can invert the clock if needed.
STFS		Internal/External	Transmit frames begin with the rising edge of this signal. See the definition of the TEFS bit of the SCR2 register for timing options. The TFSI bit can invert this signal if needed.
SRFS		Internal/External	Receive frames begin with the rising edge of this signal. See the definition of the REFS bit of the SCSR register for timing options.

7.4.8.1 Description of Clock Operation

The following section describes clock operation.

7.4.8.1.1 SSI Clock and Frame Sync Generation

Data clock and frame sync signals can be generated internally by the SSI or can be obtained from external sources. If internally generated, the SSI clock generator is used to derive bit clock and frame sync signals

from the peripheral clock. The SSI clock generator consists of a selectable, fixed prescaler and a programmable prescaler for bit rate clock generation. In gated clock mode, the data clock is valid only when data is being transmitted (See Section 7.4.6.1.1.3, “Gated Clock Operation”). A programmable frame rate divider and a word length divider are used for frame rate sync signal generation.

Figure 81 shows a block diagram of the clock generator for the transmit section. The serial bit clock can be internal or external, depending on the transmit direction (TXDIR) bit in the SSI control register 2 (SCR2). The receive section contains an equivalent clock generator circuit.

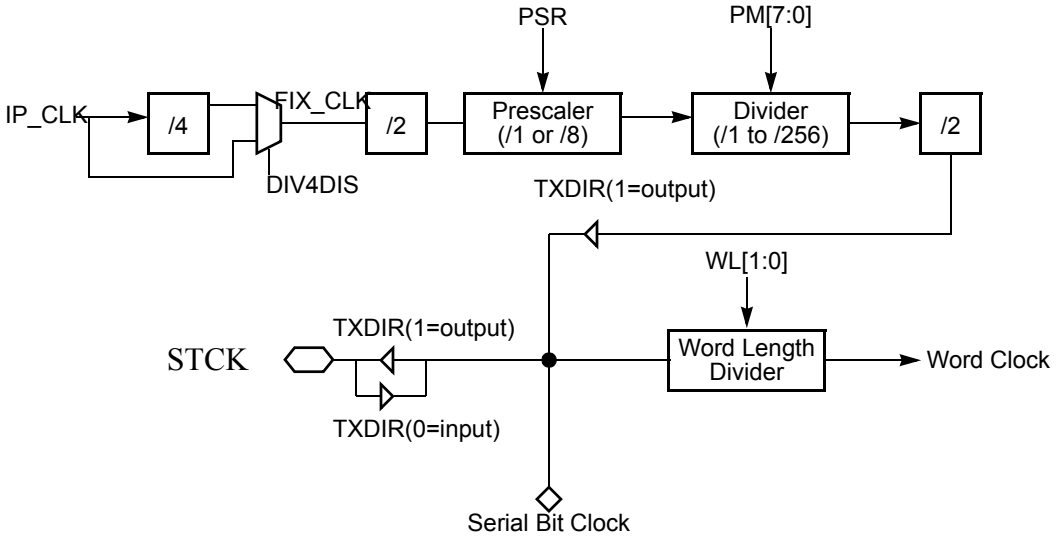


Figure 81. SSI Transmit Clock Generator Block Diagram

Figure 82 shows the frame sync generator block for the transmit section. When internally generated, both receive and transmit frame sync are generated from the word clock and are defined by the frame rate divider (DC[4:0]) bits and the word length (WL[1:0]) bits of the SSI transmit control register (STXCR). The receive section contains an equivalent circuit for its frame sync generator.

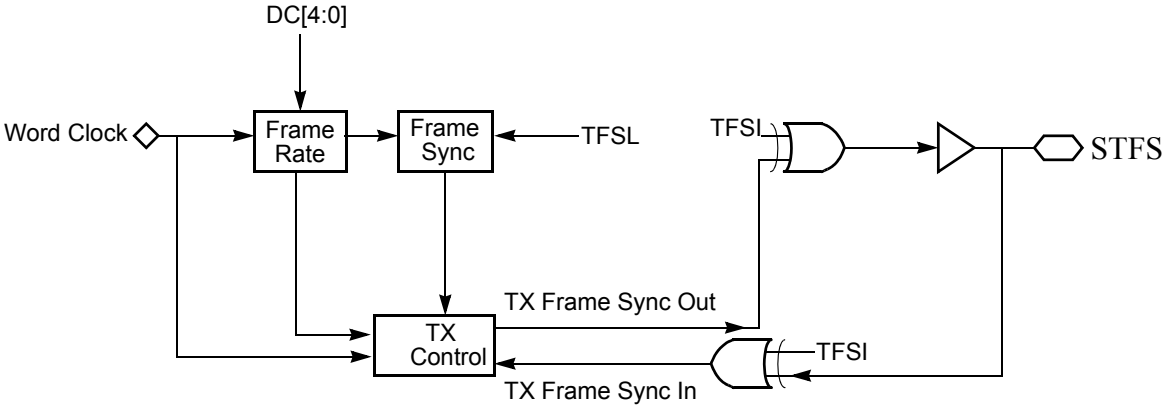


Figure 82. SSI Transmit Frame Sync Generator Block Diagram

7.4.9 Interrupts

7.4.9.1 General

The SSI can generate four interrupt vectors as shown in Table 25.

Table 62. Interrupt Summary

Interrupt	Source	Description
INTR+0	Receiver	Receive data with exception
INTR+2	Receiver	Receive data
INTR+4	Receiver	Receive last slot interrupt - this interrupt may not be present in all implementations of the SSI
INTR+6	Transmitter	Transmit data with exception
INTR+8	Transmitter	Transmit data

7.4.9.2 Description of Interrupt Operation

The following section describes interrupt operation.

7.4.9.2.1 Receive Data with Exception

This interrupt can occur when receive interrupts are enabled via the RIE bit of the SCR2 register. When a data word is ready to transfer from the RXSR to the SRX and the previous SRX data has not yet been read, the ROE bit is set and the exception interrupt will occur instead of the normal receive data interrupt. An interrupt will also occur when data is transferred from the RXSR to the RXFIFO with RFF set. In the second case, data may or may not be lost depending on whether the FIFO has 8 words in it or has been flagged as full by a watermark.

7.4.9.2.2 Receive Data

This interrupt can occur when receive interrupts are enabled via the RIE bit of the SCR2 register. When a data word is ready to transfer from the RXSR to the SRX, and the ROE bit is not set, this interrupt will occur to indicate that received data is available for processing. When the receive FIFO is enabled, this interrupt will not occur until the receive watermark level of the FIFO is reached. If the FIFO is not enabled, this interrupt will occur for each data word received.

7.4.9.2.3 Transmit Data with Exception

This interrupt can occur when transmit interrupts are enabled via the TIE bit of the SCR2 register. When it is time to transfer data to the TXSR and no data is available in the STX or TXFIFO (if enabled), the TUE status bit is set and the transmit data exception interrupt occurs.

7.4.9.2.4 Transmit Data

This interrupt can occur when transmit interrupts are enabled via the TIE bit of the SCR2 register. When data is transferred to the TXSR, this interrupt will occur if more data is needed. If the transmit FIFO is not enabled, this interrupt will occur for each data word transmitted. If the transmit FIFO is enabled, the interrupt will not occur until the transmit watermark level is reached.

7.4.10 SSI Timing Diagrams

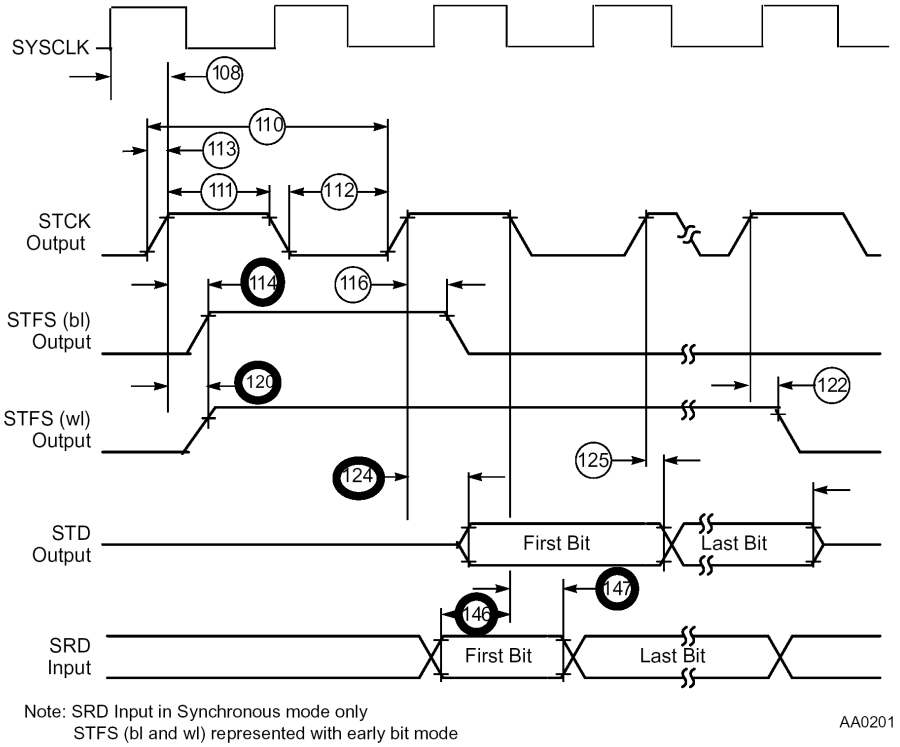


Figure 83. SSI Transmitter Internal Clock Timing

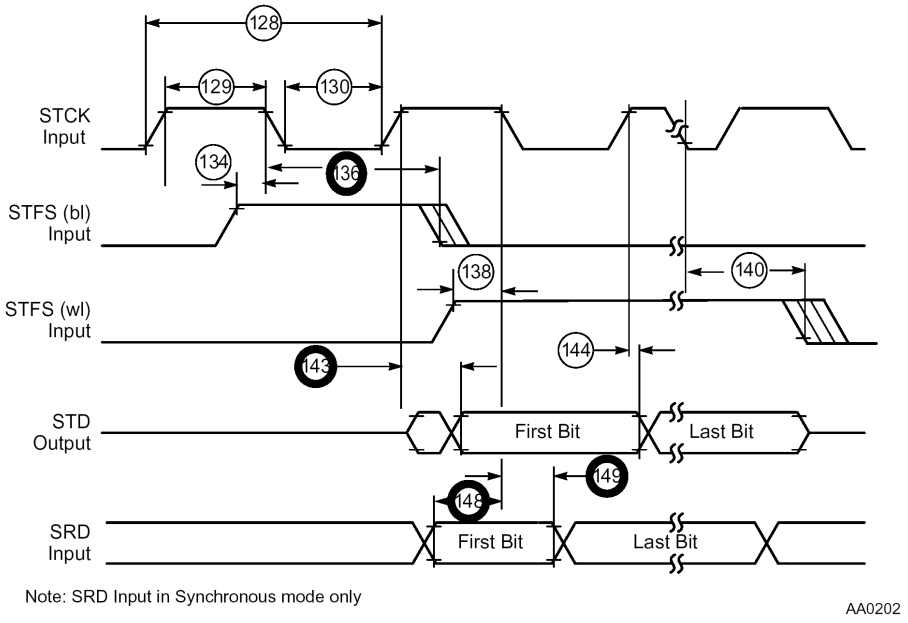


Figure 84. SSI Transmitter External Clock Timing

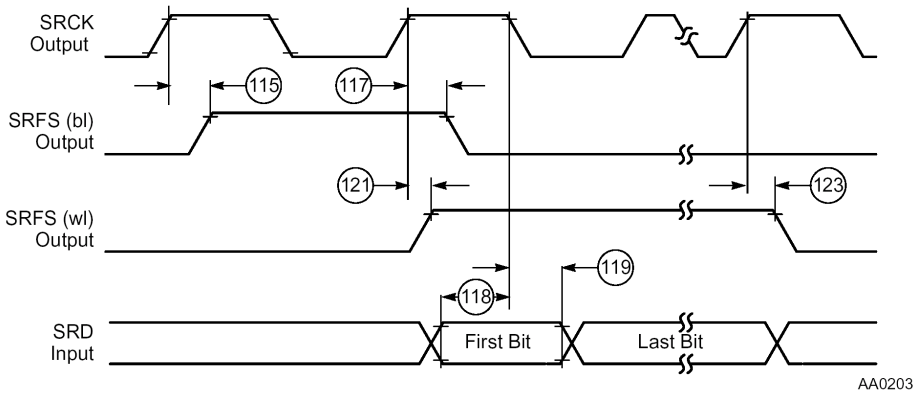


Figure 85. SSI Receiver Internal Clock Timing

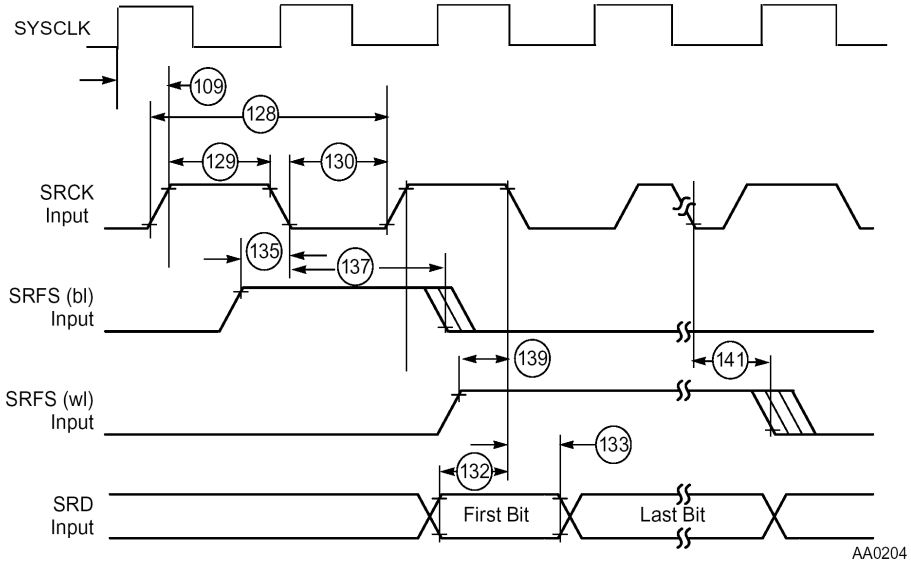


Figure 86. SSI Receiver External Clock Timing

(GND_IO = 0 V, VDD_IO = 1.8V, T_A = –40° to +85°C, CL = 20 pF)

Table 63. SSI Timing

No.	Characteristic	Min	Max	Unit
Internal Clock/Frame Sync Operation				
108	SYSCLK high to STCK high	2.2	6.07	ns
109	SYSCLK high to SRCK high	2.2	5.8	ns
110	Clock cycle[1] (SYSCLK/4)	166		ns
111	Clock high period	83		ns
112	Clock low period	83		ns
113	Output clock rise/fall time		2.0	ns

Table 63. SSI Timing (Continued)

No.	Characteristic	Min	Max	Unit
114	STCK high to STFS (bl) high[2]			ns
115	SRCK high to SRFS (bl) high[2]	.6	.6	ns
116	STCK high to STFS (bl) low[2]	.7	1.1	ns
117	SRCK high to SRFS (bl) low[2]	.1	.2	ns
118	SRD setup time before SRCK low	.2	.7	ns
119	SRD hold time after SRCK low	15.6	—	ns
120	STCK high to STFS (wl) high[2]	—	1.4	ns
121	SRCK high to SRFS (wl) high[2]	.6	.6	ns
122	STCK high to STFS (wl) low[2]	.7	1.1	ns
123	SRCK high to SRFS (wl) low[2]	.1	.2	ns
124	STCK high to STD valid			ns
125	STCK High to STD not valid			ns
External Clock/Frame Sync Operation				
128	Clock cycle period[3]	166	CPmax	ns
129	Clock high period	83		ns
130	Clock low period	83		ns
132	SRD Setup time before SRCK low	5.5		ns
133	SRD hold time after SRCK low		1.8	ns
134	STFS (bl) setup before STCK low[2]	4.5	CPmax-10	ns
135	SRFS (bl) setup before SRCK low[2]	5.6	CPmax-10	ns
136	STFS (bl) hold after STCK low[2]	5	CPmax-20	ns
137	SRFS (bl) hold after SRCK low[2]	5	CPmax-20	ns
138	STFS (wl) setup before STCK low[2]	4.5	CPmax-10	ns
139	SRFS (wl) setup before SRCK low[2]	5.6	CPmax-10	ns
140	STFS (wl) hold after STCK low[2]	5	CPmax-20	ns
141	SRFS (wl) hold after SRCK low[2]	5	CPmax-20	ns
143	STCK high to STD valid		17.0	ns
144	STCK high to STD not valid	5.6	17.0	ns
148	SRD setup before STCK low	4.5	CPmax-10	ns

Table 63. SSI Timing (Continued)

No.	Characteristic	Min	Max	Unit
149	SRD hold after STCK low	5	CPmax-20	ns

1. Based on SYSCLK of 24 MHz (from MC72000 BT radio). All the timings for the SSI are given for a non-inverted serial clock polarity and a non-inverted frame sync. If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK and/or the frame sync FSR/FST in the tables and in the figures.
2. bl = bit length; wl = word length
3. CPmax = clock period max for system

7.4.10.1 Frame Sync/Clock Phasing

When using an external bit-wide frame sync, the transmit frame sync should be asserted when the clock is asserted and should remain asserted for a full clock period. The timing of the trailing edge of STFS is no longer critical with respect to the rising edge of STCK. This is shown in Figure 87.

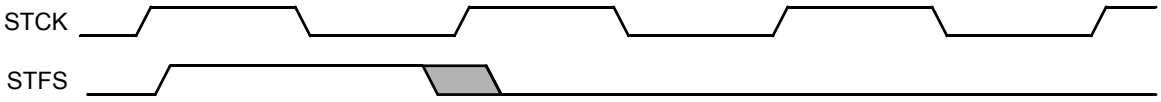


Figure 87. SSI Frame Sync versus Clock Timing Diagram

7.4.10.2 External Frame Sync Setup

When using external frame syncs, there must be at least four clocks after enabling the transmitter/receiver and before the first frame sync.

7.4.10.3 Max External Clock Rate

The maximum allowable rate for an external clock source is 1/4 of the peripheral clock, or up to 2 Mbits/s.

8 Bluetooth Baseband Functionality Overview

This section describes the features of the Bluetooth baseband stack, which is included in the MC72000. The baseband runs on the ARM7 microcontroller and features highly advanced third generation link control (LC), link manager (LM), and human-computer interface (HCI) layers fully compliant with the Bluetooth v1.1 specification.

The baseband stack is specifically designed with complex scenarios in mind, and is capable of handling concurrent execution of multiple HCI, LM, and LC procedures. This means that the stack is well suited even for advanced scenarios involving full 7 slave piconet situations as well as scatternet operation. The stack also features state-of-the-art Bluetooth audio and includes all Bluetooth v1.1 supported air coding formats.

In order to ensure high quality and stability, the stack has been thoroughly tested by an independent test house. Furthermore, the baseband is firmware upgradeable through a ROM patching system allowing firmware patches resident in an attached EEPROM to be applied.

8.1 Link Controller Features

The following table lists in detail the supported Link Controller features of the MC72000. The table parallels the Bluetooth SIG's PICS Proforma for Baseband, Annex B, Version 0.92, except for some additional fields, which have been included to provide additional overview.

Table 64. Overview of Link Controller Features

Feature	ROM
Frequency Hopping Systems	
79-channel frequency hopping system	x
23-channel frequency hopping system[1]	x
Link Types	
ACL link support	x
SCO link support	x
Piconet Capabilities	
Max simultaneous ACL links[2]	7
Broadcast messages	x
Point-to-multipoint connections	x
Scatternet Capabilities	
Master in one piconet and slave in another	x
Slave in more than one piconet	x
Inquiry Scan as slave	x
Remote Name Request and/or response regardless if slave or master	x
SCO Link Capabilities	
Max simultaneous SCO links[2]	1
Multiple SCO links to same slave	
Multiple SCO links to different slaves	
Multiple SCO links from same master	
Multiple SCO links from different masters	
Voice Coding Schemes	
A-law	x
μ-law	x

Table 64. Overview of Link Controller Features (Continued)

Feature	ROM
CVSD	x
Common Packet Types	
ID packet type	x
NULL packet type	x
POLL packet type	x
FHS packet type	x
DM1 packet type	x
ACL Packet Types	
DH1 packet type	x
DM3 packet type	x
DH3 packet type	x
DM5 packet type	x
DH5 packet type	x
AUX1 packet type	
SCO Packet Types	
HV1 packet type	x
HV2 packet type	x
HV3 packet type	x
DV packet type	x
Paging Procedures	
Paging, 79-channel system	x
Page scan, 79-channel system	x
Paging, 23-channel system[1]	x
Page scan, 23-channel system[1]	x
Paging Schemes	
Paging scheme 0 (Mandatory)	x
Paging scheme 1 (Optional I)	
Paging Scheme 2 (Optional II) - Not defined in specification yet.	x

Table 64. Overview of Link Controller Features (Continued)

Feature	ROM
Paging Scheme 3 (Optional III) - Not defined in specification yet.	x
Page Scanning Modes	
Paging mode R0	x
Paging mode R1	x
Paging mode R2	x
Paging Train Repetition	
$N_{page} \geq 1$	x
$N_{page} \geq 128$	x
$N_{page} \geq 256$	x
Inquiry Procedures	
Inquiry, 79-channel system	x
Inquiry scan, 79-channel system	x
Inquiry, 23-channel system[1]	x
Inquiry scan, 23-channel system[1]	x
Inquiry support for all IACs	x
Inquiry scan, max num simultaneous IACs	2

1. The 23-channel frequency hopping system is fully implemented in ROM, but as it is being discontinued by the Bluetooth SIG, extensive testing has not been performed.
2. This value can be adjusted down to reduce the amount of RAM used on the MC72000.

8.2 Link Manager Features

The table on the following pages lists the Link Manager features of the MC72000. The table parallels the Bluetooth SIG's PICS Proforma for LM, Annex B, Version 0.92.

Table 65. Overview of Link Manager Features

Feature	ROM
Response Messages	
Accept message	x
Reject message	x
Supported Features (General Statement)	
3-slot packets	x
5-slot packets	x
Encryption	x
Slot offset	x
Timing accuracy	x
Role switch (master/slave)	x
Hold mode	x
Sniff mode	x
Park mode	
Power control	x [1]
Channel quality driven data rate	
RSSI	x
Authentication	
Initiate authentication before connection completed	x
Initiate authentication after connection completed	x
Respond to authentication request	x
Pairing	
Initiate pairing before connection completed	x
Initiate pairing after connection completed	x
Respond to pairing request	x
Use fixed PIN and request responder-to-initiator switch	x

Table 65. Overview of Link Manager Features (Continued)

Feature	ROM
Use variable PIN	x
Accept initiator-to-responder switch	x
Link Keys	
Link key creation using a unit key (local device is configured with a unit key)	
Link key creation using a combination key	x
Initiate change of link key	x
Accept change of link key	x
Change to temporary key (i.e., master link key)	x
Make semi-permanent link key the current link key (i.e., exit master link key)	x
Accept pairing with unit key (remote device is configured with a unit key)	x
Encryption	
Initiate encryption	x
Accept encryption requests	x
Point-to-point encryption	x
Point-to-point and broadcast encryption	x
Key size negotiation (up to 128 bit)	x
Start encryption	x
Accept start of encryption	x
Stop encryption	x
Accept stop of encryption	x
Information Requests/Status Requests	
Request clock offset information	x
Respond to clock offset requests	x
Send slot offset information	x
Request timing accuracy information	x
Respond to timing accuracy requests	x
Request LM version information	x

Table 65. Overview of Link Manager Features (Continued)

Feature	ROM
Respond to LM version requests	x
Request supported features	x
Respond to supported features requests	x
Request name information	x
Respond to name requests	x
Get link quality	x
Read RSSI	x
Role Switch	
Request master/slave switch	x
Accept master/slave switch requests	x
Detach	
Detach connection	x
Hold Mode	
Request hold mode	x
Respond to hold mode requests	x
Force hold mode	
Accept forced hold mode	x
Sniff Mode	
Request sniff mode	x
Respond to sniff mode requests	x
Request un-sniff	x
Accept un-sniff requests	x
Park Mode	
Request park mode	
Respond to park mode request	
Set up broadcast scan window	
Accept change to the broadcast scan window	
Modify beacon parameters	

Table 65. Overview of Link Manager Features (Continued)

Feature	ROM
Accept modification of beacon parameters	
Request unpark using PM_ADDR	
Request unpark using BD_ADDR	
Slave requested unpark	
Accept unpark using PM_ADDR	
Accept unpark using BD_ADDR	
Power Control	
Request to increase power	x
Request to decrease power	x
Respond when max power reached	x[1]
Respond when minimum power reached	x[1]
Link Supervision Timeout	
Set link supervision timeout value	x
Accept link supervision timeout setting	x
Quality of Service	
Channel quality driven change between DM and DH packet types	
Force/accept forced change of Quality of Service (QoS)	x[2]
Request/accept change of QoS	x[2]
Multi-Slot Packages	
Allow maximum number of slots to be used	x
Request maximum number of slots to be used	x
Accept request of maximum number of slots to be used	x
SCO Links	
Initiate SCO Links as master	x
Initiate SCO Links as slave	x
Accept SCO links	x

Table 65. Overview of Link Manager Features (Continued)

Feature	ROM
Remove SCO Links as master	x
Remove SCO Links as slave	x
Negotiate SCO parameters as master	x
Negotiate SCO parameters as slave	x
Paging Scheme	
Request page mode to use	
Accept suggested page mode	
Request page scan mode to use	
Accept suggested page scan mode	
Connection Establishment	
Create connection for higher layers	x
Respond to requests to establish connections for higher layers	x
Indicate that link set-up is complete	x
Test Mode	
Activate test mode (as tester)	
Enable test mode (as DUT) and ability to accept activation of test mode	x
Ability to reject activation of test mode if test mode is disabled	x
Control test mode (as tester)	
Ability to reject test mode control commands if test mode is disabled	x

1. Power control is enabled if supported by hardware (use next available number).
2. The ROM version supports Best-Effort Quality of Service (QoS) only.

9 HCI Features

The HCI provides a command interface to the baseband controller and link manager, and access to hardware status and control registers. This interface provides a uniform method of accessing the Bluetooth baseband capabilities. Table 65 shows the currently supported HCI commands. The commands are divided into the following major groupings: link control, link policy, host/baseband, events, informational parameters, status parameters, and testing. The following list shows some of the key features of the HCI:

- 23- and 79-channel frequency hopping.
- Support of all connection types.
- Support of all packet types.
- Host controller HCI flow control.
- Authentication and pairing.
- Change packet type.
- Encryption.
- Master/slave role switch.
- Hold/sniff modes.
- Radio TX power status and control.
- Test modes.

Table 66. HCI Commands and Events

HCI Command Name	Currently Supported
Link Control Commands	
HCI_Inquiry	x
HCI_Inquiry_Cancel	x
HCI_Periodic_Inquiry_Mode	x
HCI_Exit_Periodic_Inquiry_Mode	x
HCI_Create_Connection	x
HCI_Disconnect	x
HCI_Accept_Connection_Request	x
HCI_Reject_Connection_Request	x
HCI_Change_Connection_Packet_Type	x
HCI_Add_SCO_Connection	x
HCI_Remote_Name_Request	x
HCI_Read_Remote_Supported_Features	x
HCI_Read_Clock_Offset	x
HCI_Read_Remote_Version_Information	x
HCI_Authentication_Requested	x
HCI_Link_Key_Request_Reply	x
HCI_Link_Key_Request_Negative_Reply	x
HCI_Pin_Code_Request_Reply	x

Table 66. HCI Commands and Events (Continued)

HCI Command Name	Currently Supported
HCI_Pin_Code_Request_Negative_Reply	x
HCI_Change_Connection_Link_Key	x
HCI_Master_Link_Key	x
HCI_Set_Connection_Encryption	x
Link Policy Commands	
HCI_Read_Link_Policy_Settings	x
HCI_Write_Link_Policy_Settings	x
HCI_Switch_Role	x
HCI_Role_Discovery	x
HCI_Read_Link_Policy_Settings	x
HCI_Write_Link_Policy_Settings	x
HCI_Hold_Mode	x
HCI_Sniff_Mode	x
HCI_Exit_Sniff_Mode	x
HCI_Park_Mode	
HCI_Exit_Park_Mode	
HCI_QoS_Setup	
Host/Baseband Commands	
HCI_Read_Scan_Enable	x
HCI_Write_Scan_Enable	x
HCI_Read_Page_Scan_Activity	x
HCI_Write_Page_Scan_Activity	x
HCI_Read_Inquiry_Scan_Activity	x
HCI_Write_Inquiry_Scan_Activity	x
HCI_Read_Number_Of_Supported_IAC	x
HCI_Read_Current_IAC_LAP	x
HCI_Write_Current_IAC_LAP	x
HCI_Read_Connection_Accept_Timeout	x

Table 66. HCI Commands and Events (Continued)

HCI Command Name	Currently Supported
HCI_Write_Connection_Accept_Timeout	x
HCI_Read_Page_Timeout	x
HCI_Write_Page_Timeout	x
HCI_Flush	x
HCI_Read_Automatic_Flush_Timeout	x
HCI_Write_Automatic_Flush_Timeout	x
HCI_Set_Event_Mask	x
HCI_Set_Event_Filter	x
HCI_Reset	x
HCI_Read_Class_of_Device	x
HCI_Write_Class_of_Device	x
HCI_Read_Num_Broadcast_Retransmissions	x
HCI_Write_Num_Broadcast_Retransmissions	x
HCI_Read_Link_Supervision_Timeout	x
HCI_Write_Link_Supervision_Timeout	x
HCI_Read_Voice_Setting	x
HCI_Write_Voice_Setting	x
HCI_Read_SCO_Flow_Control_Enable	x
HCI_Write_SCO_Flow_Control_Enable	x
HCI_Host_Buffer_Size	x
HCI_Set_Host_Controller_To_Host_Flow_Control	x
HCI_Host_Number_Of_Completed_Packets	x
HCI_Read_Authentication_Enable	x
HCI_Write_Authentication_Enable	x
HCI_Read_PIN_Type	x
HCI_Write_PIN_Type	x
HCI_Read_Stored_Link_Key	x
HCI_Write_Stored_Link_Key	x
HCI_Delete_Stored_Link_Key	x

Table 66. HCI Commands and Events (Continued)

HCI Command Name	Currently Supported
HCI_Read_Encryption_Mode	x
HCI_Write_Encryption_Mode	x
HCI_Read_Hold_Mode_Activity	x
HCI_Write_Hold_Mode_Activity	x
HCI_Read_Transmit_Power_Level	x
HCI_Read_Page_Scan_Mode	x
HCI_Write_Page_Scan_Mode	
HCI_Read_Page_Scan_Period_Mode	x
HCI_Write_Page_Scan_Period_Mode	
Informational Parameters	
HCI_Read_BD_ADDR	x
HCI_Read_Buffer_Size	x
HCI_Read_Local_Supported_Features	x
HCI_Read_Country_Code	x
HCI_Read_Local_Version_Information	x
Status Parameters	
HCI_Read_Failed_Contact_Counter	x
HCI_Reset_Failed_Contact_Counter	x
HCI_Get_Link_Quality	x
HCI_Read_RSSI	x
Testing	
HCI_Read_Loopback_Mode	x
HCI_Read_RSSI	x
HCI_Enable_Device_Under_Test_Mode	x
Motorola Vendor Specific Commands	
HCI_MOT_Read_Connect_Status	x
HCI_MOT_Read_Tx_Enable	x
HCI_MOT_Write_Tx_Enable	x

Table 66. HCI Commands and Events (Continued)

HCI Command Name	Currently Supported
HCI_MOT_Set_Fixed_PIN_Code	x
HCI_MOT_Read_Power_Mgmt_Enable	x
HCI_MOT_Write_Power_Mgmt_Enable	x
HCI_MOT_Read_SCO_Interpolation	x
HCI_MOT_Write_SCO_Interpolation	x
HCI_MOT_Read_SCO_Interpolation_Default	x
HCI_MOT_Write_SCO_Interpolation_Default	x
HCI_MOT_Read_Wakeup_Config	x
HCI_MOT_Write_Wakeup_Config	x
HCI_MOT_Read_Encryption_Key_Size	x
HCI_MOT_Write_Encryption_Key_Size	x
HCI_MOT_Read_Transaction_Discipline	x
HCI_MOT_Write_Transaction_Discipline	x
HCI_MOT_Statistics_Report	x

10 Applications Information

The following sections provide applications information for the MC72000.

10.1 General Purpose Output

The GPO must be set to a logic one during a transmit cycle and set to a logic zero during a receive cycle via internal circuitry, when driving an external antenna switch as shown in Figure 92. When the GPO is not actively used to drive a peripheral, R2/8 in the Radio Register Map is considered a don’t care.

10.2 General Purpose Output Invert

The MC72000 General Purpose Output (GPO) Invert bit (R3/6) can be used to invert the output value of GPO located at Pin K5 of the device. The default setting for GPO Invert is zero (i.e., no inversion). When it is set to one, the GPO output pin assumes the inverted value of GPO in the Radio Register Map location R2/8. This is a useful feature when an inverter is not available. It can serve as a complement to GPO Invert.

10.3 External Power Amplifier Enable

The External Power Amplifier Enable (EPAEN) bit, R6/15, can be used in two applications. It may serve as a complementary driver to a dual-port antenna. This is accomplished when External PA Enable Invert, R3/10, is set to logic one. In this configuration, EPAEN assumes the inverted value of GPO, which is the second driver for the antenna switch. EPAEN may also assist in Class 1 operation by setting bit R11/6 to logic high. This setting allows the MC72000 to drive an external power amplifier. Setting bits R11/6 and R3/10 to zero disables EPAEN.

10.4 External Power Amplifier DAC

The Bluetooth specification for Class 1 Power implementation requires power control from 4.0 dBm (or less) to 20 dBm (max) power. The MC72000 external power amplifier digital to analog converter (EPADRV) output (Pin K6) provides a voltage reference for power control of an external power amplifier (PA), if desired. The EPADRV output is enabled when External PA DAC Enable (R11/7) is set to one. Setting R11/7 to zero pulls the EPADRV output to ground. When enabled, the EPADRV output voltage is controlled by the PA DAC setting (R3/5-0). The minimum EPADRV output voltage is 0 VDC and the maximum output voltage is 3.2 VDC. The 6-bit resolution of the PA DAC setting corresponds to approximately 50 mV/bit. When using a VCCRF < 3.2 Vdc, the maximum EPADRV output voltage is reduced to VCCRF (i.e., the full-scale output of the PA DAC is referenced to 3.2 V). To obtain optimum functionality of EPADRV with an external PA, this feature should be utilized with the External PA Enable. Refer to Section 10, “Applications Information,” for additional usage information. The output of the EPADRV, when enabled, is gated by the MC72000 sequence manager. During a sleep, idle, or RX cycle, the output is set to zero volts. The programmed value of the output voltage is only achieved during an active TX cycle as shown in Figure 30.

10.5 PIN Implementation of Antenna Switch

An alternative approach to using an RF switch is to utilize a PIN diode technique as shown in Figure 88. When both PIN diodes are in the high resistance (i.e., un-biased) state, the transmitter is isolated from the antenna and LNA input. Conversely, when both PIN diodes are in the low resistance (i.e., forward-biased) state, the l/4 section appears as an open circuit from the transmitter output to the LNA input, and the transmitter output is coupled directly to the antenna through the bandpass filter. For receive mode, GPO is set low. For transmit mode, GPO is set high. Some advantages to this implementation include very low current consumption while in receive or idle mode, moderate current consumption while in transmit mode, high receiver isolation, and low cost.

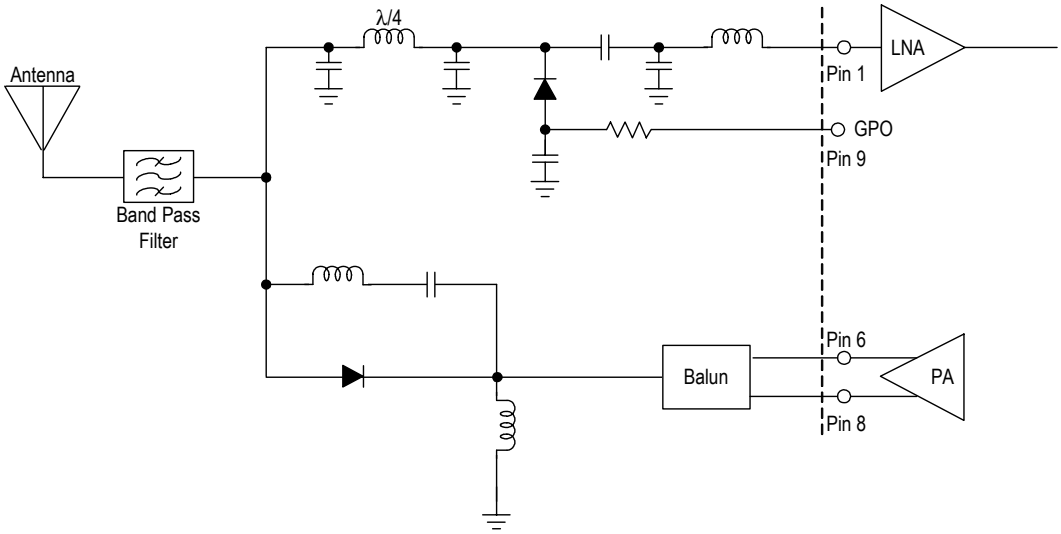


Figure 88. PIN Implementation of Antenna Switch

10.6 Class 1 Operation

Class 1 Operation can be realized by the MC72000 with the use of an external power amplifier (PA) such as the MRFIC2408 as shown in Figure 40. During a transmit cycle, EPAEN drives the external PA Bias Enable. Figure 38 shows the transmitter warm up sequence for this mode of operation. The external PA is required to be fully powered within 5 ms. It is recommended that the antenna switch be set to the TX position before the internal PA is enabled. This option minimizes frequency pulling of the VCO, which may appear as splatter. The power level of the external PA can be digitally controlled through the use of a digital-to-analog converter (EPADAC) internal to the MC72000. To access the DAC capability, External PA DAC Enable (R11/7), must be set to one. This line is generally decoupled with a small capacitor value (H 0.1 ìF). Approximately 44 ìs is available to fully charge this capacitor (see Figure 30).

10.7 Manufacturer Code

The format of the device identification code is shown in Figure 89. The 32-bit value is defined in the IEEE 1149.1 specification. This is also known as the Bluetooth address.

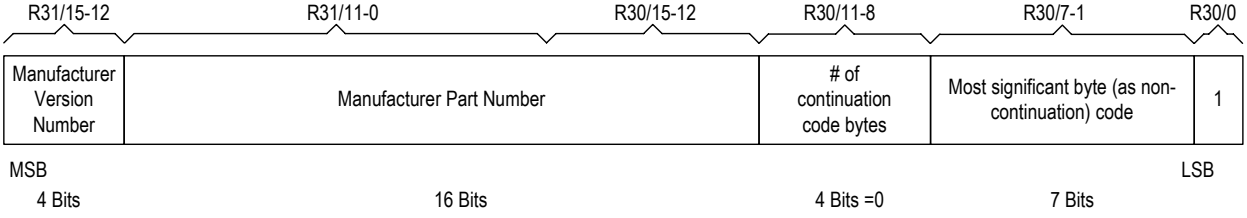


Figure 89. Manufacturer Identification Code

10.8 File System

Three different approaches are possible with the Motorola Bluetooth file system. The first two approaches enable a solution without external EEPROM. All approaches are described in detail in the application notes: *Motorola Bluetooth File System, Host-based General Application Note* (document number 94001481003), *Motorola Bluetooth File System, Host Based One File Application Note* (document number 94001481004) and *Motorola Bluetooth File System, Embedded File System Application Note* (document number 94001481002).

The host interface is the normal serial UART interface, where all communication from application, upper stack, and filesystem passes through (see Figure 90).

Refer to *MC71000/MC72000 Wake-Up, Reset, and Host Clock Request Sequences Application Note* (document number AN2340/D) for a thorough explanation.

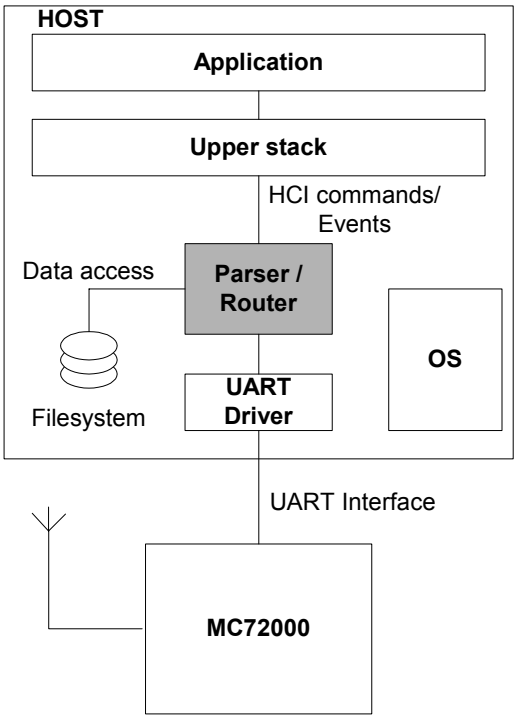


Figure 90. File System Overview

10.8.1 UART Interface Telegrams

The serial UART interface is transporting all types of HCI telegrams. This, in short, is the following:

- HCI ACL: Data transport — typically a file from another unit.
- HCI SCO: Audio transport — typically sound from another unit.
- HCI Commands: Sent to the MC72000, ordering it to do something. Will always result in one or more HCI Events returned.
- HCI Events: Are sent from MC72000 to the host and are a direct response to an HCI command or a spontaneous reaction to something happening in the MC72000.

10.8.2 UART Interface Hardware

The UART driver uses the following signals:

- GND for common ground reference point.
- TxD/RxD for serial data.
- RTS/CTS lines as normal HW-handshake (Optional).
- DTR/DSR lines as Sleep mode request / grand (Optional).

However, the interface can be configured to be a 2, 4 or 6 wire interface. For more details, see document *MC71000/MC72000 Wake-Up, Reset, and Host Clock Request Sequences Application Note* (document number AN2340/D).

10.8.3 UART Driver

The UART driver is highly dependent on the HW and the operating system of the host system. However, it must conform to the following rules:

1. Transmit and receive at 9600Baud, 8Bit, 1 StopBit, NoParity.
2. Ability to change Baudrate, if needed, in this application.
3. Support handshake on RTS/CTS lines, if needed, in this application. Refer to *MC71000/MC72000 Wake-Up, Reset, and Host Clock Request Sequences Application Note* (document number AN2340/D) for more details.
4. Support sleepmode, if needed, in this application. Refer to *MC71000/MC72000 Wake-Up, Reset, and Host Clock Request Sequences Application Note* (document number AN2340/D) for more details.
5. A delay of more than 300 mS between characters in a command results in a “Hardware Error” event returned, telling to retransmit the last telegram. This will impact general speed and should be avoided.

10.8.4 Parser/Router

There are three possible ways to implement the file system. Each has great impact on the way the Parser / Router part has to be implemented, as well as cost and hardware. For details, see the following subsections.

10.8.4.1 General File System on Host

This saves the EEPROM and can use an existing file system on the host.

The router must do the following things:

1. Sort all commands/events/ACL/SCO and send it to correct receiver.
2. Send host connect after reset.
3. Change baud rate after host connect, if needed.
4. Resend telegrams on “Hardware error” event received, if needed.
5. Keep track of number of pending commands.

The parser has to do the following things:

1. Translate received file system events into local file system calls.
2. Send correct command, with data, on received file system events.

3. No action necessary on “Command Complete” events.

Some way of reprogramming the files on the host must be considered.

For more details, see *Motorola Bluetooth File System, Host-based General Application Note* (document number 94001481003)

10.8.4.2 One-File File System Downloaded to RAM in MC72000

This will download an image of all files to RAM in MC72000. This saves the EEPROM and no parser/router must be present when running application and upper stack code.

The download of this image is done once under the initialization of the MC72000.

This functionality will be available from ROM 2.1.

No EEPROM is needed, but the host must have initialization software that can make host connect and send one file after all resets. Furthermore, the host must store link keys, if needed, and send those after each reset.

For more details, see *Motorola Bluetooth File System, Host Based One File Application Note* (document number 94001481004).

10.8.4.3 File System in EEPROM on MC72000

An EEPROM containing the files is connected to the MC72000. The parser/router part does not exist in this configuration and the upper stack are directly connected to the UART driver.

Some way of reprogramming the EEPROM normally must be considered. This can be done through JTAG with special programming, or directly through UART interface with a parser program.

This solution will add the cost of an EEPROM but will keep the host software simple.

For more details, see *Motorola Bluetooth File System, Embedded File System Application Note* (document number 94001481002).

10.8.5 Files

To make the MC72000 as flexible as possible, the following files have been defined as shown in Table 67.

Table 67. Filename Description

Filename	Name	Description
1000	Boot image	This file is the boot program that controls startup.
2000	Patch	This file contains the patch code. Enabling new features or correcting errors in existing functions in ROM or RAM.
3000	OEM application	The application file contains the customer specific application.
3500	Headset config.	Configuration for a headset application.
3600	UART config.	Configuration for a UART-based application.
3fff	Production test code	Code-specific for testing the MC72000 and the radio module in a test environment.
4000	Baseband NVM	NVM parameters for the baseband (i.e., Bluetooth address, link keys, country code and sleep mode setup, etc.)
4100	Radio parameters/patch	Radio register values in different setups and software patch code for the radio.
4200	Production data	Hardware name string, serial number, revision etc.
5500	ROM image	The ROM image file is a copy of complete EEPROM.
6500	RAM image	The image of a file system to be accessed from RAM.

Not all of the files will be present in all configurations. Refer to *Motorola Bluetooth File System, Host-based General Application Note* (document number 94001481003), *Motorola Bluetooth File System, Host-Based One File Application Note* (document number 94001481004) and *Motorola Bluetooth File System, Embedded File System Application Note* (document number 94001481002) for more details.

All files are created by tools or provided by Motorola.

10.8.6 File Loading

The files will typically be loaded in the following sequence for a host-based general file system using ROM, with a UART application (see Figure 91 for an example).

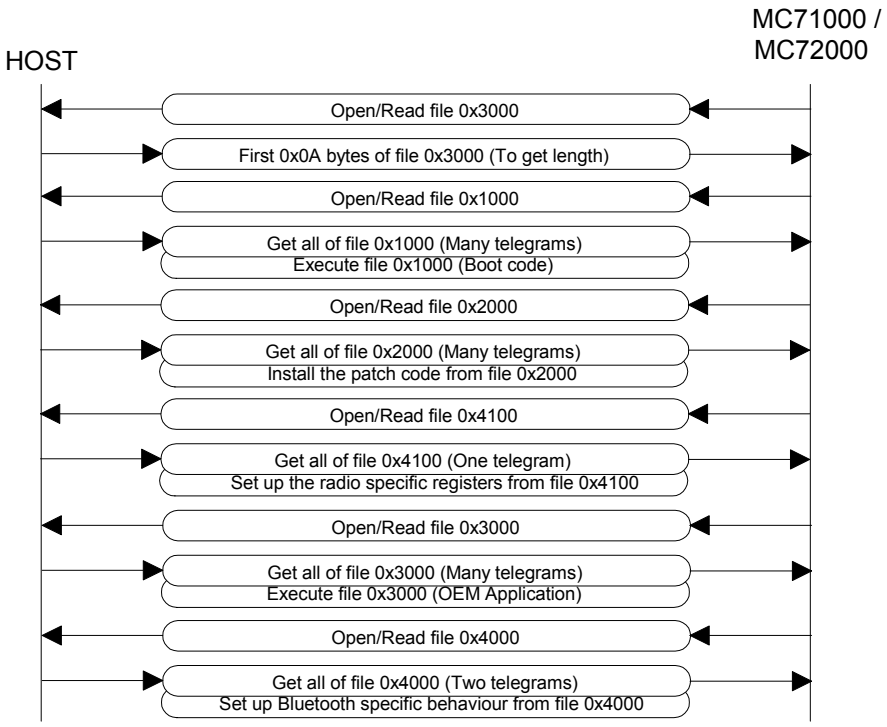


Figure 91. File Loading Example

Refer to *Motorola Bluetooth File System, Embedded File System Application Note* (document number 94001481002) for more details.

10.8.7 Possible EEPROM Types

The following EEPROM types can be considered for use in the systems with an embedded EEPROM (see Table 68).

Note that the speed depends on the applied voltage and the EEPROM type chosen. The speed in the table is the one chosen by Motorola. Customers can change this by changing a number in a file.

Table 68. EEPROMs

Type	Size	Speed
SST 45LF/VF512	64 kBytes	6.00 MHz
SST 45LF/VF010	128 kBytes	6.00 MHz
SST 45LF/VF020	256 kBytes	6.00 MHz
ATMEL AT25P1024	128 kBytes	1.50 MHz
ATMEL AT25HP512	64 kBytes	1.50 MHz
ATMEL AT25HP256	32 kBytes	1.50 MHz
ATMEL AT25256	32 kBytes	1.50 MHz
ATMEL AT25128	16 kBytes	1.50 MHz

Table 68. EEPROMs (Continued)

Type	Size	Speed
ATMEL AT25640	8 kBytes	1.50 MHz
ATMEL AT25320	4 Kbytes	1.50 MHz
ST M95320	4 kBytes	1.50 MHz
ST M95640	8 kBytes	1.50 MHz
ST M95128	16 kBytes	1.50 MHz
ST M95256	32 kBytes	1.50 MHz
Microchip 25640	8 kBytes	1.50 MHz

10.9 Audio

A key feature of Bluetooth is its native quality-of-service (QoS) supporting audio at both the link and application levels. A key component of Motorola's approach to delivering high quality audio over Bluetooth is the Bluetooth Audio Signal Processor (BTASP) that has been designed into the MC72000.

The Bluetooth Audio Signal Processor (BTASP) is a dedicated module that handles all computation-intensive audio functionality in a Bluetooth system. Bluetooth supports voice links compressed with either log-PCM (A-law or μ-law) or CVSD. A voice link is duplex and the data rate is fixed at 64 kbit/s.

Four different packet types are defined: HV1, HV2, HV3 packets with 10, 20, or 30 bytes of encoded audio, and DV packets with 10 bytes of encoded audio and up to 9 bytes of ACL data. SCO packets are single-slot packets sent at fixed intervals. Multiple simultaneous SCO links are possible if HV2 or HV3 packets are used.

Powerful 6th order IIR filtering will band limit the signal according to the Bluetooth requirements. 60dB stop band attenuation is easily achieved. This is important to avoid imaging and aliasing in the up/down-sampling. The audio quality is significantly better when compared to a 4th order IIR filter. The IIR filter also provides extremely low audio latency that is essential in many applications. In duplex applications, such as a headset, a too high latency may necessitate the use of echo cancellers. The filter noise floor is close to -100dB, and will not degrade the quality possible within the Bluetooth audio specification.

The included DC blocker will remove any potential DC-offset from the signal in order to minimize packet loss effects.

The Bluetooth clock and the CODEC sample clock are not synchronous and may drift. Therefore, it is necessary to synchronize data to/from a CODEC with the Bluetooth clock. For this reason, the BTASP includes a second order interpolation algorithm. The interpolator provides a way to stretch or compress the number of available samples to what is needed, providing a quality far superior to simpler synchronization schemes such as repeating or discarding samples. The setup and control of the interpolator is handled by software so the synchronization and choice of CODEC is highly flexible.

The BTASP implements all signal processing needed to support a maximum of three simultaneous audio links using all the defined compression/decompression standards. The BTASP will also handle Bluetooth/CODEC synchronization.

BTASP key features:

- Overall system pass-band is 280 Hz to 3.45 kHz (-3 dB), measured with white noise.
- Out-of-band attenuation above 4 kHz is at least 80 dB, measured with white noise.
- SNR at 1.020 kHz with maximal signal level (max. volume setting) is above 60 dB, measured with a 1.020 kHz fixed sine.
- The latency measured with a short sine pulse (one-way latency) is as follows:
  - Using HV1 packets: 4.9 ms
  - Using HV2 packets: 6.1 ms
  - Using HV3 packets: 7.4 ms
- Phase jitter: < 5° C measured for a 1.020 kHz sine.

10.10 Timing and Low Power Mode

The timing for the Power on reset (POR) and the implementation of the low power modes is thoroughly described in *MC71000/MC72000 Wake-Up, Reset, and Host Clock Request Sequences Application Note* (document number AN2340/D).

10.11 UART Interface

The host interface is a standard HCI UART (H:4) transport layer, where all communication from application, upper stack and file system passes through.

The UART transport layer supports baud rate ranging from 1200 to 1843200 bit/s.

The MC72000 UART interface can be configured to be a 4-, 5-, or 6-wire interface.

The default baud rate upon start up can be configured. See *Motorola Bluetooth File System, Overview Application Note* (document number 94001481001), *UART/SSI Configuration User´s Guide* (document number 94001481900) and *Motorola Bluetooth File System, Host-based General Application Note* (document number 94001481003) for more details.

10.12 JTAG Interface

The JTIC interface intended for debug and production test purposes, may be wired to an external JTAG controller. In this case, refer to the external document *Production Test Application Note* (document number 94001481100) in Section 5.2, “Document References,” and other implementation guidance documents in this section.

If JTAG is omitted from design, all JTAG interface pins must be left open. TRST_B may be pulled-down and TMS may be pulled-up to enhance reliability, and to ensure that the JTAG interface stays disabled at all times. All JTAG input pins has internal pull-up/downs and cannot be disabled as normal GPIO pins can.

10.13 Production Test

All issues regarding the production with regards to vendor-specific command and setup are explained thoroughly in *Production Test Application Note* (document number 94001481100)

10.14 Bluetooth Qualification

For information on Bluetooth Qualification, see *Motorola Bluetooth Solutions, Bluetooth Qualification application note* (document number AN2386/D).

11 Application Example Evaluation Printed Circuit Boards

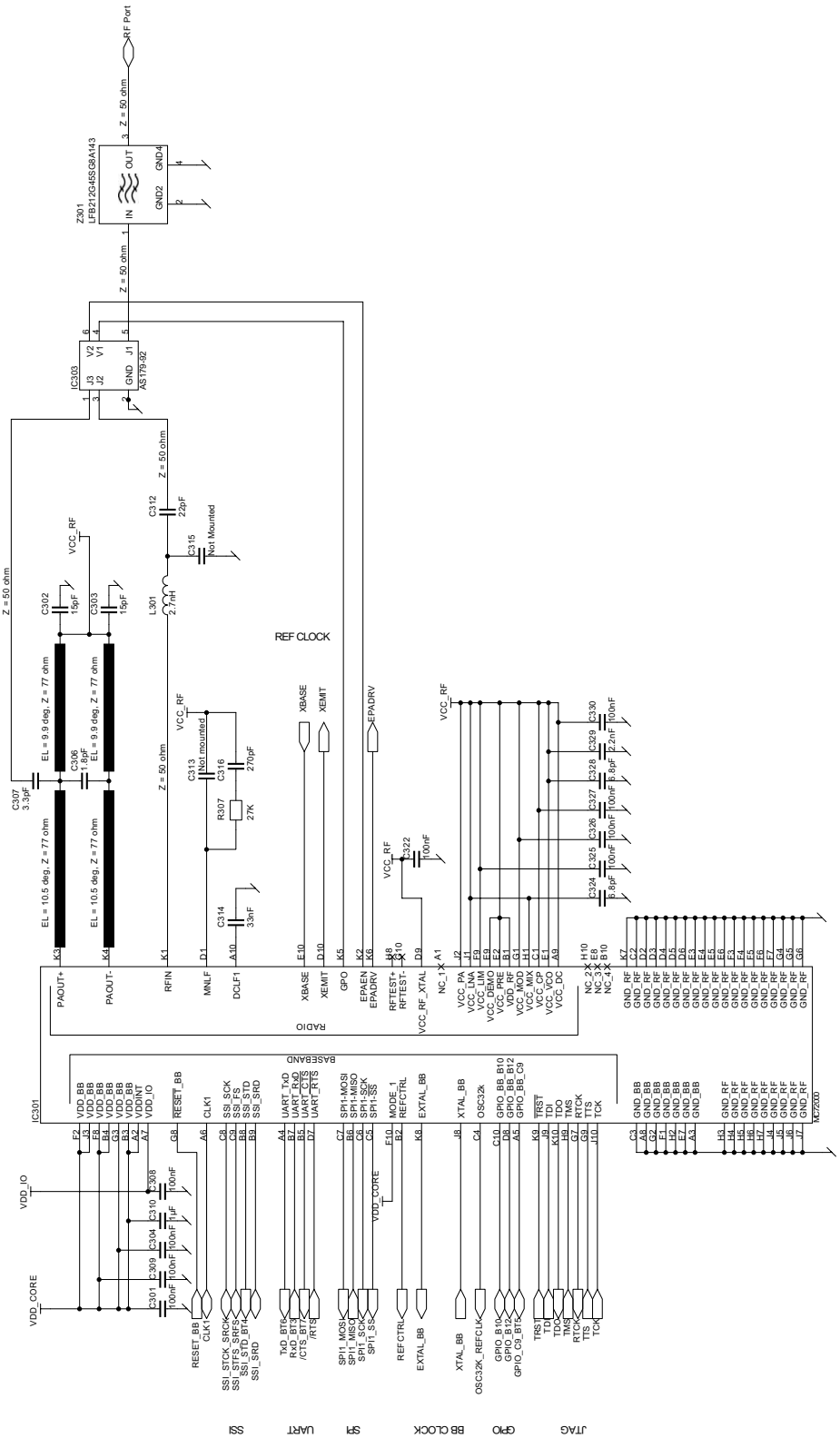


Figure 92. Application Example Evaluation Schematic

12 Mechanical Outline (Package Information)

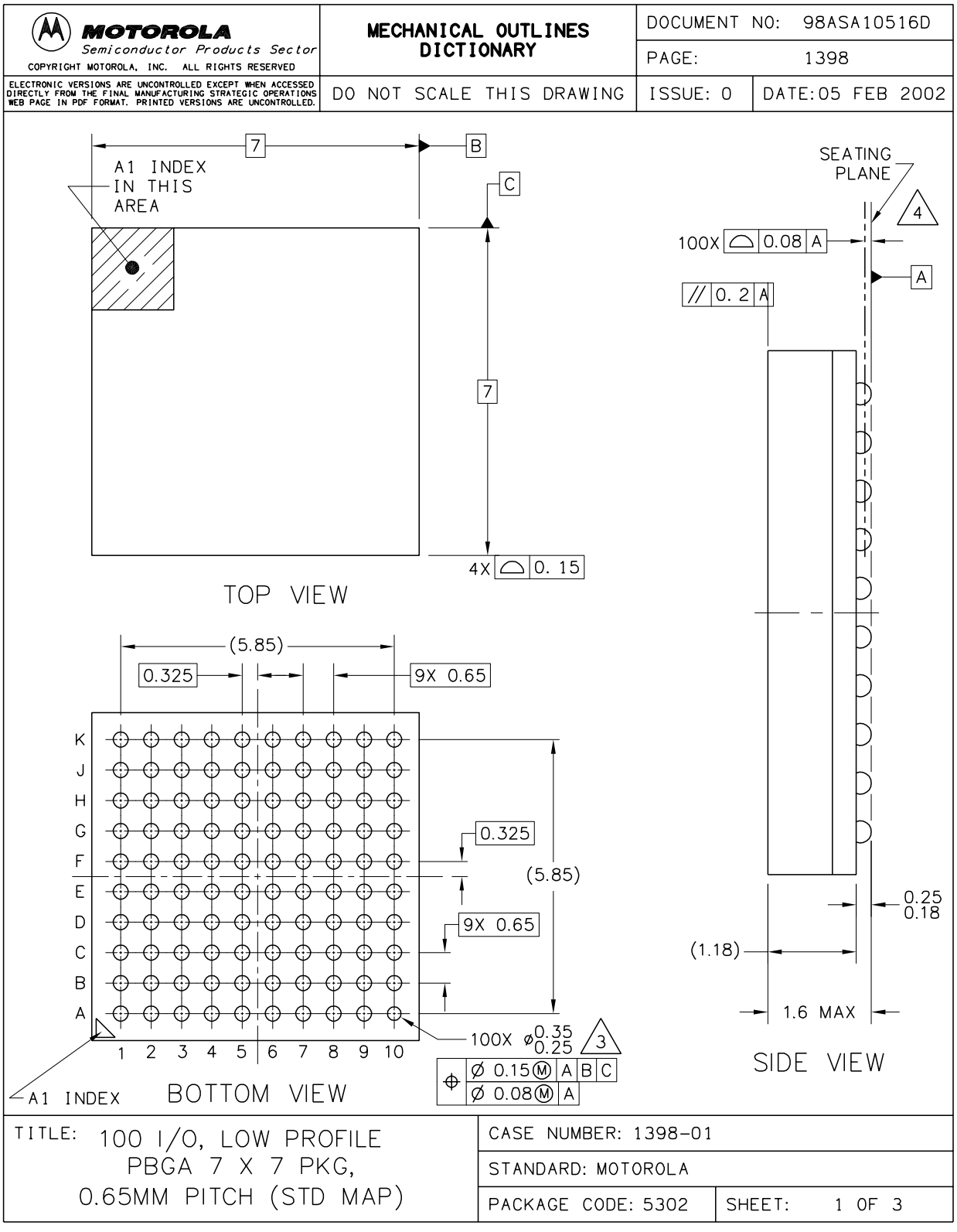


Figure 93. 100 MAPBGA Package Diagram 7 mm x 7 mm x 1.6 mm

Appendix A: Radio Register Map

The following figure shows the MC72000 Radio Register Map.

MC72000		Byte 1								Byte 0							
Register Address	Register Number	MSB Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
$00 Programmable Reset																	
$01	1	MSB	16 Bit Frac-N Numerator Divide Value - num														LSB
Rx Test	$37FA	0	0	1	1	0	1	1	1	1	1	1	1	1	0	1	0
Tx Test	$C1D2	1	1	0	0	0	0	0	1	1	1	0	1	0	0	1	0
$02	2	Sleep Enable	Tx Enable	Rx Enable	Narrow Bandwidth Enable	High/Low Injection Enable			General Purpose Output	MSB	Frac-N Integer Divide Value						LSB
Rx Test	$2CB9	0	0	1	0	1	1	0	0	1	0	1	1	1	0	0	1
Tx Test	$55B8	0	1	0	1	0	1	0	1	1	0	1	1	1	0	0	0
$03	3						External PA Enable Invert				General Purpose Output Invert	MSB	PA DAC Setting				LSB
	$4180	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0
$04	4										RSSI Read Enable						
	$78D9	0	1	1	1	1	0	0	0	1	1	0	1	1	0	0	1
$05	5														MSB	PA Bias Adjust	LSB
	$28BA	0	0	1	0	1	0	0	0	1	0	1	1	1	0	1	0
$06	6	External PA Enable = GPO	MSB	Xtal Trim			LSB	z	DC PII R Counter								LSB
	$C28A	1	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0
$07	7	MSB	Dual Port Programmable Delay For Tx PLL			LSB	MSB	DC PII N Counter									LSB
	$9CB0	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0
$08	8	MSB	Transmit Synchronization Time Delay Value						LSB	MSB	B-Dual Port Digital Multiplier Value For Tx PLL						LSB
	$B862	1	0	1	1	1	0	0	0	0	1	1	0	0	0	1	0
$09	9								RSSI Enable								
	$7FDF	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
$0A	10																
	$5FFF	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
$0B	11									External PA DAC Enable	External PA Enable		Xtal Boost Enable				Xtal Enable
	$FF6F	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1
$0C	12	MSB	ROM_r2_c2						LSB	MSB	ROM_r1_c1						LSB
	$C6C6	1	1	0	0	0	1	1	0	1	1	0	0	0	1	1	0
$0D	13	MSB	ROM_r2_c4						LSB	MSB	ROM_r2_c3						LSB
	$C0C5	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	1
$0E	14	MSB	ROM_r3_c2						LSB	MSB	ROM_r3_c1						LSB
	$6825	0	1	1	0	1	0	0	0	0	0	1	0	0	1	0	1
$0F	15	MSB	ROM_r3_c4						LSB	MSB	ROM_r3_c3						LSB
	$B498	1	0	1	1	0	1	0	0	1	0	0	1	1	0	0	0
$10	16	MSB	ROM_r4_c3						LSB	MSB	ROM_r4_c2						LSB
	$9668	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	0
$11	17	MSB	M-Dual Port Digital Multiplier Value For Tx PLL						LSB	MSB	ROM_r4_c4						LSB
	$65AD	0	1	1	0	0	1	0	1	1	0	1	0	1	1	0	1

Figure 94. MC72000 Radio Register Map

NOTES

Freescale Semiconductor, Inc.

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P.O. Box 5405, Denver, Colorado 80217
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3-20-1, Minami-Azabu Minato-ku, Tokyo 106-8573 Japan
81-3-3440-3569

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MC72000/D

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