Hex Buffer

The MC74LVX50 is an advanced high speed CMOS buffer fabricated with silicon gate CMOS technology.

The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: $t_{PD} = 4.1 \text{ ns (Typ)}$ at $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2 \mu A \text{ (Max)}$ at $T_A = 25 \text{°C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% \ V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 3.6 V Operating Range
- Low Noise: $V_{OLP} = 0.5 \text{ V (Max)}$
- Pb-Free Packages are Available*

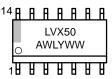


http://onsemi.com

MARKING DIAGRAMS



SOIC-14 **D SUFFIX CASE 751A**



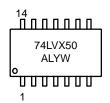


TSSOP-14 **DT SUFFIX CASE 948G**





SOEIAJ-14 **M SUFFIX CASE 965**



Assembly Location

WL or L Wafer Lot Year WW or W =Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

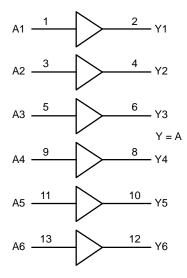


Figure 1. Logic Diagram

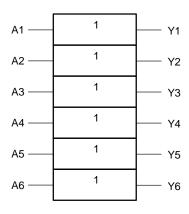
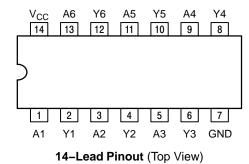


Figure 2. Logic Symbol



FUNCTION TABLE

A Input	Y Output
L	L
Н	Н

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVX50D	SOIC-14	55 Units / Rail
MC74LVX50DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74LVX50DR2	SOIC-14	2500 Tape & Reel
MC74LVX50DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LVX50DT	TSSOP-14*	96 Units / Rail
MC74LVX50DTR2	TSSOP-14*	2500 Tape & Reel
MC74LVX50M	SOEIAJ-14	50 Units / Rail
MC74LVX50MG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC74LVX50MEL	SOEIAJ-14	2000 Tape & Reel
MC74LVX50MELG	SOEIAJ-14 (Pb-Free)	2000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb–Free.

MAXIMUM RATINGS

Symbol	Parame	ter	Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to $+7.0$	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V	
V _{OUT}	DC Output Voltage		-0.5 to $V_{CC} + 0.5$	V
I _{IK}	DC Input Diode Current	V _I < GND	-20	mA
I _{OK}	DC Output Diode Current	V _O < GND	±20	mA
I _{OUT}	DC Output Sink Current		±25	mA
I _{CC}	DC Supply Current per Supply Pin	±50	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 S	260	°C	
TJ	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	(Note 1) SOIC TSSOP	125 170	°C/W
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94-V0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 2000	V
I _{Latchup}	Latchup Performance Above	e V _{CC} and Below GND at 85°C (Note 5)	±300	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
- 2. Tested to EIA/JESD22-A114-A.
- 3. Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.
- 5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	2.0	3.6	V
VI	Input Voltage (Note 6)	0	5.5	V
Vo	Output Voltage (HIGH or LOW State)	0	V _{CC}	V
T _A	Operating Free–Air Temperature	-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate $V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$	0	100	ns/V

^{6.} Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

NOTE: The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DC ELECTRICAL CHARACTERISTICS

			Vcc	7	Γ _A = 25°0	2	T _A ≤	85°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Unit
V _{IH}	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V _{IL}	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V _{OH}	High-Level Output Voltage (V _{IN} = V _{IH} or V _{IL})	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V _{OL}	Low-Level Output Voltage (V _{IN} = V _{IH} or V _{IL})	I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 3.6			±0.1		±1.0	μΑ
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	3.6			2.0		20.0	μΑ

AC ELECTRICAL CHARACTERISTICS Input $t_f = t_f = 3.0 \text{ ns}$

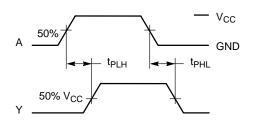
					T _A = 25°C		$T_A \le 85^{\circ}C$		
Symbol	Parameter	Test Cond	ditions	Min	Тур	Max	Min	Max	Unit
t _{PLH} ,	Propagation Delay, Input A to Y	V _{CC} = 2.7 V	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		5.4 7.9	10.1 13.6	1.0 1.0	12.5 16.0	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		4.1 6.6	6.2 9.7	1.0 1.0	7.5 11.5	
toshl	Output-to-Output Skew	V _{CC} = 2.7 V	C _L = 50 pF			1.5		1.5	ns
toslh	(Note 7)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{V}$	C _L = 50 pF			1.5		1.5	
C _{IN}	Input Capacitance				4	10		10	pF
				Ty	pical @	25°C, V	_{CC} = 3.3	٧	
C _{PD}	Power Dissipation Capacitance (Note 8)					15			pF

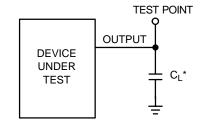
Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

NOISE CHARACTERISTICS Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V

		T _A = 25°C		
Symbol	Characteristic	Тур	Max	Unit
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.3	0.5	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.3	-0.5	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

^{8.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.





*Includes all probe and jig capacitance Figure 4. Test Circuit

Figure 3. Switching Waveforms

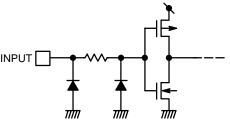
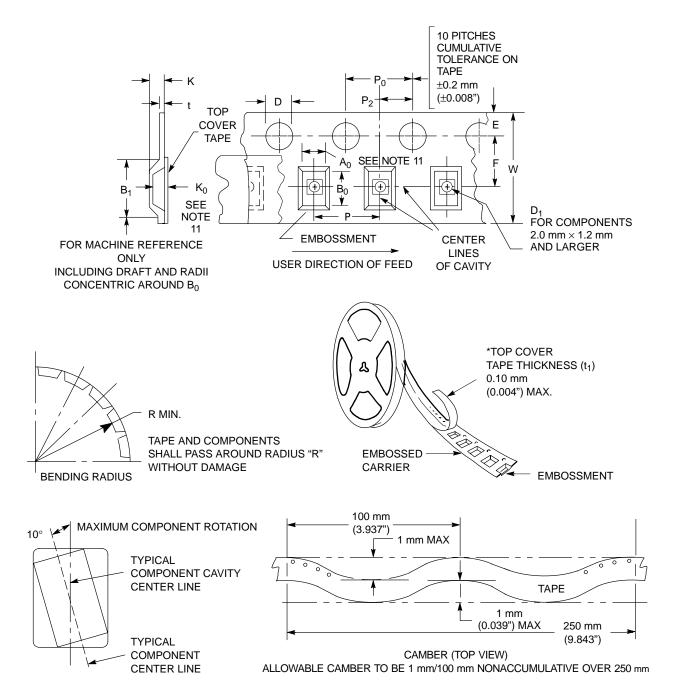


Figure 5. Input Equivalent Circuit

EMBOSSED CARRIER DIMENSIONS (See Notes 9 and 10)

Tape Size	B ₁ Max	D	D ₁	E	F	К	Р	P ₀	P ₂	R	т	w
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 -0.0 (0.059"	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024)	8.3 mm (0.327)
12 mm	8.2 mm (0.323")	+0.004 -0.0)	1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")			30 mm (1.18")		12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642)
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957)

^{9.} Metric Dimensions Govern–English are in parentheses for reference only. 10. A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity



11. A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

Figure 6. Carrier Tape Specifications

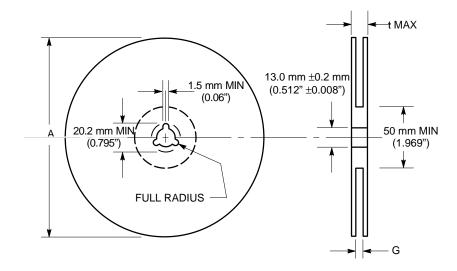


Figure 7. Reel Dimensions

REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")
8 mm	T3, T4	330 mm (13")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")
12 mm	R2	330 mm (13")	12.4 mm, +2.0 mm, -0.0 (0.49" + 0.079", -0.00)	18.4 mm (0.72")
16 mm	R2	360 mm (14.173")	16.4 mm, +2.0 mm, -0.0 (0.646" + 0.078", -0.00)	22.4 mm (0.882")
24 mm	R2	360 mm (14.173")	24.4 mm, +2.0 mm, -0.0 (0.961" + 0.078", -0.00)	30.4 mm (1.197")

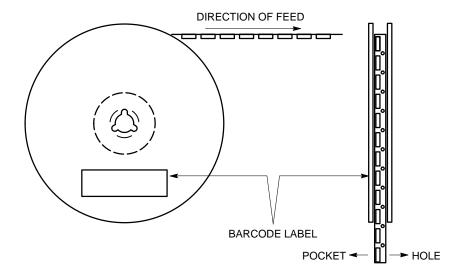


Figure 8. Reel Winding Direction

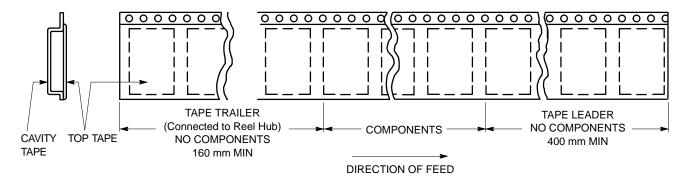


Figure 9. Tape Ends for Finished Goods

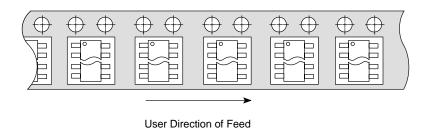


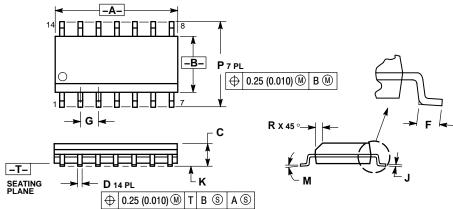
Figure 10. TSSOP and SOIC R2 Reel Configuration/Orientation

TAPE UTILIZATION BY PACKAGE

Tape Size	SOIC	TSSOP	QFN	SC88A / SOT-353 SC88/SOT-363
8 mm				5-, 6-Lead
12 mm	8-Lead	8-, 14-, 16-Lead	8-, 14-, 16-Lead	
16 mm	14-, 16-Lead	20-, 24-Lead	20-, 24-Lead	
24 mm	18-, 20-, 24-, 28-Lead	48-, 56-Lead	48-, 56-Lead	

PACKAGE DIMENSIONS

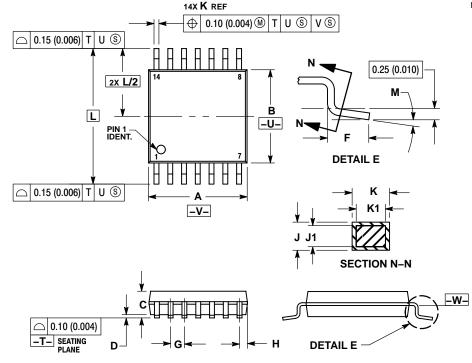
SOIC-14 **D SUFFIX** CASE 751A-03 ISSUE G



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE
 DAMBAR PROTRUSION. ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.127
 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
М	0 °	7°	0 °	7°
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP-14 **DT SUFFIX** CASE 948G-01 **ISSUE A**



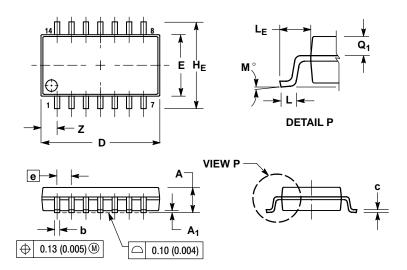
NOTES:

- DIMENSIONING AND TOLERANCING PER
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 MIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 DIMENSION K DOES NOT INCLUDE
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE
- DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40 BSC		0.252	BSC	
M	0°	8 °	0°	8 °	

PACKAGE DIMENSIONS

SOEIAJ-14 **M SUFFIX** CASE 965-01 **ISSUE O**



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
 THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10°
Q ₁	0.70	0.90	0.028	0.035
Z		1.42		0.056

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