MOTOROMA^{88913供应商} SEMICONDUCTOR TECHNICAL DATA

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MC88913

LOW SKEW CMOS

CLOCK DRIVER

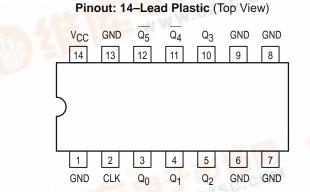
from Logic Marketing

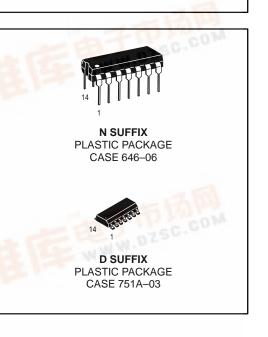
Low Skew CMOS Clock Driver

The MC88913 is a high–speed, low power, hex divide–by–two D–type flip–flop with two inverting and four non–inverting outputs that have closely matched propagation delays. With a TTL compatible buffered clock input that is common to all flip–flops, the MC88913 is ideal for use in high–frequency systems as a clock driver, providing multiple outputs that are synchronous.

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- Minimum Clock Input fMAX of 110MHz
- TTL Compatible Positive Edge–Triggered Clock
- Matched Outputs for Synchronous Applications
- Outputs Source/Sink 24mA
- Part-to-Part Skew of Less Than 4.0ns
- · Guaranteed Rise and Fall Times for a Given Capacitive Load





MAXIMUM RATINGS*

Symbol	Parameter		Value	Units
Vcc	DC Supply Voltage (Referenced to GND)		-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)		-0.5 to V _{CC} + 0.5	V
Vout	DC Output Voltage (Referenced to GND)	- 18	-0.5 to V _{CC} + 0.5	V
l _{in}	DC Input Current, per Pin	190 10	±20	mA
lout	DC Output Sink/Source Current, per Pin		± 50	mA
ICC	DC V _{CC} or GND Current per Output Pin		± 50	mA
PD		ic Package** C Package**	750 500	mW
T _{stg}	Storage Temperature		-65 to +150	°C
ТL	Lead Temperature, 1mm from Case for 10s (Plastic Package)	or SOIC	260	°C

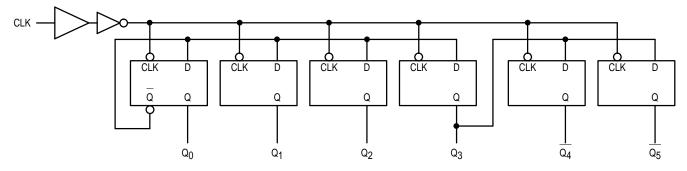
* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Derating) F Plastic Package: -10mW/°C from 65°C to 125°C

SOIC Package: -7.0mW/°C from 65°C to 125°C

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LOGIC DIAGRAM



NOTE: This diagram is provided only for understanding of logic operation and should not be used to estimate propagation delays

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VCC	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	VCC	V
Т _А	Operating Temperature	-40	+85	°C
t _r , t _f	Input Rise and Fall Time V _{in} from 0.8 to 2.0V V _{meas} from 0.8 to 2.0V	0 0	10 8.0	ns/V

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter		Unit	Condition
ICC	Maximum Quiescent Supply Current	80	μΑ	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$, $T_A = Worst Case$
ICC	Maximum Quiescent Supply Current	8.0	μΑ	$V_{IN} = V_{CC} \text{ or GND}$ $V_{CC} = 5.5V,$ $T_A = 25^{\circ}C$
ICCT	Maximum Additional I _{CC} /Input	1.5	mA	$V_{IN} = V_{CC} - 2.1V$ $V_{CC} = 5.5V$, $T_A = Worst Case$

AC OPERATING REQUIREMENTS

			Тд = СL =	T _A = 25°C C _L = 50 pF		T _A = -40 to +85°C C _L = 50 pF	
Symbol	Parameter	V _{CC} (V)	Min	Max	Min	Max	Unit
tw	CLK Pulse Width (HIGH to LOW)	5.0	3.0		3.0		ns

CAPACITANCE

Symbol	Parameter	Тур	Unit	Condition
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	30	pF	V _{CC} = 5.0V

DC CHARACTERISTICS

			T _A =	+25°C	T _A = −40 to +85°C		
Symbol	Parameter	Vcc	Тур	Gua	aranteed Max	Unit	Conditions
VIH	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1V \text{ or}$ $V_{CC} - 0.1V$
VIL	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1 V \text{ or}$ $V_{CC} - 0.1 V$
Voh	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = -50μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	VIN = VIL or VIH IOH = -24mA -24mA
VOL	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{OH} = 24\text{mA}$ 24mA
I _{IN}	Maximum Input	5.5		±0.1	±0.1	μA	V _I = V _{CC} , GND
ІССТ	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	$V_{I} = V_{CC} - 2.1 V$
IOLD	Minimum Dynamic Output Current**	5.5			75	mA	V _{OLD} = 1.65V
IOHD]	5.5			-75	mA	V _{OHD} = 3.85V

* All outputs loaded; thresholds on inputs associated with output under test.
** Maximum test duration 20ms, one output at a time.

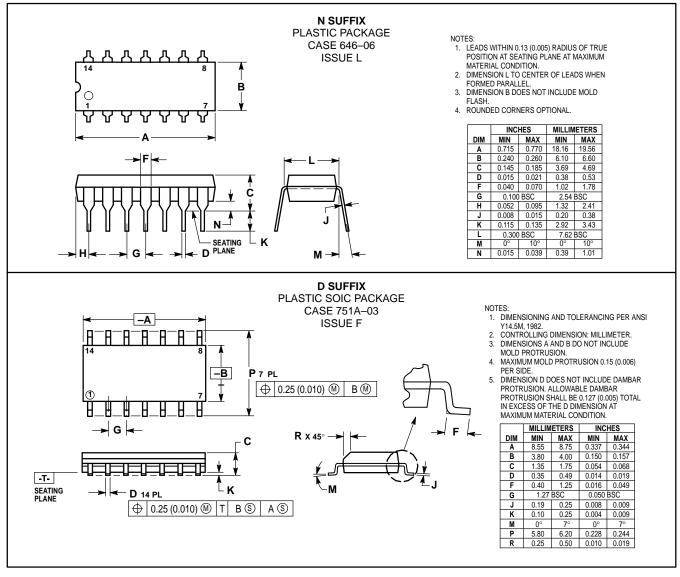
AC CHARACTERISTICS (V_{CC} = $5.0V \pm 10\%$)

			TA = 25°C CL = 50 pF		T _A = -40 to +85°C C _L = 50 pF		
Symbol	Parameter	V _{CC} (V)	Min	Max	Min	Max	Unit
fMAX	Maximum Clock Frequency (50% Duty Cycle)	5.0	110		110		MHz
^t PLH [,] ^t PHL	Propagation <u>D</u> elay CLK to Q _n , Q _n	5.0	4.0	10.5	4.0	11.5	ns
^t PV	Propagation Delay Variation CLK to Q_0 , Q_1 , Q_2 (see Note 1)	5.0		4.0		5.0	ns
	Propagation Delay Variation CLK to All Outputs (see Note 1)	5.0		4.5		5.5	ns
^t PS	Propagation Delay Skew (Q ₀ , Q ₁ , Q ₂) tp _{HL} Actual – tp _{LH} Actual	5.0		1.0		1.0	ns
	Propagation Delay Skew (All Outputs) tpHL Actual – tpLH Actual	5.0		1.5		1.5	ns
tOS	Output–to–Output Skew (Q ₀ , Q ₁ , Q ₂) $ t_p Q_n - t_p Q_m $ (see Note 2)	5.0		1.0		1.0	ns
	Output–to–Output Skew (All Outputs) $ t_p Q_n - t_p Q_m $ (see Note 2)	5.0		1.5		1.5	ns
t _{rise} ^t fall	Rise/Fall Time for Q_0 , Q_1 , Q_2 (0.2 x V _{CC} to 0.8 x V _{CC})	5.0		3.0		4.0	ns
	Rise/Fall Time for All Outputs $(0.2 \times V_{CC} \text{ to } 0.8 \times V_{CC})$	5.0		3.5		4.5	ns

1. For a given set of conditions (i.e., capacitive load, temperature and V_{CC}) the variation from device to device is guaranteed to be less than or equal to the maximum. 2. Where $t_p Q_n$ and $t_p Q_m$ are the actual propagation delays (any combination of HIGH or LOW) for any two separate outputs from a given high transition of CLK.

MC88913

OUTLINE DIMENSIONS



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