

## Open-Drain Output Sub-Microamp Comparators

### Features

- Low Quiescent Current: 600 nA/comparator (typ.)
- Rail-to-Rail Input:  $V_{SS} - 0.3V$  to  $V_{DD} + 0.3V$
- Open-Drain Output:  $V_{OUT} \leq 10V$
- Propagation Delay: 4  $\mu s$  (typ., 100 mV Overdrive)
- Wide Supply Voltage Range: 1.6V to 5.5V
- Single available in SOT-23-5, SC-70-5 \* packages
- Available in Single, Dual and Quad
- Chip Select ( $\overline{CS}$ ) with MCP6548
- Low Switching Current
- Internal Hysteresis: 3.3 mV (typ.)
- Temperature Range:
  - Industrial:  $-40^{\circ}C$  to  $+85^{\circ}C$
  - Extended:  $-40^{\circ}C$  to  $+125^{\circ}C$

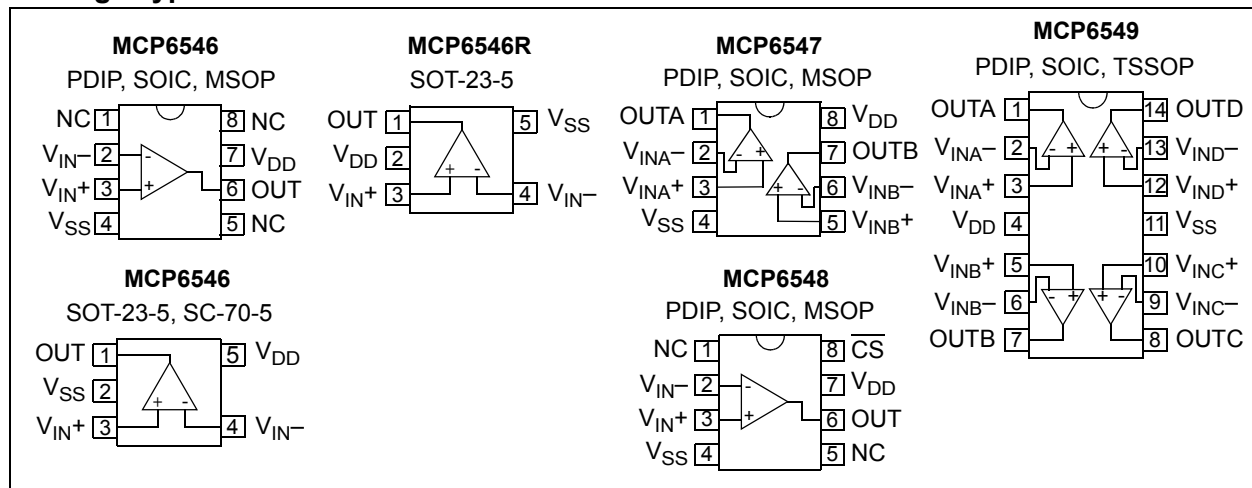
### Typical Applications

- Laptop Computers
- Mobile Phones
- Metering Systems
- Hand-held Electronics
- RC Timers
- Alarm and Monitoring Circuits
- Windowed Comparators
- Multi-vibrators

### Related Devices

- CMOS/TTL-Compatible Output: MCP6541/2/3/4

### Package Types



### Description

The Microchip Technology Inc. MCP6546/7/8/9 family of comparators is offered in single (MCP6546), single with chip select (MCP6548), dual (MCP6547) and quad (MCP6549) configurations. The outputs are open-drain and are capable of driving heavy DC or capacitive loads.

These comparators are optimized for low power, single-supply application with greater than rail-to-rail input operation. The output limits supply current surges and dynamic power consumption while switching. The open-drain output of the MCP6546/7/8/9 family can be used as a level-shifter for up to 10V using a pull-up resistor. It can also be used as a wired-OR logic. The internal Input hysteresis eliminates output switching due to internal noise voltage, reducing current draw. These comparators operate with a single-supply voltage as low as 1.6V and draw a quiescent current of less than 1  $\mu A$ /comparator.

The related MCP6541/2/3/4 family of comparators from Microchip has a push-pull output that supports rail-to-rail output swing and interfaces with CMOS/TTL logic.

\* SC-70-5 E-Temp parts not available at this release of the data sheet.

# MCP6546/7/8/9

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....	7.0V
Open-Drain output.....	$V_{SS} + 10.5V$
All other inputs and outputs .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input voltage .....	$ V_{DD} - V_{SS} $
Output Short-Circuit Current .....	continuous
Current at Input Pins .....	$\pm 2$ mA
Current at Output and Supply Pins .....	$\pm 30$ mA
Storage temperature .....	$-65^{\circ}C$ to $+150^{\circ}C$
Maximum Junction Temperature ( $T_J$ ).....	$+150^{\circ}C$
ESD protection on all pins (HBM;MM) .....	4 kV;200V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = 25^{\circ}C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = V_{SS}$ ,  $R_{PU} = 2.74$  k $\Omega$  to  $V_{PU} = V_{DD}$  (Refer to Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	1.6	—	5.5	V	$V_{PU} \geq V_{DD}$
Quiescent Current (per comparator)	$I_Q$	0.3	0.6	1	$\mu A$	$I_{OUT} = 0$
<b>Input</b>						
Input Voltage Range	$V_{CMR}$	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common Mode Rejection Ratio	CMRR	55	70	—	dB	$V_{DD} = 5V$ , $V_{CM} = -0.3V$ to $5.3V$
Common Mode Rejection Ratio	CMRR	50	65	—	dB	$V_{DD} = 5V$ , $V_{CM} = 2.5V$ to $5.3V$
Common Mode Rejection Ratio	CMRR	55	70	—	dB	$V_{DD} = 5V$ , $V_{CM} = -0.3V$ to $2.5V$
Power Supply Rejection Ratio	PSRR	63	80	—	dB	$V_{CM} = V_{SS}$
Input Offset Voltage	$V_{OS}$	-7.0	$\pm 1.5$	+7.0	mV	$V_{CM} = V_{SS}$ ( <b>Note 1</b> )
Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	$\pm 3$	—	$\mu V/^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$ , $V_{CM} = V_{SS}$
Input Hysteresis Voltage	$V_{HYST}$	1.5	3.3	6.5	mV	$V_{CM} = V_{SS}$ ( <b>Note 1</b> )
Linear Temp. Co.	$T_{C1}$	—	67	—	$\mu V/^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$ , $V_{CM} = V_{SS}$ ( <b>Note 2</b> )
Quadratic Temp. Co.	$T_{C2}$	—	-0.035	—	$\mu V/^{\circ}C^2$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$ , $V_{CM} = V_{SS}$ ( <b>Note 2</b> )
Input Bias Current	$I_B$	—	1	—	pA	$V_{CM} = V_{SS}$
At Temperature (I-Temp parts)	$I_B$	—	25	100	pA	$T_A = +85^{\circ}C$ , $V_{CM} = V_{SS}$ ( <b>Note 3</b> )
At Temperature (E-Temp parts)	$I_B$	—	1200	5000	pA	$T_A = +125^{\circ}C$ , $V_{CM} = V_{SS}$ ( <b>Note 3</b> )
Input Offset Current	$I_{OS}$	—	$\pm 1$	—	pA	$V_{CM} = V_{SS}$
Common Mode Input Impedance	$Z_{CM}$	—	$10^{13}  4$	—	$\Omega  pF$	
Differential Input Impedance	$Z_{DIFF}$	—	$10^{13}  2$	—	$\Omega  pF$	
<b>Open-Drain Output</b>						
Output Pull-Up Voltage	$V_{PU}$	1.6	—	10	V	( <b>Note 4</b> )
High-Level Output Current	$I_{OH}$	-100	—	—	nA	$V_{DD} = 1.6V$ to $5.5V$ , $V_{PU} = 10V$ ( <b>Note 4</b> )
Low-Level Output Voltage	$V_{OL}$	$V_{SS}$	—	$V_{SS} + 0.2$	V	$I_{OUT} = 2$ mA, $V_{PU} = V_{DD} = 5V$
Short-Circuit Current	$I_{SC}$	—	$\pm 1.5$	—	mA	$V_{PU} = V_{DD} = 1.6V$ ( <b>Note 4</b> )
	$I_{SC}$	—	30	—	mA	$V_{PU} = V_{DD} = 5.5V$ ( <b>Note 4</b> )
Output Pin Capacitance	$C_{OUT}$	—	8	—	pF	

**Note 1:** The input offset voltage is the center of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

**2:**  $V_{HYST}$  at differential temperatures is estimated using:  $V_{HYST}(T_A) = V_{HYST} + (T_A - 25^{\circ}C)TC_1 + (T_A - 25^{\circ}C)^2TC_2$ .

**3:** Input bias current at temperature is not tested for the SC-70-5 package.

**4:** Do not short the output above  $V_{SS} + 10V$ . Limit the output current to Absolute Maximum Rating of 30 mA. The minimum  $V_{PU}$  tested was  $V_{DD}$  before Dec. 2004 (week code 52).

## AC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ , Step = 200 mV, Overdrive = 100 mV,  $R_{PU} = 2.74 k\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36 pF$  (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Fall Time	$t_F$	—	0.7	—	$\mu s$	(Note 1)
Propagation Delay (High-to-Low)	$t_{PHL}$	—	4.0	8.0	$\mu s$	
Propagation Delay (Low-to-High)	$t_{PLH}$	—	3.0	8.0	$\mu s$	(Note 1)
Propagation Delay Skew	$t_{PDS}$	—	-1.0	—	$\mu s$	(Notes 1 and 2)
Maximum Toggle Frequency	$f_{MAX}$	—	225	—	kHz	$V_{DD} = 1.6V$
	$f_{MAX}$	—	165	—	kHz	$V_{DD} = 5.5V$
Input Noise Voltage	$E_N$	—	200	—	$\mu V_{P-P}$	10 Hz to 100 kHz

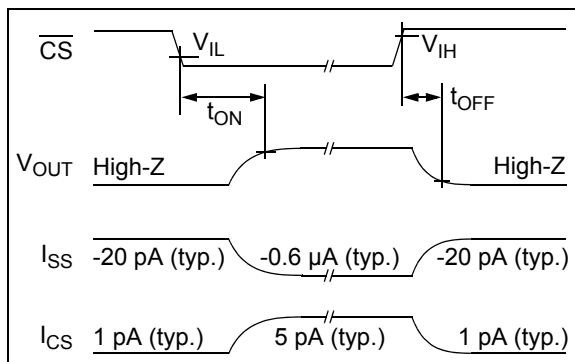
**Note 1:**  $t_R$  and  $t_{PLH}$  depend on the load ( $R_L$  and  $C_L$ ); these specifications are valid for the indicated load only.

**Note 2:** Propagation Delay Skew is defined as:  $t_{PDS} = t_{PLH} - t_{PHL}$ .

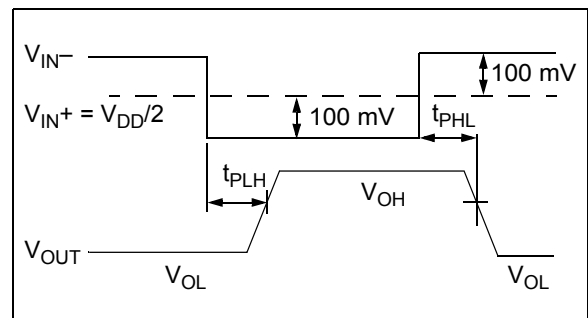
## MCP6548 CHIP SELECT ( $\overline{CS}$ ) CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = V_{SS}$ ,  $R_{PU} = 2.74 k\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36 pF$  (Refer to Figures 1-1 and 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b><math>\overline{CS}</math> Low Specifications</b>						
$\overline{CS}$ Logic Threshold, Low	$V_{IL}$	$V_{SS}$	—	$0.2 V_{DD}$	V	
$\overline{CS}$ Input Current, Low	$I_{CSL}$	—	5	—	pA	$\overline{CS} = V_{SS}$
<b><math>\overline{CS}</math> High Specifications</b>						
$\overline{CS}$ Logic Threshold, High	$V_{IH}$	$0.8 V_{DD}$	—	$V_{DD}$	V	
$\overline{CS}$ Input Current, High	$I_{CSH}$	—	1	—	pA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, $V_{DD}$ Current	$I_{DD}$	—	18	—	pA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, GND Current	$I_{SS}$	—	-20	—	pA	$\overline{CS} = V_{DD}$
Comparator Output Leakage	$I_{O(LEAK)}$	—	1	—	pA	$V_{OUT} = V_{SS} + 10V$ , $\overline{CS} = V_{DD}$
<b><math>\overline{CS}</math> Dynamic Specifications</b>						
$\overline{CS}$ Low to Comparator Output Low Turn-on Time	$t_{ON}$	—	2	50	ms	$\overline{CS} = 0.2V_{DD}$ to $V_{OUT} = V_{DD}/2$ , $V_{IN-} = V_{DD}$
$\overline{CS}$ High to Comparator Output High Z Turn-off Time	$t_{OFF}$	—	10	—	$\mu s$	$\overline{CS} = 0.8V_{DD}$ to $V_{OUT} = V_{DD}/2$ , $V_{IN-} = V_{DD}$
$\overline{CS}$ Hysteresis	$V_{CS\_HYST}$	—	0.6	—	V	$V_{DD} = 5V$



**FIGURE 1-1:** Timing Diagram for the  $\overline{CS}$  pin on the MCP6548.



**FIGURE 1-2:** Propagation Delay Timing Diagram.

# MCP6546/7/8/9

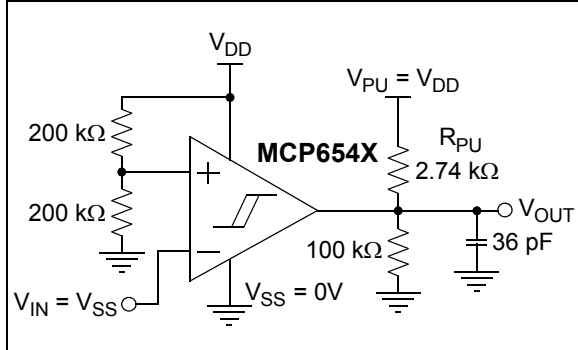
## TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{DD} = +1.6V$ to $+5.5V$ and $V_{SS} = GND$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+85	$^{\circ}C$	
Operating Temperature Range	$T_A$	-40	—	+125	$^{\circ}C$	<b>Note</b>
Storage Temperature Range	$T_A$	-65	—	+150	$^{\circ}C$	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 5L-SC-70	$\theta_{JA}$	—	331	—	$^{\circ}C/W$	
Thermal Resistance, 5L-SOT-23	$\theta_{JA}$	—	256	—	$^{\circ}C/W$	
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	85	—	$^{\circ}C/W$	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	163	—	$^{\circ}C/W$	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	$^{\circ}C/W$	
Thermal Resistance, 14L-PDIP	$\theta_{JA}$	—	70	—	$^{\circ}C/W$	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	120	—	$^{\circ}C/W$	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	$^{\circ}C/W$	

**Note:** The MCP6546/7/8/9 I-temp family operates over this extended temperature range, but with reduced performance. In any case, the Junction Temperature ( $T_J$ ) must not exceed the absolute maximum specification of  $+150^{\circ}C$ .

### 1.1 Test Circuit Configuration

This test circuit configuration is used to determine the AC and DC specifications.

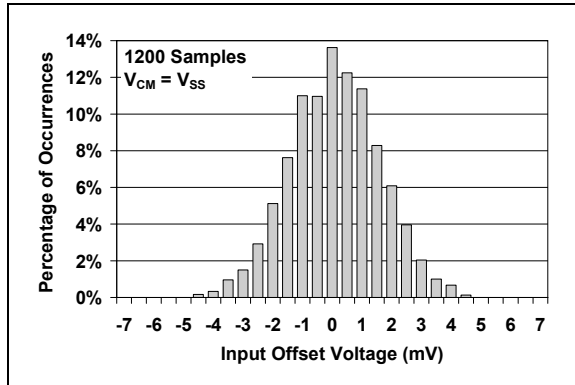


**FIGURE 1-3:** AC and DC Test circuit for the open-drain output comparators.

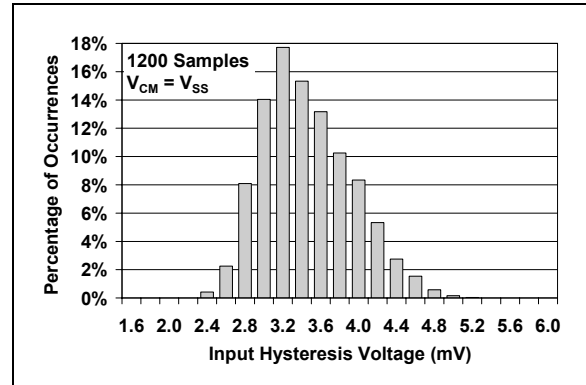
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

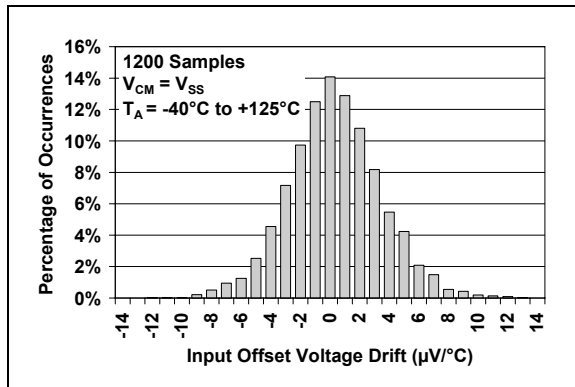
**Note:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = +25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



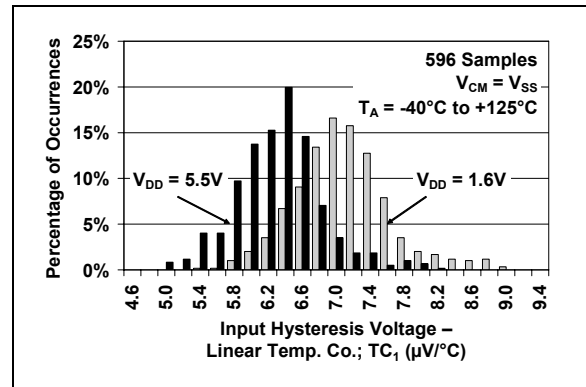
**FIGURE 2-1:** Input Offset Voltage at  $V_{CM} = V_{SS}$ .



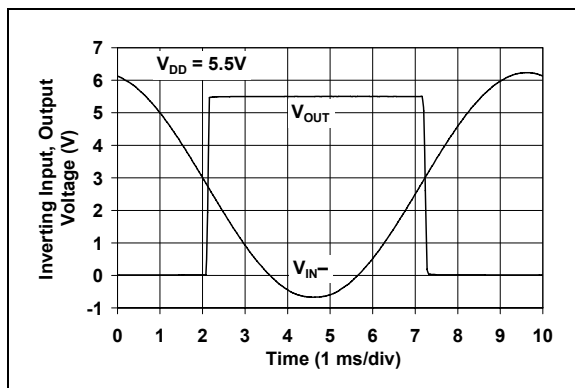
**FIGURE 2-4:** Input Hysteresis Voltage at  $V_{CM} = V_{SS}$ .



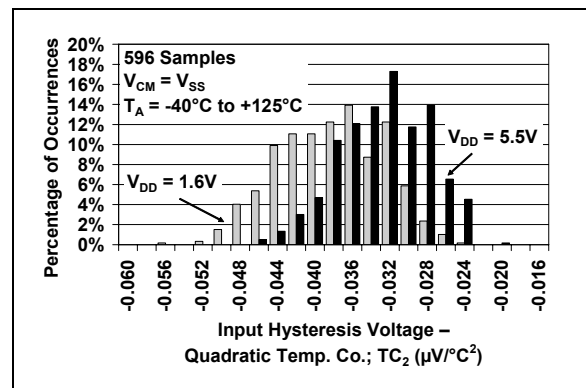
**FIGURE 2-2:** Input Offset Voltage Drift at  $V_{CM} = V_{SS}$ .



**FIGURE 2-5:** Input Hysteresis Voltage Linear Temp. Co. ( $TC_1$ ) at  $V_{CM} = V_{SS}$ .



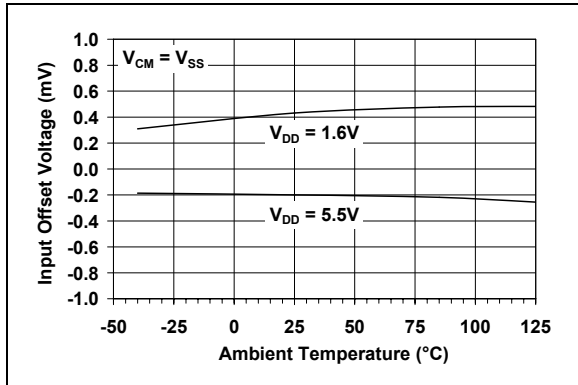
**FIGURE 2-3:** The MCP6546/7/8/9 comparators show no phase reversal.



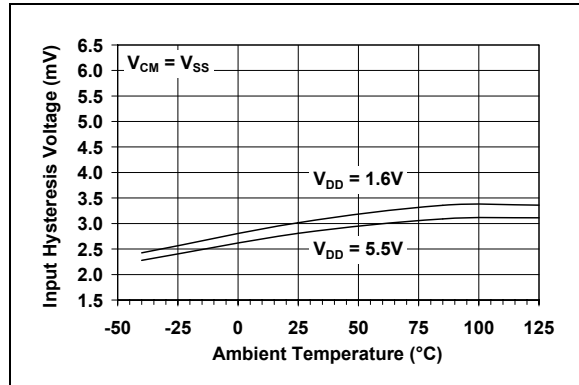
**FIGURE 2-6:** Input Hysteresis Voltage Quadratic Temp. Co. ( $TC_2$ ) at  $V_{CM} = V_{SS}$ .

# MCP6546/7/8/9

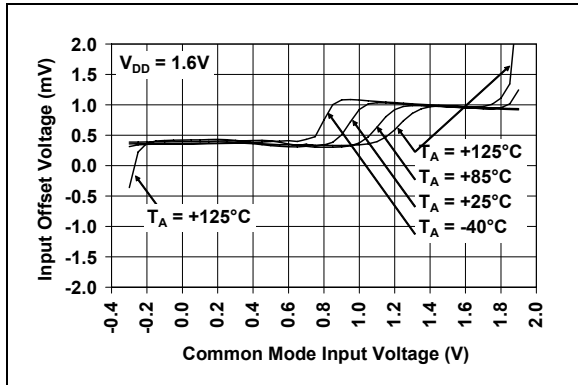
**Note:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = +25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



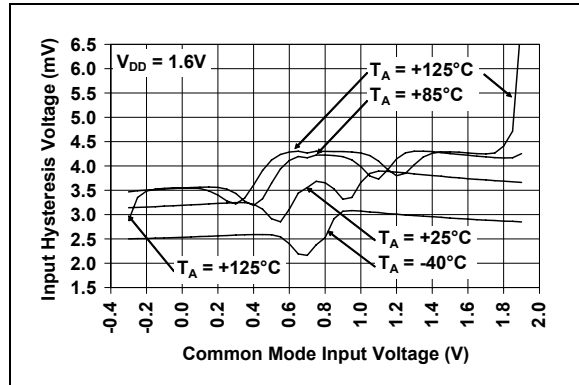
**FIGURE 2-7:** Input Offset Voltage vs. Ambient Temperature at  $V_{CM} = V_{SS}$ .



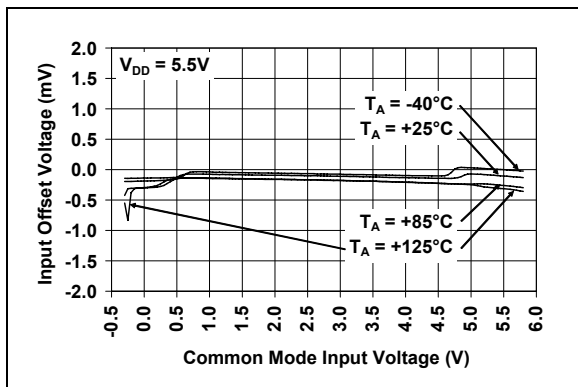
**FIGURE 2-10:** Input Hysteresis Voltage vs. Ambient Temperature at  $V_{CM} = V_{SS}$ .



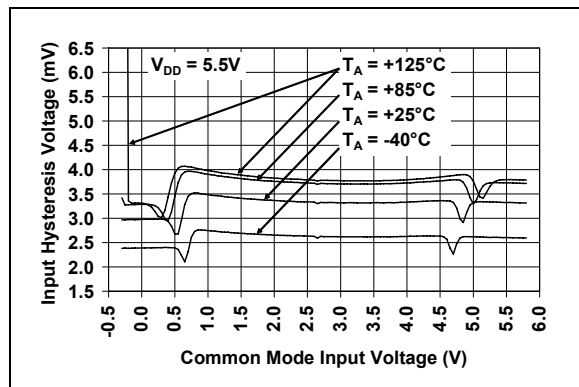
**FIGURE 2-8:** Input Offset Voltage vs. Common Mode Input Voltage at  $V_{DD} = 1.6V$ .



**FIGURE 2-11:** Input Hysteresis Voltage vs. Common Mode Input Voltage at  $V_{DD} = 1.6V$ .



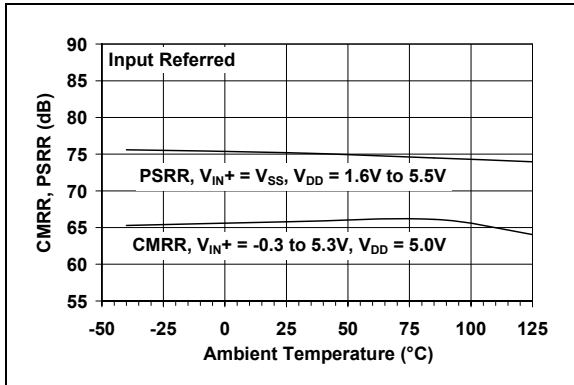
**FIGURE 2-9:** Input Offset Voltage vs. Common Mode Input Voltage at  $V_{DD} = 5.5V$ .



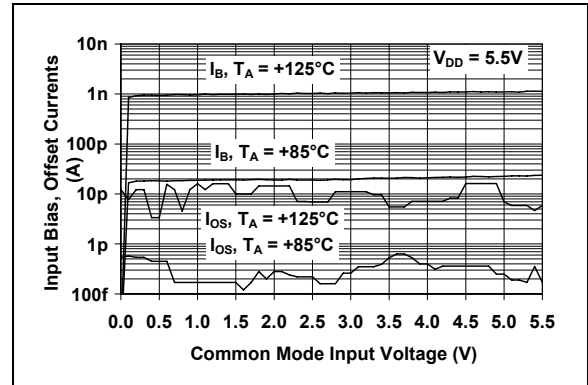
**FIGURE 2-12:** Input Hysteresis Voltage vs. Common Mode Input Voltage at  $V_{DD} = 5.5V$ .

# MCP6546/7/8/9

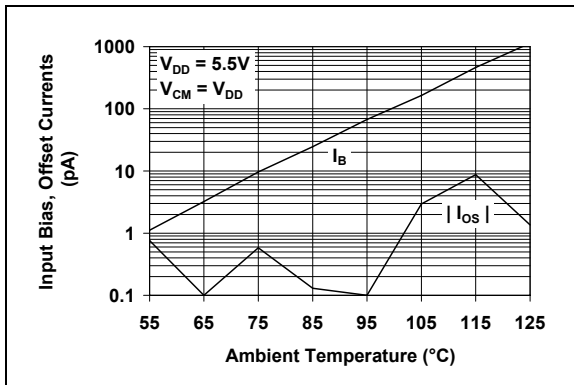
**Note:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = +25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



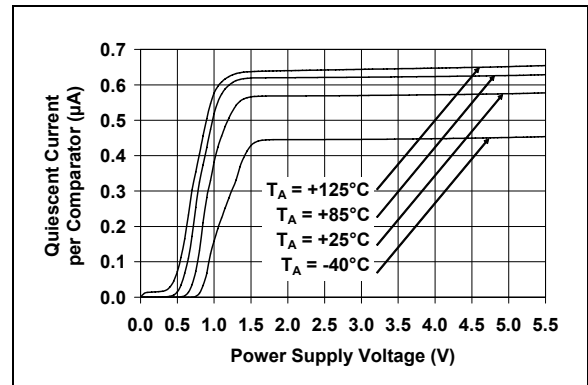
**FIGURE 2-13:** CMRR, PSRR vs. Ambient Temperature.



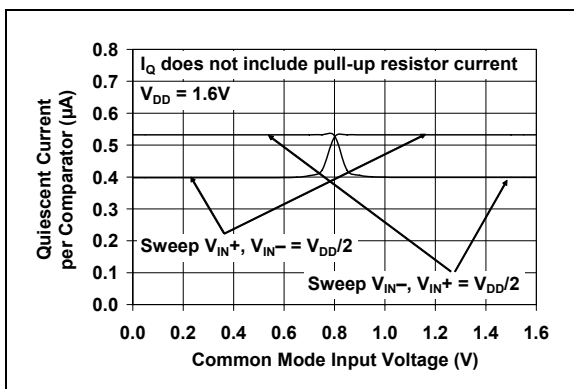
**FIGURE 2-16:** Input Bias Current, Input Offset Current vs. Common Mode Input Voltage.



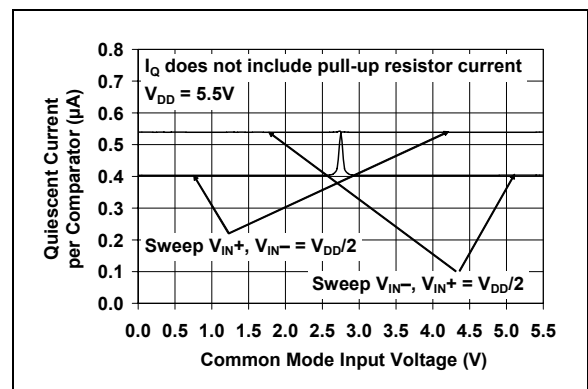
**FIGURE 2-14:** Input Bias Current, Input Offset Current vs. Ambient Temperature.



**FIGURE 2-17:** Quiescent Current vs. Power Supply Voltage.



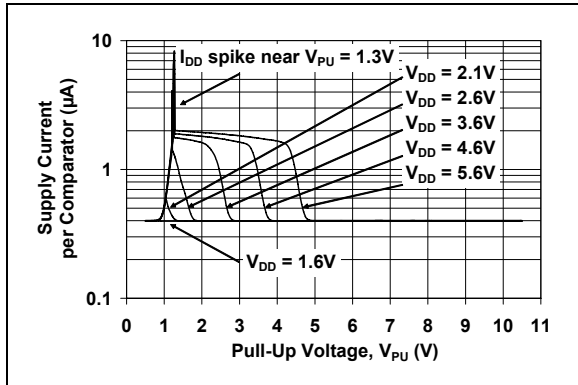
**FIGURE 2-15:** Quiescent Current vs. Common Mode Input Voltage at  $V_{DD} = 1.6V$ .



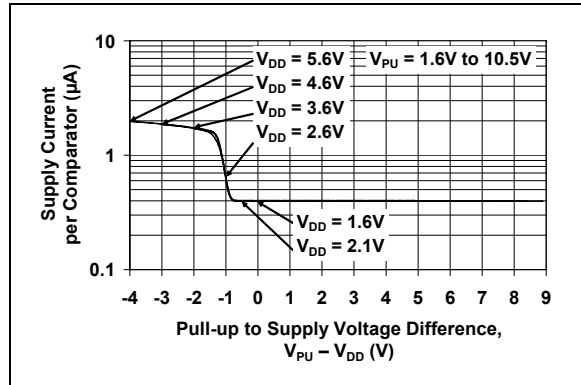
**FIGURE 2-18:** Quiescent Current vs. Common Mode Input Voltage at  $V_{DD} = 5.5V$ .

# MCP6546/7/8/9

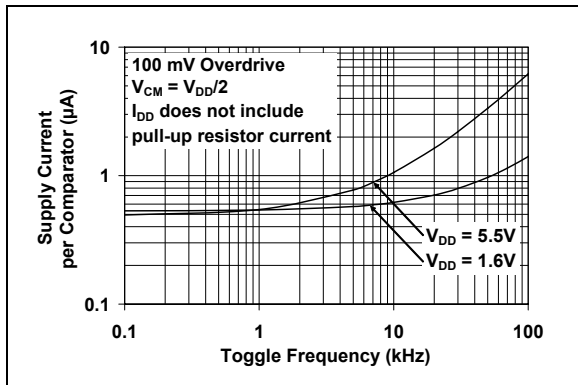
**Note:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = +25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



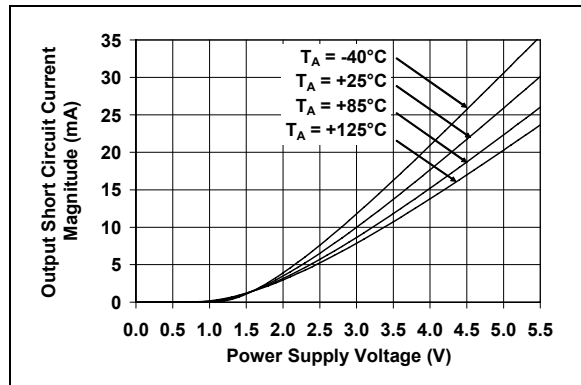
**FIGURE 2-19:** Supply Current vs. Pull-Up Voltage.



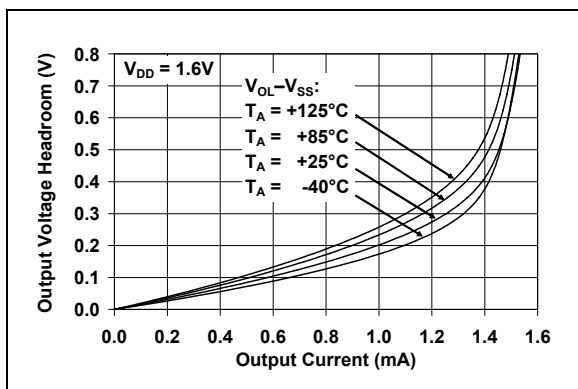
**FIGURE 2-22:** Supply Current vs. Pull-Up to Supply Voltage Difference.



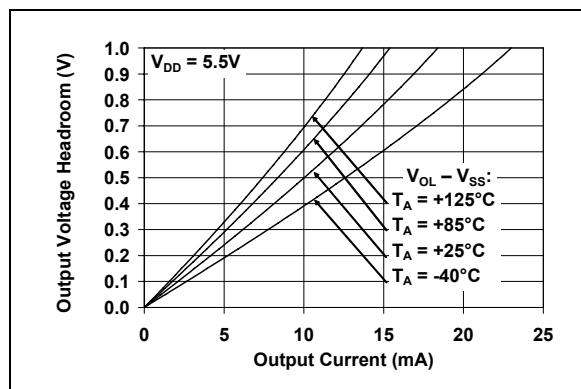
**FIGURE 2-20:** Supply Current vs. Toggle Frequency.



**FIGURE 2-23:** Output Short Circuit Current Magnitude vs. Power Supply Voltage.



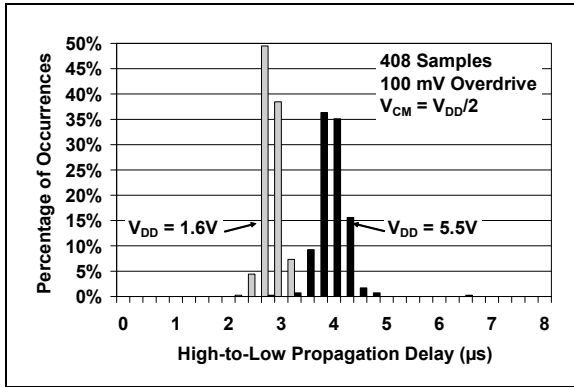
**FIGURE 2-21:** Output Voltage Headroom vs. Output Current at  $V_{DD} = 1.6V$ .



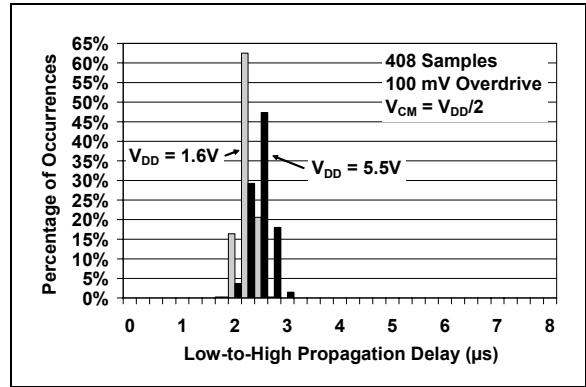
**FIGURE 2-24:** Output Voltage Headroom vs. Output Current at  $V_{DD} = 5.5V$ .



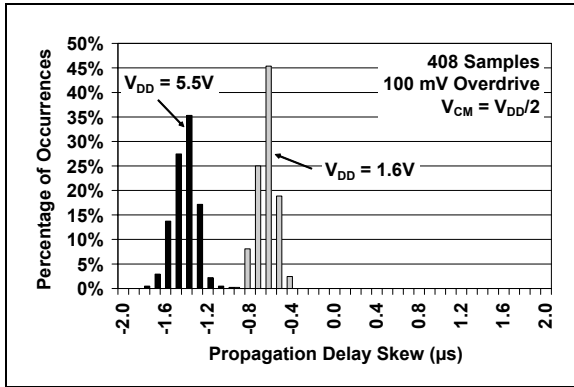
**Note:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = +25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\ k\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\ pF$ .



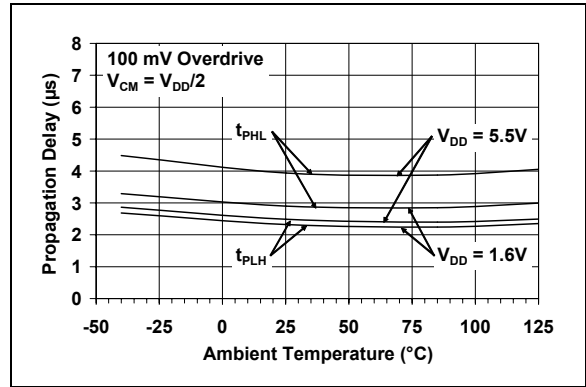
**FIGURE 2-25:** High-to-Low Propagation Delay.



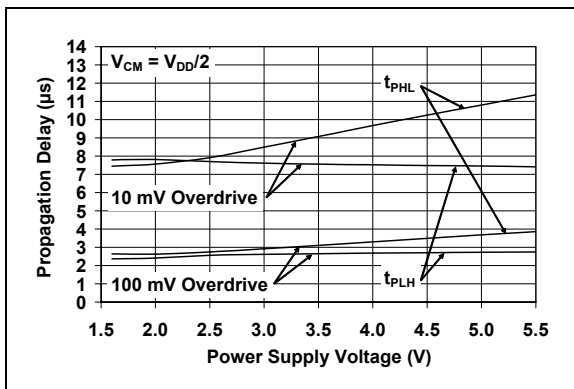
**FIGURE 2-28:** Low-to-High Propagation Delay.



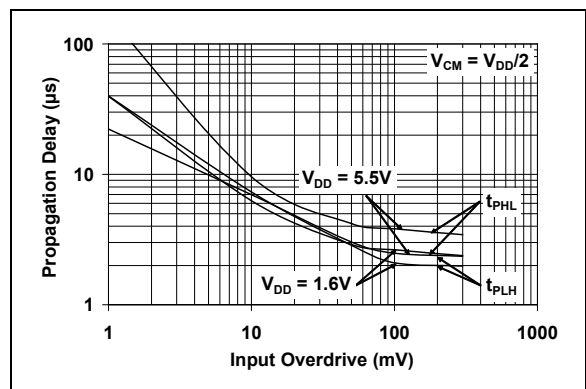
**FIGURE 2-26:** Propagation Delay Skew.



**FIGURE 2-29:** Propagation Delay vs. Ambient Temperature.



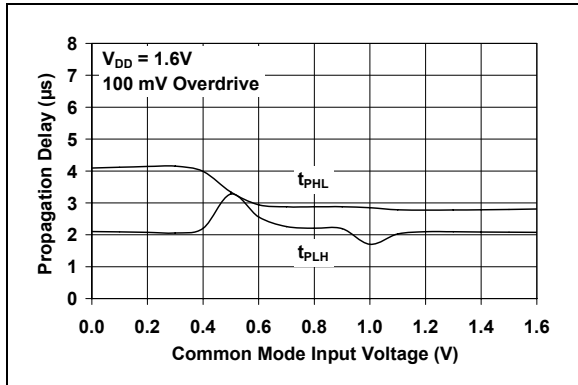
**FIGURE 2-27:** Propagation Delay vs. Power Supply Voltage.



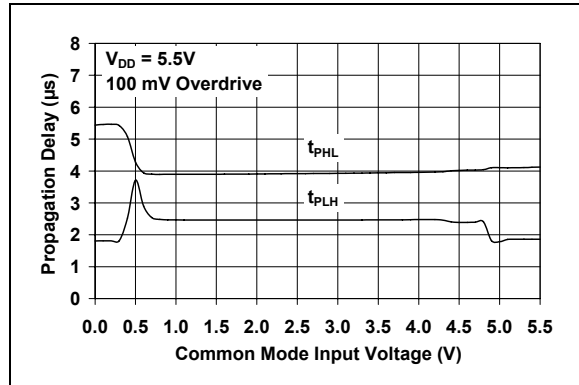
**FIGURE 2-30:** Propagation Delay vs. Input Overdrive.

# MCP6546/7/8/9

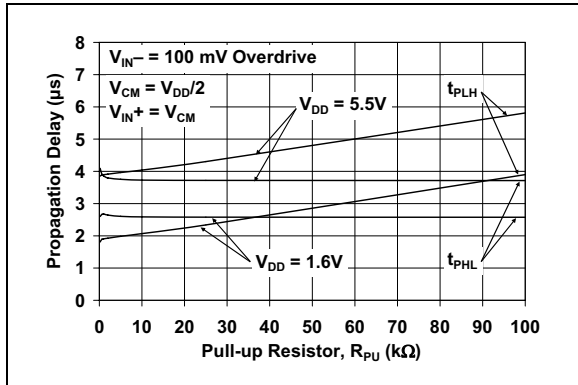
**Note:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = +25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



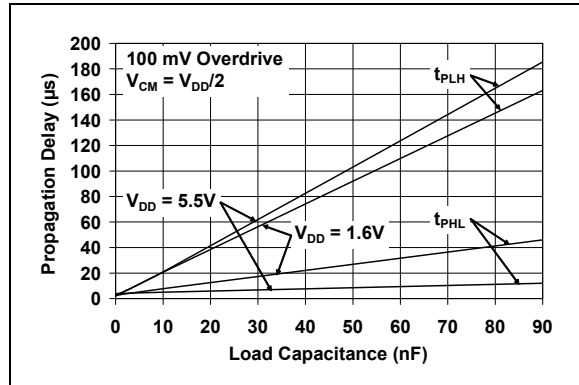
**FIGURE 2-31:** Propagation Delay vs. Common Mode Input Voltage at  $V_{DD} = 1.6V$ .



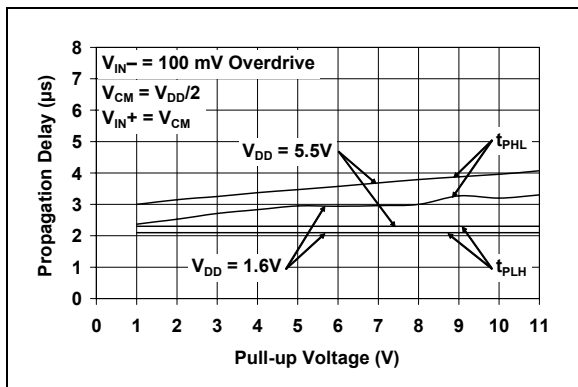
**FIGURE 2-34:** Propagation Delay vs. Common Mode Input Voltage at  $V_{DD} = 5.5V$ .



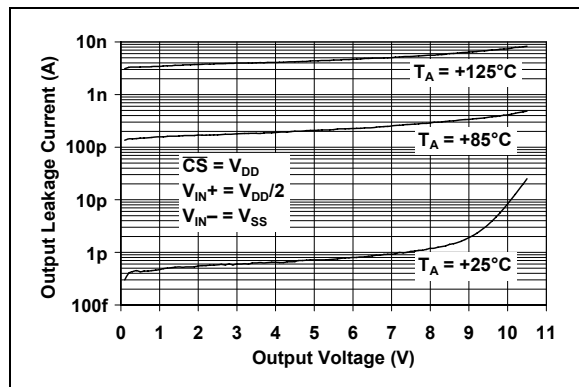
**FIGURE 2-32:** Propagation Delay vs. Pull-up Resistor.



**FIGURE 2-35:** Propagation Delay vs. Load Capacitance.

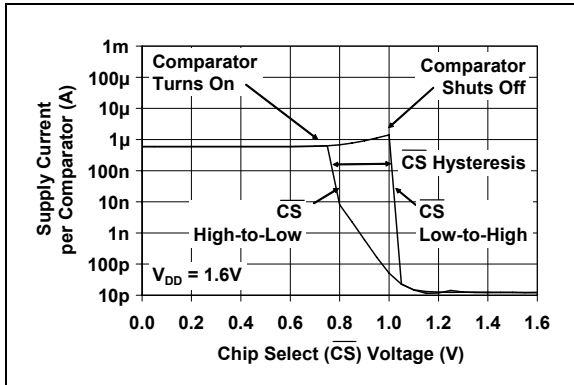


**FIGURE 2-33:** Propagation Delay vs. Pull-up Voltage.

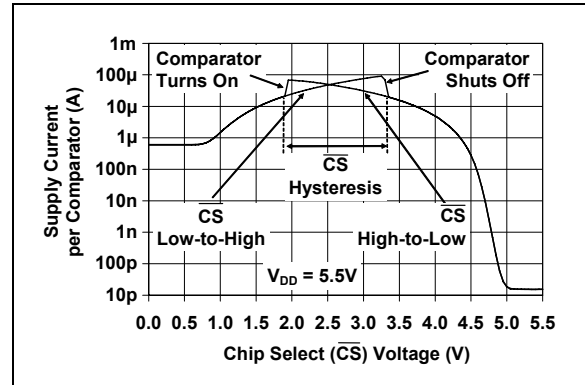


**FIGURE 2-36:** Output Leakage Current ( $C_S = V_{DD}$ ) vs. Output Voltage (MCP6548 only).

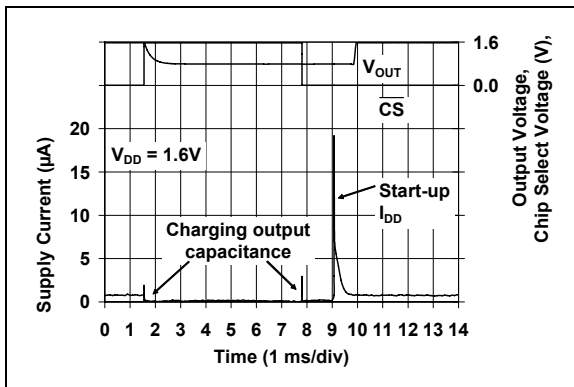
**Note:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = +25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



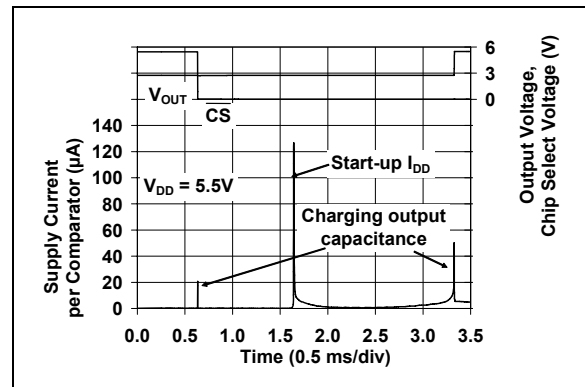
**FIGURE 2-37:** Supply Current (shoot through current) vs. Chip Select (CS) Voltage at  $V_{DD} = 1.6V$  (MCP6548 only).



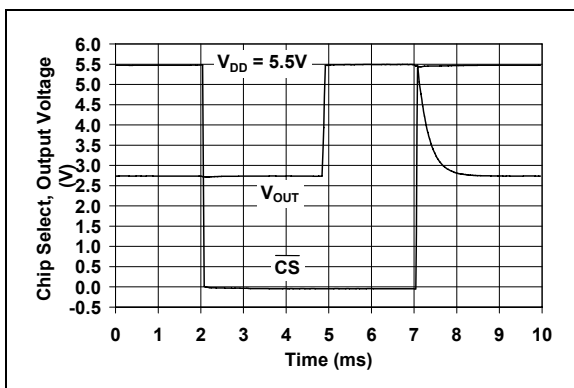
**FIGURE 2-40:** Supply Current (shoot through current) vs. Chip Select (CS) Voltage at  $V_{DD} = 5.5V$  (MCP6548 only).



**FIGURE 2-38:** Supply Current (charging current) vs. Chip Select (CS) pulse at  $V_{DD} = 1.6V$  (MCP6548 only).



**FIGURE 2-41:** Supply Current (charging current) vs. Chip Select (CS) pulse at  $V_{DD} = 5.5V$  (MCP6548 only).



**FIGURE 2-39:** Chip Select (CS) Step Response (MCP6548 only).

# MCP6546/7/8/9

## 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

MCP6546 (PDIP, SOIC, MSOP)	MCP6546 (SOT-23-5, SC-70-5)	MCP6546R	MCP6547	MCP6548	MCP6549	Symbol	Description
6	1	1	1	6	1	OUT, OUTA	Digital Output (comparator A)
2	4	4	2	2	2	$V_{IN-}$ , $V_{INA-}$	Inverting Input (comparator A)
3	3	3	3	3	3	$V_{IN+}$ , $V_{INA+}$	Non-inverting Input (comparator A)
7	5	2	8	7	4	$V_{DD}$	Positive Power Supply
—	—	—	5	—	5	$V_{INB+}$	Non-inverting Input (comparator B)
—	—	—	6	—	6	$V_{INB-}$	Inverting Input (comparator B)
—	—	—	7	—	7	OUTB	Digital Output (comparator B)
—	—	—	—	—	8	OUTC	Digital Output (comparator C)
—	—	—	—	—	9	$V_{INC-}$	Inverting Input (comparator C)
—	—	—	—	—	10	$V_{INC+}$	Non-inverting Input (comparator C)
4	2	5	4	4	11	$V_{SS}$	Negative Power Supply
—	—	—	—	—	12	$V_{IND+}$	Non-inverting Input (comparator D)
—	—	—	—	—	13	$V_{IND-}$	Inverting Input (comparator D)
—	—	—	—	—	14	OUTD	Digital Output (comparator D)
—	—	—	—	8	—	$\overline{CS}$	Chip Select
1, 5, 8	—	—	—	1, 5	—	NC	No Internal Connection

### 3.1 Analog Inputs

The comparator non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

### 3.2 $\overline{CS}$ Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low power mode of operation.

### 3.3 Digital Outputs

The comparator outputs are CMOS, open-drain digital outputs. They are designed to make level shifting and wired-OR easy to implement.

### 3.4 Power Supply ( $V_{SS}$ and $V_{DD}$ )

The positive power supply pin ( $V_{DD}$ ) is 1.6V to 5.5V higher than the negative power supply pin ( $V_{SS}$ ). For normal operation, the other pins are at voltages between  $V_{SS}$  and  $V_{DD}$ , except the output pins which can be as high as 10V above  $V_{SS}$ .

Typically, these parts are used in a single (positive) supply configuration. In this case,  $V_{SS}$  is connected to ground and  $V_{DD}$  is connected to the supply.  $V_{DD}$  will need a local bypass capacitor (typically 0.01  $\mu$ F to 0.1  $\mu$ F) within 2 mm of the  $V_{DD}$  pin. These can share a bulk capacitor with nearby analog parts (within 100 mm), but it is not required.

## 4.0 APPLICATIONS INFORMATION

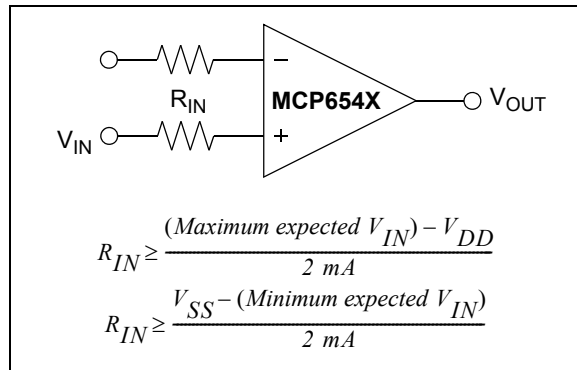
The MCP6546/7/8/9 family of push-pull output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of applications requiring very low power consumption.

### 4.1 Comparator Inputs

The MCP6546/7/8/9 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

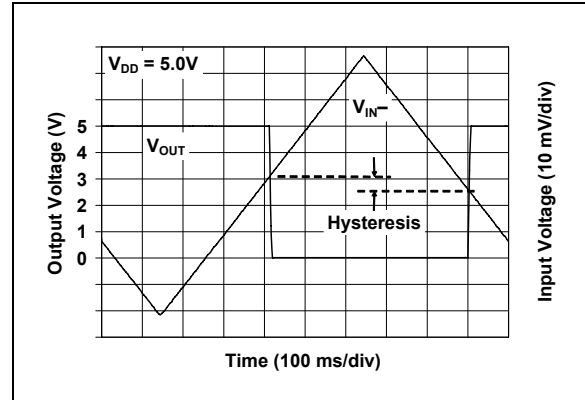
The input stage of this family of devices uses two differential input stages in parallel: one operates at low input voltages and the other at high input voltages. With this topology, the input voltage is 0.3V above  $V_{DD}$  and 0.3V below  $V_{SS}$ . The input offset voltage is measured at both  $V_{SS} - 0.3V$  and  $V_{DD} + 0.3V$  to ensure proper operation.

The maximum operating input voltages that can be applied are  $V_{SS} - 0.3V$  and  $V_{DD} + 0.3V$ . Voltages on the inputs that exceed this absolute maximum rating can cause excessive current to flow and permanently damage the device. In applications where the input pin exceeds the specified range, external resistors can be used to limit the current below  $\pm 2$  mA, as shown in Figure 4-1.



**FIGURE 4-1:** Input Current-Limiting Resistor ( $R_{IN}$ ).

The MCP6546/7/8/9 family has internally-set hysteresis that is small enough to maintain input offset accuracy ( $<7$  mV), and large enough to eliminate output chattering caused by the comparator's own input noise voltage ( $200 \mu V_{P-P}$ ). Figure 4-2 illustrates this capability.



**FIGURE 4-2:** The MCP6546/7/8/9 comparators' internal hysteresis eliminates output chatter caused by input noise voltage.

### 4.2 Open-Drain Output

The open-drain output is designed to make level-shifting and wired-OR logic easy to implement. The output can go as high as 10V for 9V battery-powered applications. The output stage minimizes switching current (shoot-through current from supply-to-supply) when the output changes state. See Figures 2-15, 2-18 and 2-37 through 2-41, for more information.

### 4.3 MCP6548 Chip Select ( $\overline{CS}$ )

The MCP6548 is a single comparator with a Chip Select ( $\overline{CS}$ ) pin. When  $\overline{CS}$  is pulled high, the total current consumption drops to 20 pA (typ.). 1 pA (typ.) flows through the  $\overline{CS}$  pin, 1 pA (typ.) flows through the output pin and 18 pA (typ.) flows through the  $V_{DD}$  pin, as shown in Figure 1-1. When this happens, the comparator output is put into a high-impedance state. By pulling  $\overline{CS}$  low, the comparator is enabled. If the  $\overline{CS}$  pin is left floating, the comparator will not operate properly. Figure 1-1 shows the output voltage and supply current response to a  $\overline{CS}$  pulse.

The internal  $\overline{CS}$  circuitry is designed to minimize glitches when cycling the  $\overline{CS}$  pin. This helps conserve power, which is especially important in battery-powered applications.

# MCP6546/7/8/9

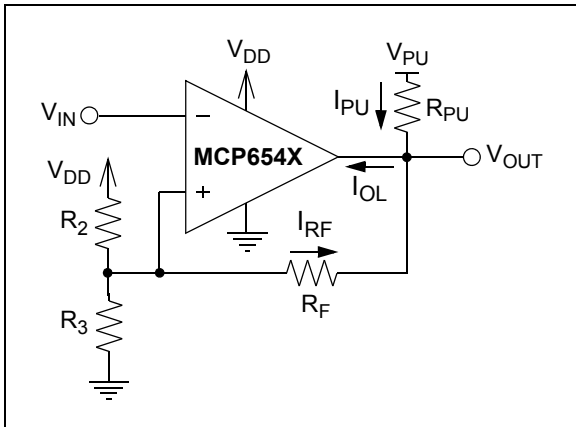
## 4.4 Externally Set Hysteresis

Greater flexibility in selecting hysteresis, or input trip points, is achieved by using external resistors.

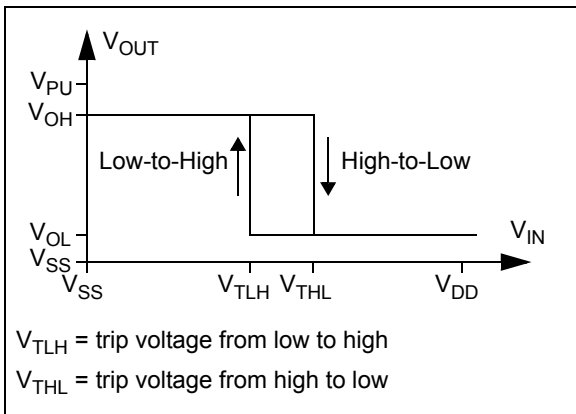
Input offset voltage ( $V_{OS}$ ) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage ( $V_{HYST}$ ) is the difference between the same trip points. Hysteresis reduces output chattering when one input is slowly moving past the other, thus reducing dynamic supply current. It also helps in systems where it is best not to cycle between states too frequently (e.g., air conditioner thermostatic control).

### 4.4.1 INVERTING CIRCUIT

Figure 4-3 shows an inverting circuit for a single-supply application using three resistors, besides the pull-up resistor. The resulting hysteresis diagram is shown in Figure 4-4.

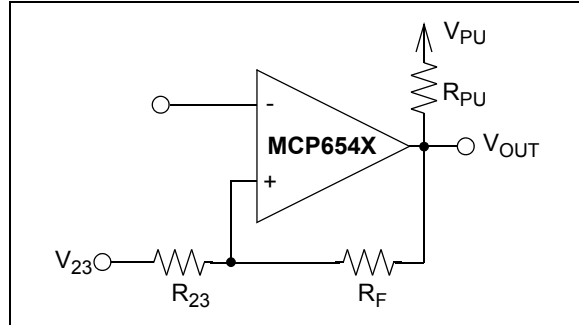


**FIGURE 4-3:** Inverting circuit with hysteresis.



**FIGURE 4-4:** Hysteresis diagram for the inverting circuit.

In order to determine the trip voltages ( $V_{TTH}$  and  $V_{TLH}$ ) for the circuit shown in Figure 4-3,  $R_2$  and  $R_3$  can be simplified to the Thevenin equivalent circuit with respect to  $V_{DD}$ , as shown in Figure 4-5.



**FIGURE 4-5:** Thevenin Equivalent Circuit.

### EQUATION 4-1:

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{R_3}{R_2 + R_3} \times V_{DD}$$

Using this simplified circuit, the trip voltage can be calculated using the following equation:

### EQUATION 4-2:

$$V_{TTH} = V_{PU} \left( \frac{R_{23}}{R_{23} + R_F + R_{PU}} \right) + V_{23} \left( \frac{R_F + R_{PU}}{R_{23} + R_F + R_{PU}} \right)$$

$$V_{TLH} = V_{OL} \left( \frac{R_{23}}{R_{23} + R_F} \right) + V_{23} \left( \frac{R_F}{R_{23} + R_F} \right)$$

$V_{TLH}$  = trip voltage from low to high

$V_{TTH}$  = trip voltage from high to low

Figure 2-21 and Figure 2-24 can be used to determine typical values for  $V_{OL}$ . This voltage is dependent on the output current  $I_{OL}$  as shown in Figure 4-3. This current can be determined using the equation below:

### EQUATION 4-3:

$$I_{OL} = I_{PU} + I_{RF}$$

$$I_{OL} = \left( \frac{V_{PU} - V_{OL}}{R_{PU}} \right) + \left( \frac{V_{23} - V_{OL}}{R_{23} + R_F} \right)$$

$V_{OH}$  can be calculated using the equation below:

### EQUATION 4-4:

$$V_{OH} = (V_{PU} - V_{23}) \times \left( \frac{R_{23} + R_F}{R_{23} + R_F + R_{PU}} \right)$$

As explained in **Section 4.1 “Comparator Inputs”**, it is important to keep the non-inverting input below  $V_{DD}+0.3V$  when  $V_{PU} > V_{DD}$ .

## 4.5 Supply Bypass

With this family of comparators, the power supply pin ( $V_{DD}$  for single supply) should have a local bypass capacitor (i.e., 0.01  $\mu F$  to 0.1  $\mu F$ ) within 2 mm for good edge rate performance.

## 4.6 Capacitive Loads

Reasonable capacitive loads (e.g., logic gates) have little impact on propagation delay (see Figure 2-27). The supply current increases with increasing toggle frequency (Figure 2-30), especially with higher capacitive loads.

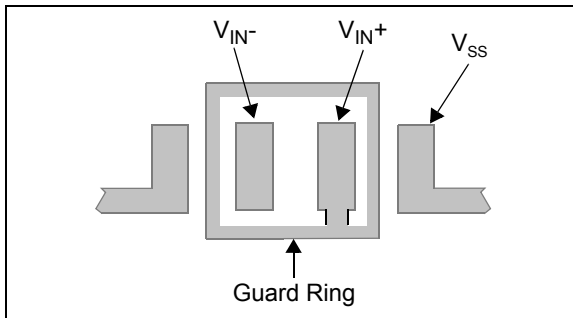
## 4.7 Battery Life

In order to maximize battery life in portable applications, use large resistors and small capacitive loads. Avoid toggling the output more than necessary. Do not use Chip Select (CS) too frequently in order to conserve power. Capacitive loads will draw additional power at start-up.

## 4.8 PCB Surface Leakage

In applications where low input bias current is critical, PCB (Printed Circuit Board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low-humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6546/7/8/9 family’s bias current at 25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.



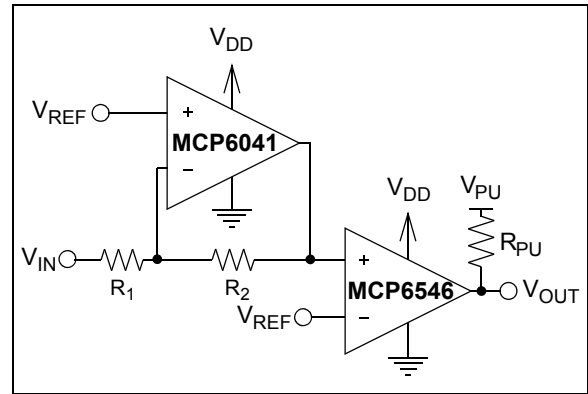
**FIGURE 4-6:** Example Guard Ring Layout for Inverting Circuit.

1. Inverting Configuration (Figures 4-3 and 4-6):
  - a. Connect the guard ring to the non-inverting input pin ( $V_{IN+}$ ). This biases the guard ring to the same reference voltage as the comparator (e.g.,  $V_{DD}/2$  or ground).
  - b. Connect the inverting pin ( $V_{IN-}$ ) to the input pad without touching the guard ring.

## 4.9 Typical Applications

### 4.9.1 PRECISE COMPARATOR

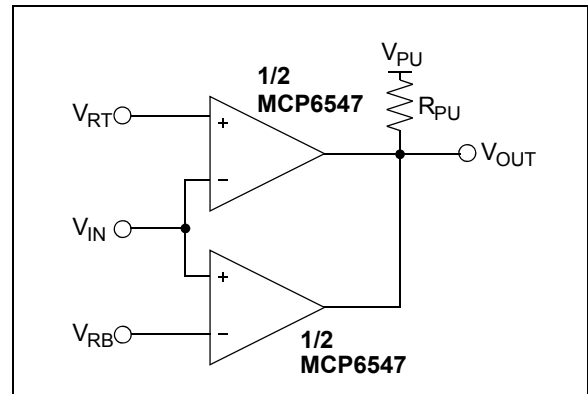
Some applications require higher DC precision. An easy way to solve this problem is to use an amplifier (such as the MCP6041) to gain-up the input signal before it reaches the comparator. Figure 4-7 shows an example of this approach.



**FIGURE 4-7:** Precise Inverting Comparator.

### 4.9.2 WINDOWED COMPARATOR

Figure 4-8 shows one approach to designing a windowed comparator. The wired-OR connection produces a high output (logic 1) when the input voltage is between  $V_{RB}$  and  $V_{RT}$  (where  $V_{RT} > V_{RB}$ ).



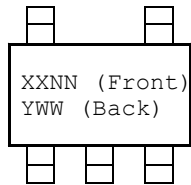
**FIGURE 4-8:** Windowed Comparator.

# MCP6546/7/8/9

## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

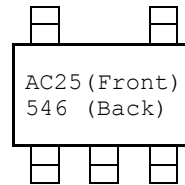
5-Lead SC-70 (MCP6546)



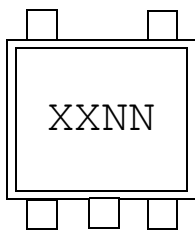
Device	I-Temp Code	E-Temp Code
MCP6546	ACNN	Note 2

**Note 1:** I-Temp parts prior to March 2005 are marked "ACN"  
**Note 2:** SC-70-5 E-Temp parts not available at this release of the data sheet.

Example: (I-temp)



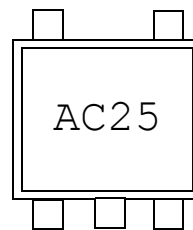
5-Lead SOT-23 (MCP6546 and MCP6546R)



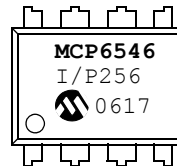
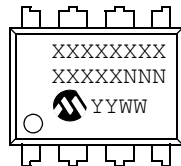
Device	I-Temp Code	E-Temp Code
MCP6546	ACNN	GWNN
MCP6546R	AHNN	GXNN

**Note:** Applies to 5-Lead SOT-23

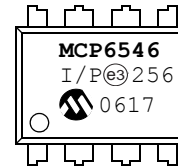
Example: (I-temp)



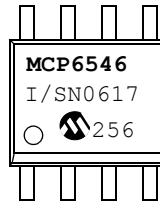
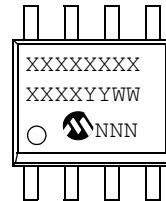
8-Lead PDIP (300 mil)



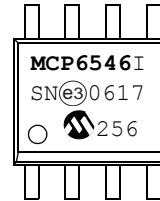
Example:



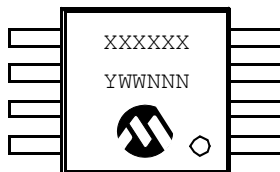
8-Lead SOIC (150 mil)



Example:



8-Lead MSOP



Example:



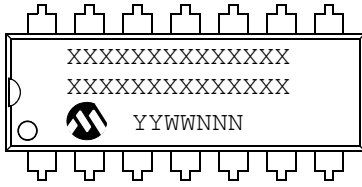
**Legend:** XX...X Customer-specific information  
 Y Year code (last digit of calendar year)  
 YY Year code (last 2 digits of calendar year)  
 WW Week code (week of January 1 is week '01')  
 NNN Alphanumeric traceability code  
 (e3) Pb-free JEDEC designator for Matte Tin (Sn)  
 \* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

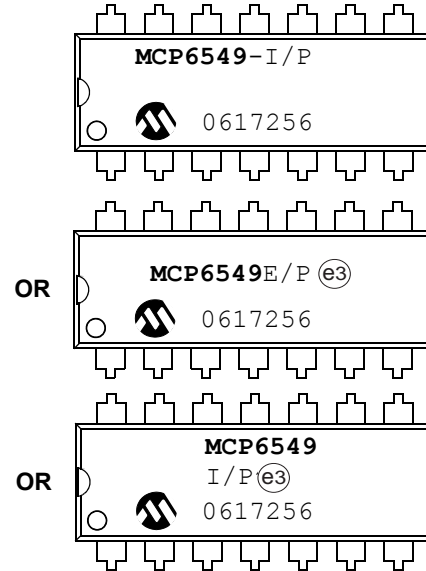


## Package Marking Information (Continued)

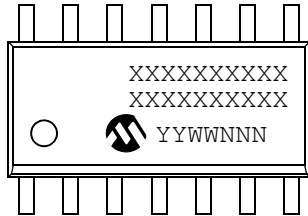
14-Lead PDIP (300 mil) (MCP6549)



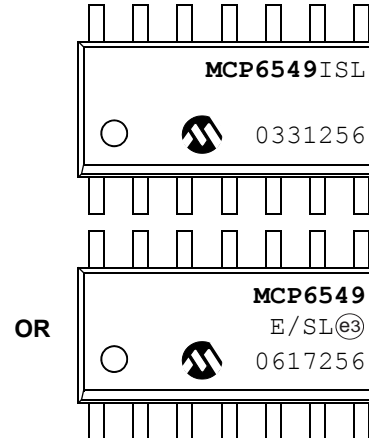
Example:



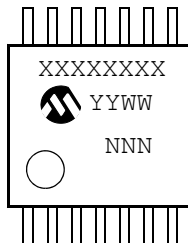
14-Lead SOIC (150 mil) (MCP6549)



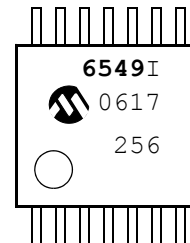
Example:



14-Lead TSSOP (MCP6549)

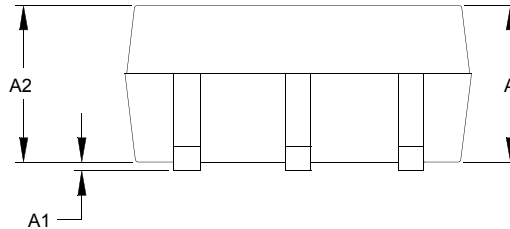
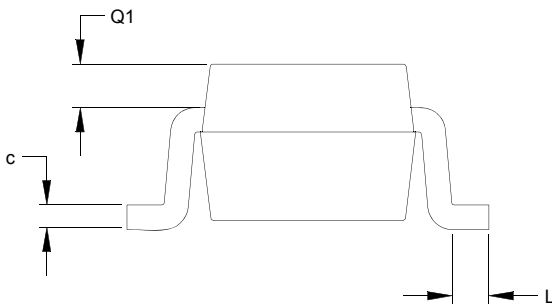
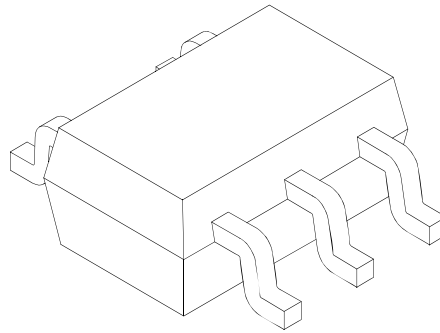
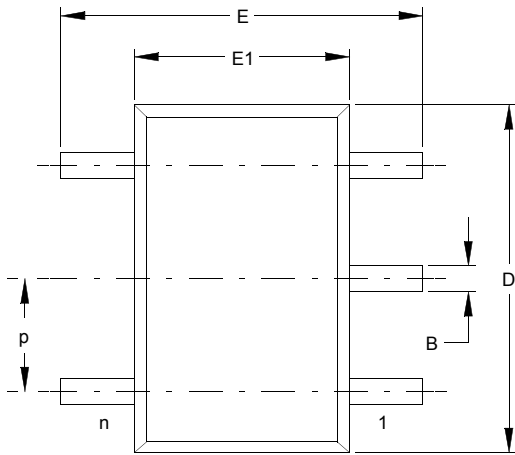


Example:



# MCP6546/7/8/9

## 5-Lead Plastic Package (LT) (SC-70)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	5			5		
Pitch	P	.026 (BSC)			0.65 (BSC)		
Overall Height	A	.031		.043	0.80		1.10
Molded Package Thickness	A2	.031		.039	0.80		1.00
Standoff	A1	.000		.004	0.00		0.10
Overall Width	E	.071		.094	1.80		2.40
Molded Package Width	E1	.045		.053	1.15		1.35
Overall Length	D	.071		.087	1.80		2.20
Foot Length	L	.004		.012	0.10		0.30
Top of Molded Pkg to Lead Shoulder	Q1	.004		.016	0.10		0.40
Lead Thickness	c	.004		.007	0.10		0.18
Lead Width	B	.006		.012	0.15		0.30

\* Controlling Parameter

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

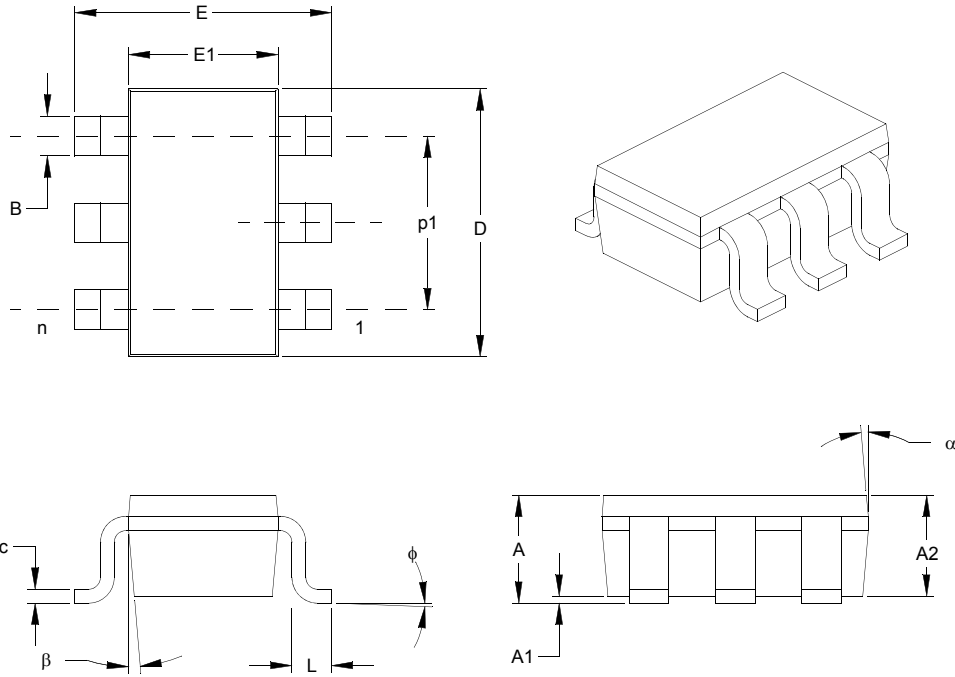
See ASME Y14.5M

JEITA (EIAJ) Standard: SC-70

Drawing No. C04-061

Revised 07-19-05

## 5-Lead Plastic Small Outline Transistor (OT) (SOT23)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	6			6		
Pitch	p	.038 BSC			0.95 BSC		
Outside lead pitch	p1	.075 BSC			1.90 BSC		
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

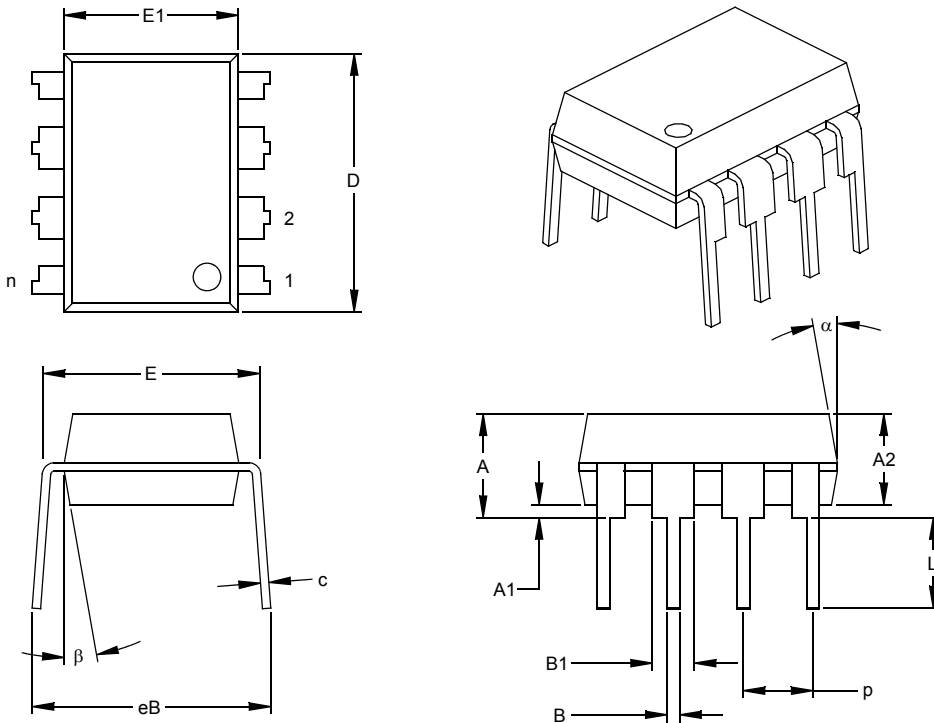
JEITA (formerly EIAJ) equivalent: SC-74A

Drawing No. C04-120

Revised 09-12-05

# MCP6546/7/8/9

## 8-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	8			8		
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

**Notes:**

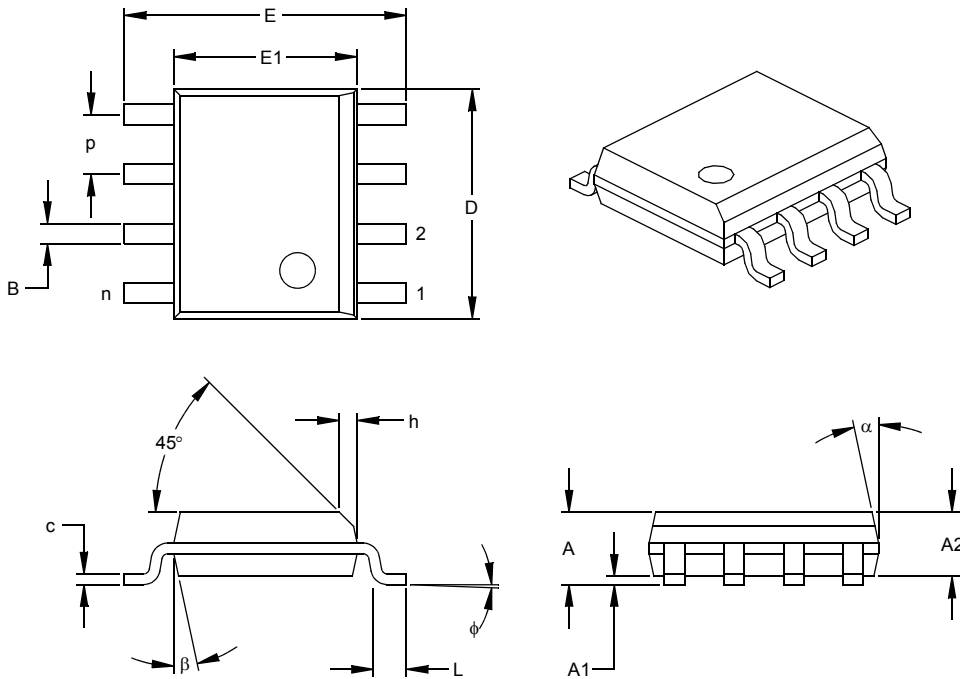
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

# MCP6546/7/8/9

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	8			8		
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

**Notes:**

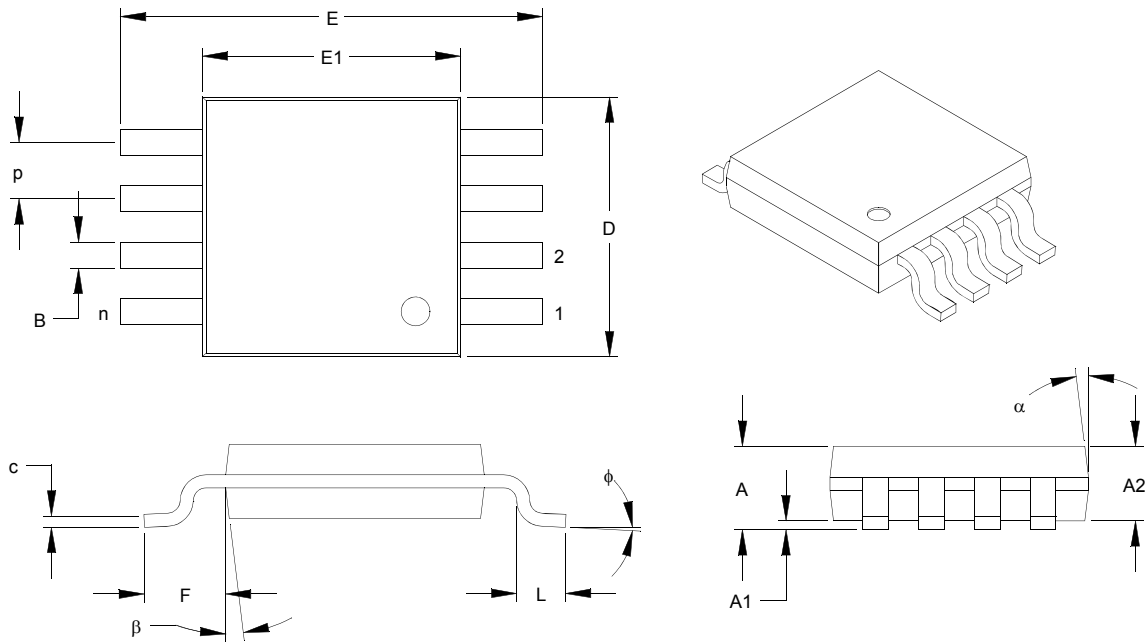
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

# MCP6546/7/8/9

## 8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p	.026 BSC			0.65 BSC		
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E	.193 BSC			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F	.037 REF			0.95 REF		
Foot Angle	$\phi$	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	$\alpha$	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	$\beta$	5°	-	15°	5°	-	15°

\* Controlling Parameter

### Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.

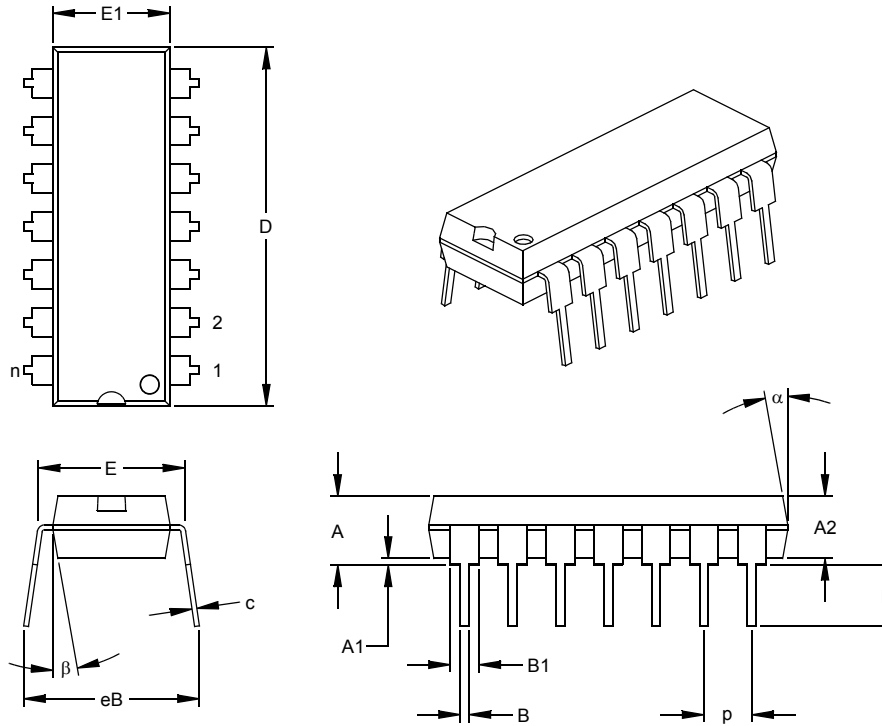
See ASME Y14.5M

JEDEC Equivalent: MO-187

Drawing No. C04-111

Revised 07-21-05

## 14-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	14			14		
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

**Notes:**

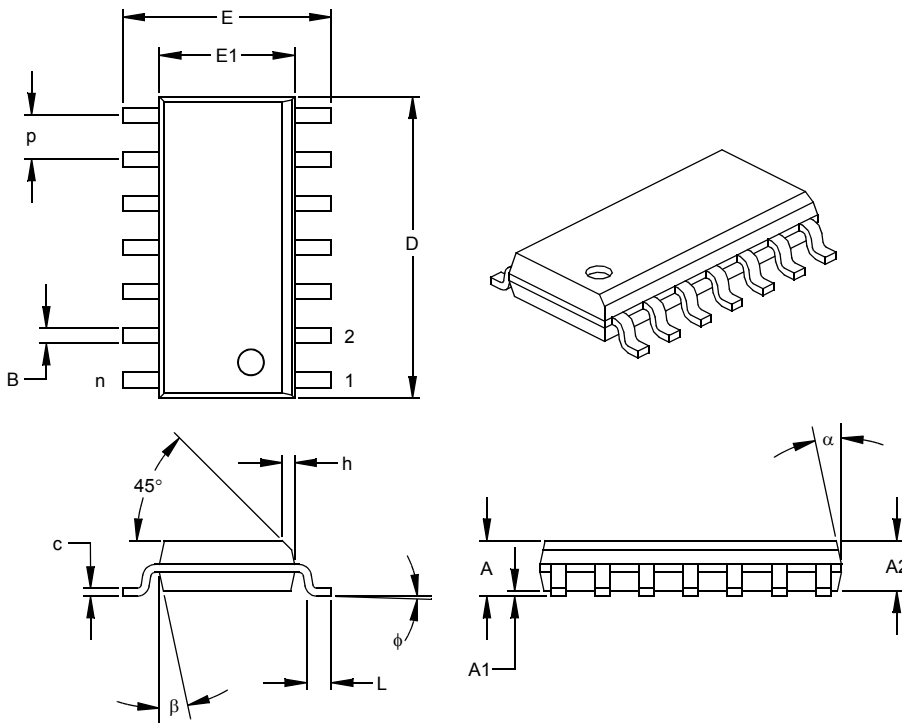
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

# MCP6546/7/8/9

## 14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	14			14		
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

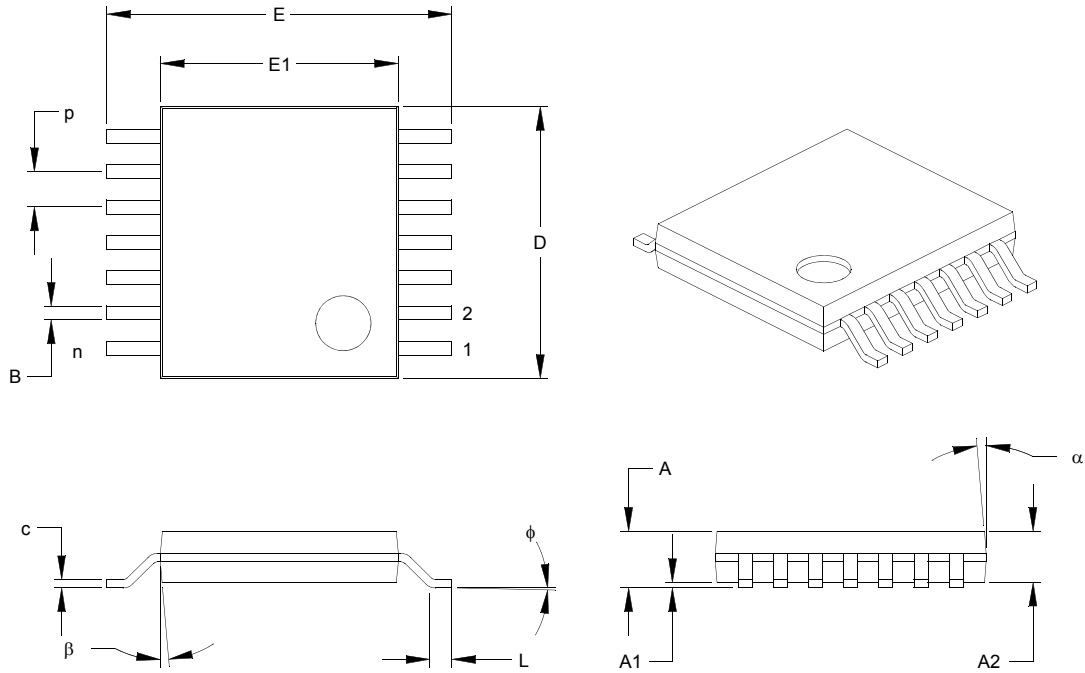
JEDEC Equivalent: MS-012

Drawing No. C04-065



# MCP6546/7/8/9

## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	14			14		
Pitch	p	.026 BSC			0.65 BSC		
Overall Height	A	.039	.041	.043	1.00	1.05	1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0°	4°	8°	0°	4°	8°
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	12° REF			12° REF		
Mold Draft Angle Bottom	β	12° REF			12° REF		

\* Controlling Parameter

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.

See ASME Y14.5M

JEDEC Equivalent: MO-153 AB-1

Drawing No. C04-087

Revised: 08-17-05

# MCP6546/7/8/9

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision D (May 2006)

The following is the list of modifications:

1. Added E-temp parts.
2. Changed minimum pull-up voltage specification ( $V_{PU}$ ) to 1.6V for parts starting Dec. 2004 (week code 52); previous parts are specified at a minimum of  $V_{DD}$ .
3. Changed VHYST temperature specifications to linear and quadratic temperature coefficients.
4. Changed specifications and plots to include E-Temp parts.
5. Added **Section 3.0 “Pin Descriptions”**.
6. Corrected package markings (**Section 5.1 “Package Marking Information”**).
7. Added **Appendix A: “Revision History”**.

### Revision C (May 2003)

### Revision B (December 2002)

### Revision A (February 2002)

- Original Release of this Document.

# MCP6546/7/8/9

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>=X</u>	<u>/XX</u>	
Device	Temperature Range	Package	
<p><b>Device:</b></p> <p>MCP6546: Single Comparator  MCP6546T: Single Comparator (Tape and Reel) (SC-70, SOT-23, SOIC, MSOP)  MCP6546RT: Single Comparator (Rotated - Tape and Reel) (SOT-23 only)  MCP6547: Dual Comparator  MCP6547T: Dual Comparator (Tape and Reel for SOIC and MSOP)  MCP6548: Single Comparator with <math>\overline{CS}</math>  MCP6548T: Single Comparator with <math>\overline{CS}</math> (Tape and Reel for SOIC and MSOP)  MCP6549: Quad Comparator  MCP6549T: Quad Comparator (Tape and Reel for SOIC and TSSOP)</p> <p><b>Temperature Range:</b> I = -40°C to +85°C  E* = -40°C to +125°C  * SC-70-5 E-Temp parts not available at this release of the data sheet.</p> <p><b>Package:</b> LT = Plastic Package (SC-70), 5-lead  OT = Plastic Small Outline Transistor (SOT-23), 5-lead  MS = Plastic MSOP, 8-lead  P = Plastic DIP (300 mil Body), 8-lead, 14-lead  SN = Plastic SOIC (150 mil Body), 8-lead  SL = Plastic SOIC (150 mil Body), 14-lead (MCP6549)  ST = Plastic TSSOP (4.4mm Body), 14-lead (MCP6549)</p>			
			<p><b>Examples:</b></p> <p>a) MCP6546T-I/LT: Tape and Reel, Industrial Temperature, 5LD SC-70.  b) MCP6546T-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT-23.  c) MCP6546-E/P: Extended Temperature, 8LD PDIP.  d) MCP6546RT-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT23.  e) MCP6546-E/SN: Extended Temperature, 8LD SOIC.  a) MCP6547-I/MS: Industrial Temperature, 8LD MSOP.  b) MCP6547T-I/MS: Tape and Reel, Industrial Temperature, 8LD MSOP.  c) MCP6547-I/P: Industrial Temperature, 8LD PDIP.  d) MCP6547-E/SN: Extended Temperature, 8LD SOIC.  a) MCP6548-I/SN: Industrial Temperature, 8LD SOIC.  b) MCP6548T-I/SN: Tape and Reel, Industrial Temperature, 8LD SOIC.  c) MCP6548-I/P: Industrial Temperature, 8LD PDIP.  d) MCP6548-E/SN: Extended Temperature, 8LD SOIC.  a) MCP6549T-I/SL: Tape and Reel, Industrial Temperature, 14LD SOIC.  b) MCP6549T-I/SL: Tape and Reel, Industrial Temperature, 14LD SOIC.  c) MCP6549-I/P: Industrial Temperature, 14LD PDIP.  d) MCP6549-E/SN: Extended Temperature, 8LD SOIC.</p>

# MCP6546/7/8/9

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NOTES:

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