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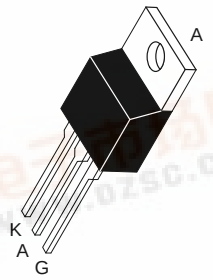
# Silicon Controlled Rectifiers
## Reverse Blocking Thyristors

**MCR16 SERIES***
*Motorola preferred devices

**SCRs**
**16 AMPERES RMS**
**400 thru 800**
**VOLTS**

Designed primarily for half–wave ac control applications, such as motor controls, heating controls, and power supplies; or wherever half–wave, silicon gate–controlled devices are needed.

- Blocking Voltage to 800 Volts
- On-State Current Rating of 16 Amperes RMS
- High Surge Current Capability — 160 Amperes
- Industry Standard TO–220AB Package for Ease of Design
- Glass Passivated Junctions for Reliability and Uniformity




**CASE 221A–06**
**(TO-220AB)**
**Style 3**

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Peak Repetitive Off-State Voltage (1)<br>Peak Repetitive Reverse Voltage<br>($T_J$ = –40 to 125°C) | MCR16D<br>MCR16M<br>MCR16N | $V_{DRM}$<br>$V_{RRM}$ | <br>400<br>600<br>800 | Volts |
| On-State RMS Current<br>(All Conduction Angles) | | $I_{T(RMS)}$ | 16 | A |
| Peak Non-repetitive Surge Current<br>(One Half Cycle, 60 Hz, $T_J$ = 125°C) | | $I_{TSM}$ | 160 | A |
| Circuit Fusing Consideration (t = 8.3 ms) | | $I^2t$ | 106 | $A^2$sec |
| Peak Gate Power (Pulse Width ≤ 1.0 µs, $T_C$ = 80°C) | | $P_{GM}$ | 5.0 | Watts |
| Average Gate Power (t = 8.3 ms, $T_C$ = 80°C) | | $P_{G(AV)}$ | 0.5 | Watts |
| Peak Gate Current (Pulse Width ≤ 1.0 µs, $T_C$ = 80°C) | | $I_{GM}$ | 2.0 | A |
| Operating Junction Temperature Range | | $T_J$ | –40 to +125 | °C |
| Storage Temperature Range | | $T_{stg}$ | –40 to +150 | °C |

**THERMAL CHARACTERISTICS**

| | | | |
|---|---|---|---|
| Thermal Resistance — Junction to Case<br>— Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.5<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds | $T_L$ | 260 | °C |

(1) $V_{DRM}$ and $V_{RRM}$ for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.



Preferred devices are Motorola recommended choices for future use and best overall value.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Peak Forward Blocking Current<br>Peak Reverse Blocking Current<br>($V_{AK}$ = Rated $V_{DRM}$ or $V_{RRM}$, Gate Open) | $T_J$ = 25°C<br>$T_J$ = 125°C | $I_{DRM}$<br>$I_{RRM}$ | —<br>— | —<br>— | 0.01<br>2.0 | mA |
| **ON CHARACTERISTICS** | | | | | | |
| Peak On-State Voltage* ($I_{TM}$ = 32 A) | | $V_{TM}$ | — | — | 1.7 | Volts |
| Gate Trigger Current (Continuous dc) ($V_D$ = 12 V, $R_L$ = 100 Ω) | | $I_{GT}$ | 2.0 | 8.0 | 20 | mA |
| Gate Trigger Voltage (Continuous dc) ($V_D$ = 12 V, $R_L$ = 100 Ω) | | $V_{GT}$ | 0.5 | 0.65 | 1.0 | Volts |
| Hold Current (Anode Voltage =12 V) | | $I_H$ | 4.0 | 25 | 40 | mA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Critical Rate of Rise of Off–State Voltage<br>($V_D$ = Rated $V_{DRM}$, Exponential Waveform, Gate Open, $T_J$ = 25°C) | | dv/dt | 50 | 200 | — | V/μs |

*Indicates Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

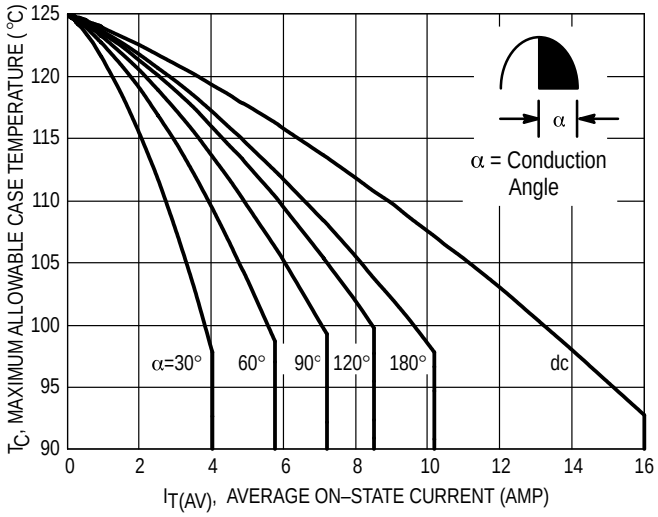



**Figure 1. Average Current Derating**

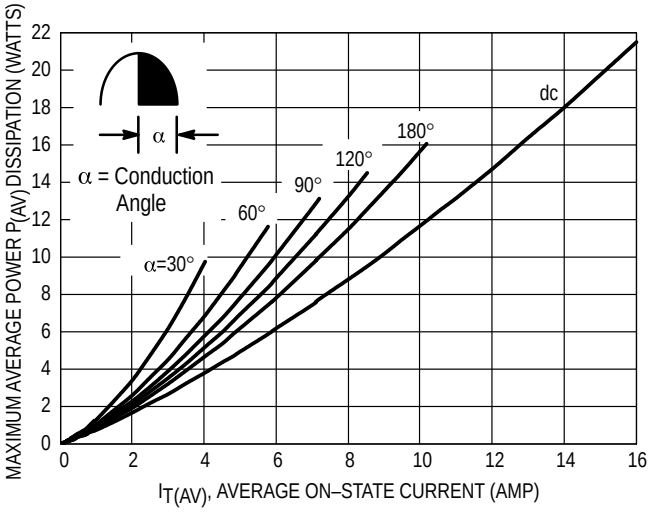



**Figure 2. Maximum On–State Power Dissipation**

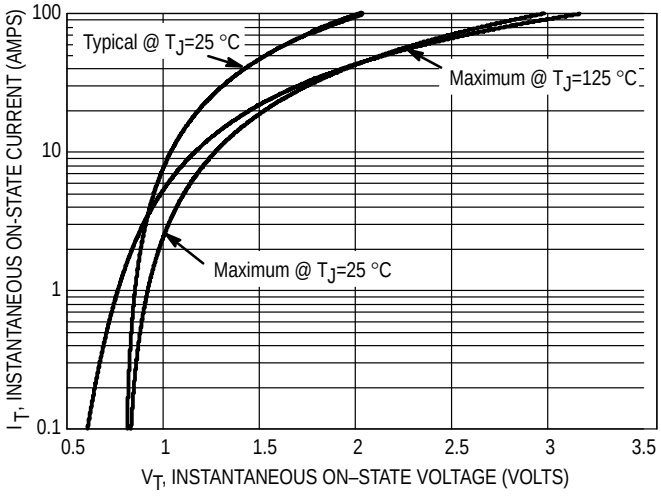



**Figure 3. On–State Characteristics**

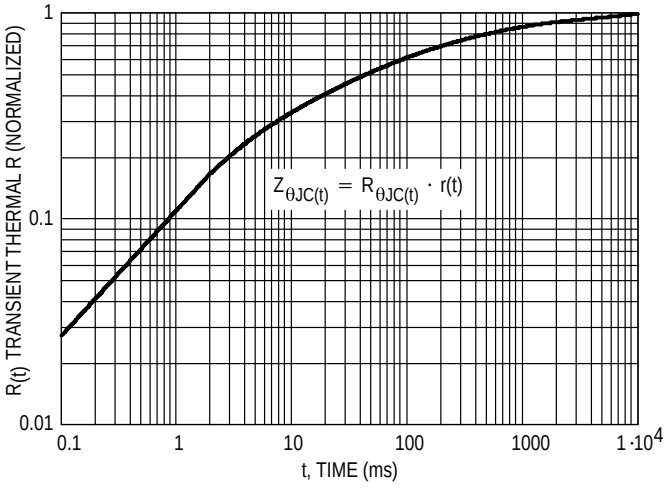



**Figure 4. Transient Thermal Response**

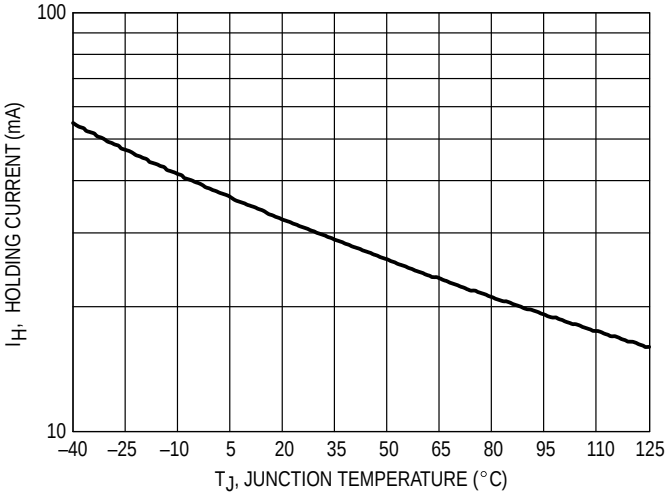



**Figure 5. Typical Holding Current Versus Junction Temperature**

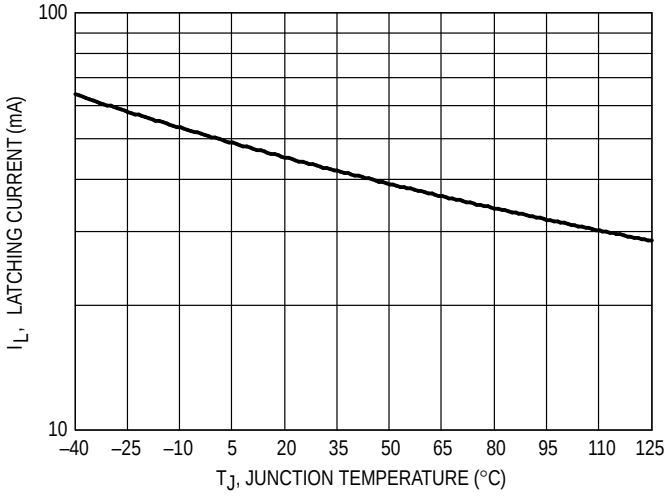



**Figure 6. Typical Latching Current Versus Junction Temperature**

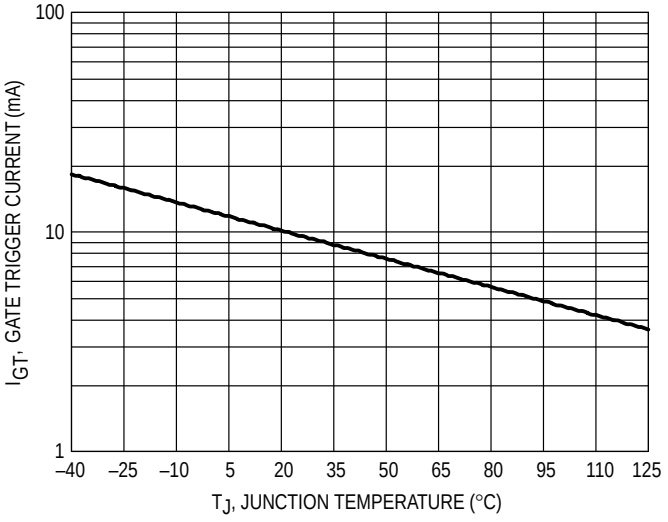



**Figure 7. Typical Gate Trigger Current Versus Junction Temperature**

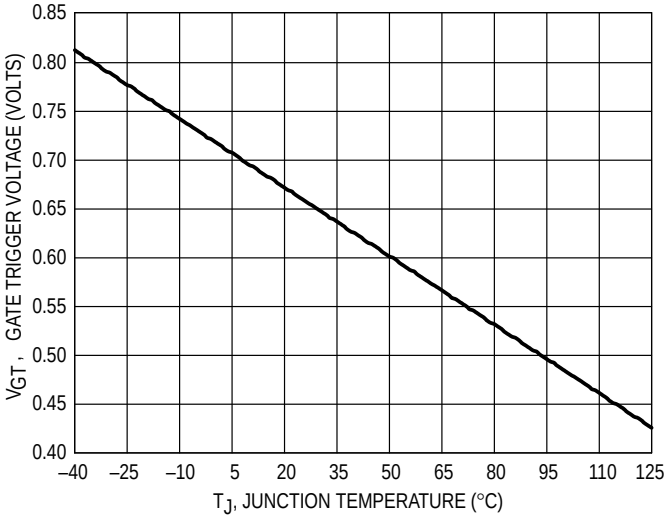



**Figure 8. Typical Gate Trigger Voltage Versus Junction Temperature**

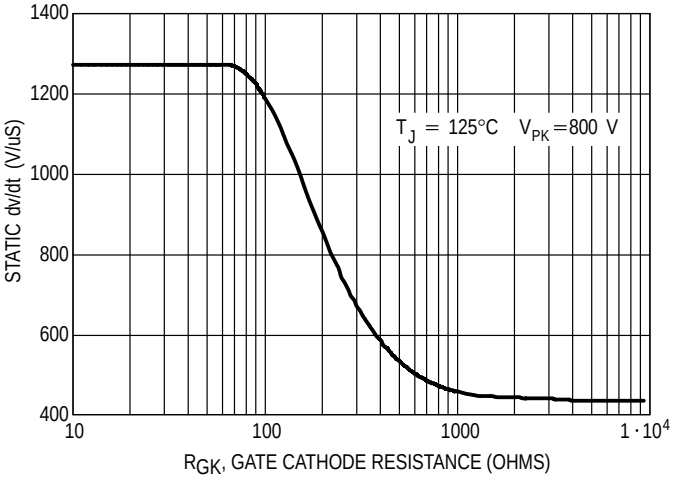



**Figure 9. Typical Exponential Static dv/dt Versus Gate Cathode Resistance.**

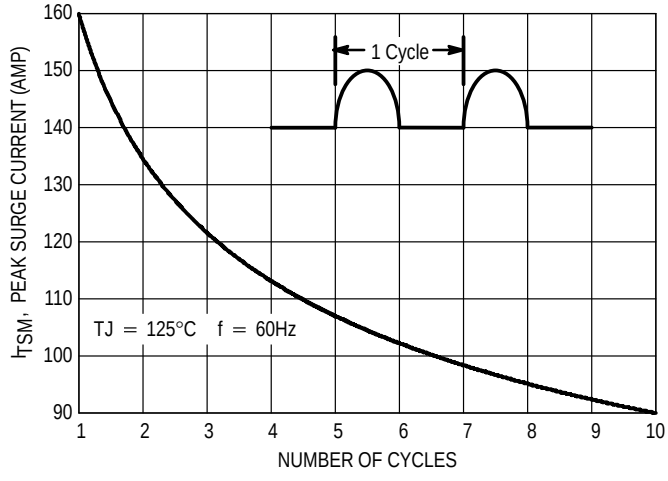
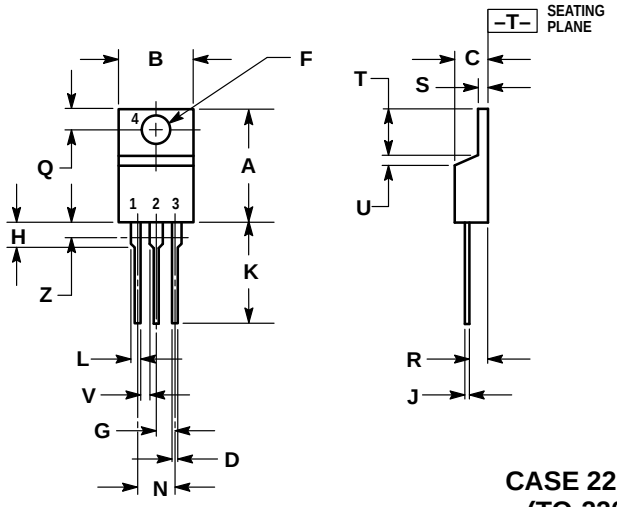



**Figure 10. Maximum Non–Repetitive Surge Current**

## PACKAGE DIMENSIONS




**CASE 221A–06**
**(TO-220AB)**

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.405 | 9.66 | 10.28 |
| C | 0.160 | 0.190 | 4.07 | 4.82 |
| D | 0.025 | 0.035 | 0.64 | 0.88 |
| F | 0.142 | 0.147 | 3.61 | 3.73 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.155 | 2.80 | 3.93 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.39 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | — | 1.15 | — |
| Z | — | 0.080 | — | 2.04 |



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