Initial Release

High Speed Quad MOSFET Driver

Features

- 6ns rise and fall time with 1000pF load
- 2A peak output source/sink current
- 1.2V to 5V input CMOS compatible
- 5V to 12V total supply voltage
- Smart Logic threshold
- Low jitter design
- Four matched channels
- Outputs can swing below ground
- Output is high impedence when disabled
- Low inductance package
- High-performance thermally-enhanced

Applications

- Medical ultrasound imaging
- Piezoelectric transducer drivers
- Nondestructive evaluation
- PIN diode driver
- CCD Clock driver/buffer
- High speed level translator

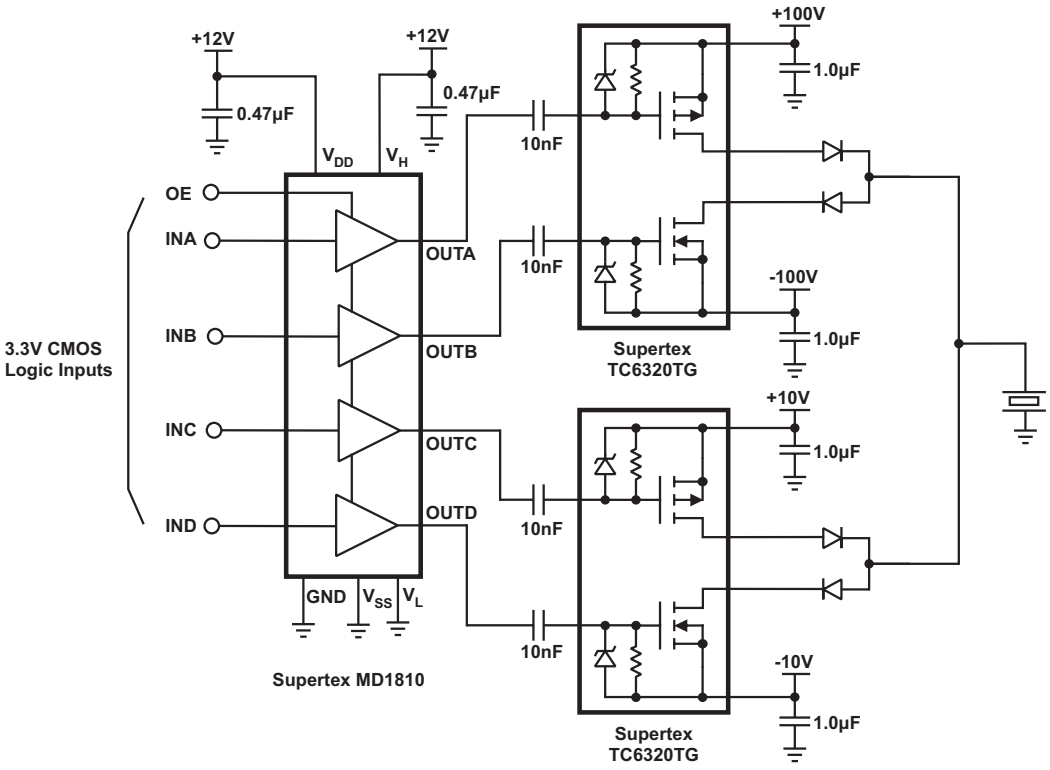
General Description

The Supertex MD1810 is a high-speed quad MOSFET driver. It is designed to drive high voltage P-and N-channel MOSFETs for medical ultrasound imaging applications. The MD1810 can also be used for ultrasound metal flaw detection, nondestructive evaluation test, piezoelectric transducer drive, clock drive, and PIN diode drive.

The MD1810 has four inputs which individually control four outputs. It also has an output enable (OE) pin. When OE is low, all of the outputs will be in a high impedance state regardless of their logic input control. When OE is high, the MD1810 sets the threshold logic transition to $(V_{OE}+V_{GND})/2$. This ensures the transition to always be at half the amplitude of the logic input signal. This allows the device to have inherent propagation delay matching regardless of the logic input amplitude.

The output stage of the MD1810 has separate power connections enabling the output signal L and H levels to be chosen independently from the V_{DD} and V_{SS} supply voltages. As an example, the input logic levels may be 0 and 1.8 volts, the control logic may be powered by +5 and –5 volts, and the output L and H levels may be varied anywhere over the range of –5 to +5 volts. The output stage is capable of peak currents of up to ±2 amps, depending on the supply voltages used and load capacitance present.

Typical Application Circuit



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Ordering Information

DEVICE	Package Option
	16-Lead 4x4x0.9 QFN
MD1810	MD1810K6-G
θ_{JA}	45°C/W (1oz. 4-layer 3x4inch PCB)

-G indicates package is RoHS compliant ('Green')

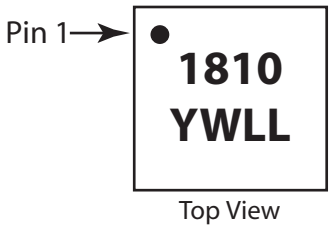
Absolute Maximum Ratings*

V_{DD}-V_{SS}, Logic Supply Voltage	-0.5V to +13.5V
V_H, Output High Supply Voltage	V_L-0.5V to V_{DD}+0.5V
V_L, Output Low Supply Voltage	V_{SS}-0.5V to V_H+0.5V
Vss, Low Side Supply Voltage	-7V to +0.5V
Logic Input Levels	V_{SS}-0.5V to V_{SS}+7V
Maximum Junction Temperature	+125°C
Storage Temperature	-65°C to 150°C
Soldering Temperature	235°C
Package Power Dissipation	2.2W

**Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

Product Marking Information		
1ST Line	Device Number	1810
2ND Line	Year, Week Code, Lot Number	YWLL

Example: 5A88 means Lot #88 of first or second week in 2005



Top View

DC Electrical Characteristics *($V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{OE} = 3.3V$, $T_J = 25°C$)*

Sym.	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{DD}-V_{SS}	Logic supply voltage	4.5		13	V	
V_{SS}	Low side supply voltage	-5.5		0	V	
V_H	Output high supply voltage	V_{SS}+2		V_{DD}	V	
V_L	Output low supply voltage	V_{SS}		V_{DD}-2	V	
I_{DDQ}	V_{DD} quiescent current		0.8		mA	No input transitions, OE = 1
I_{HQ}	V_H quiescent current			10	µA	
I_{DD}	V_{DD} average current		7.0		mA	One channel on at 5.0Mhz, No load
I_H	V_H average current		18		mA	
V_{IH}	Input logic voltage high	V_{OE}-0.3		5	V	For logic inputs INA, INB, INC, and IND
V_{IL}	Input logic voltage low	0		0.3	V	
I_{IH}	Input logic current high			1.0	µA	
I_{IL}	Input logic current low			1.0	µA	
V_{IH}	OE Input logic voltage high	1.2		5	V	For logic input OE
V_{IL}	OE Input logic voltage low	0		0.3	V	
R_{IN}	Input logic impedance to GND	12	20	30	KΩ	
C_{IN}	Logic input capacitance		5	10	pF	

Outputs *($V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{OE} = 3.3V$, $T_J = 25°C$)*

Sym.	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{SINK}	Output sink resistance			12.5	Ω	I_{SINK} = 50mA
R_{SOURCE}	Output source resistance			12.5	Ω	I_{SOURCE} = 50mA
I_{SINK}	Peak output sink current		2.0		A	
I_{SOURCE}	Peak output source current		2.0		A	

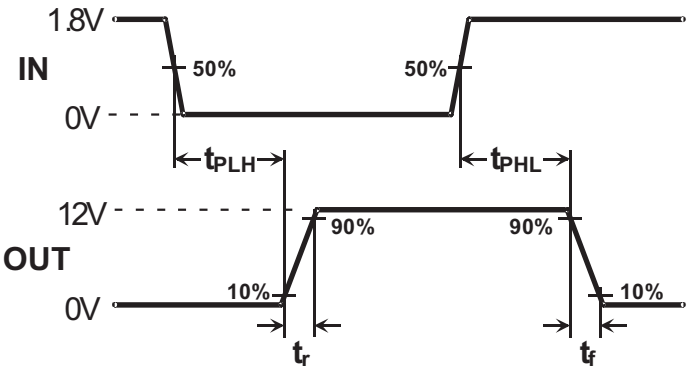
AC Electrical Characteristics ($V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{OE} = 3.3V$, $T_J = 25°C$)

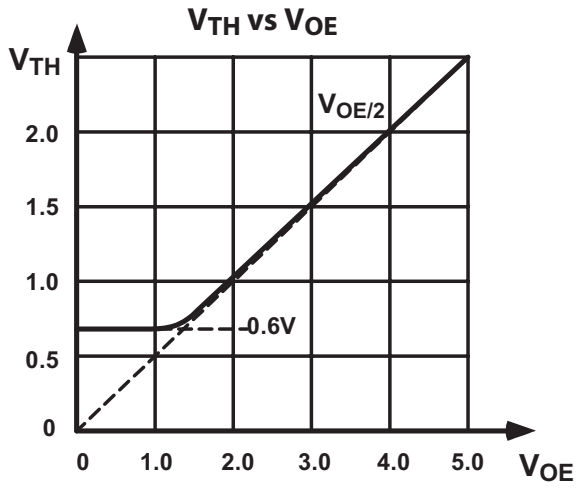
Sym.	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{irf}	Input or OE rise & fall time			10	ns	Logic input edge speed requirement
t_{PLH}	Propagation delay when output is from low to high		7		ns	C_{LOAD} = 1000pF, see timing diagram Input signal rise/fall time 2ns
t_{PHL}	Propagation delay when output is from high to low		7		ns	
t_{POE}	Propagation delay OE to output		9		ns	
t_r	Output rise time		6		ns	
t_f	Output fall time		6		ns	
$\lvert t_r - t_f \rvert$	Rise and fall time matching		1.0		ns	for each channel
$\lvert t_{PLH} - t_{PHL} \rvert$	Propagation low to high and high to low matching		1.0		ns	
Δt_{dm}	Propagation delay matching		±2.0		ns	Device to device delay match

Logic Truth Table

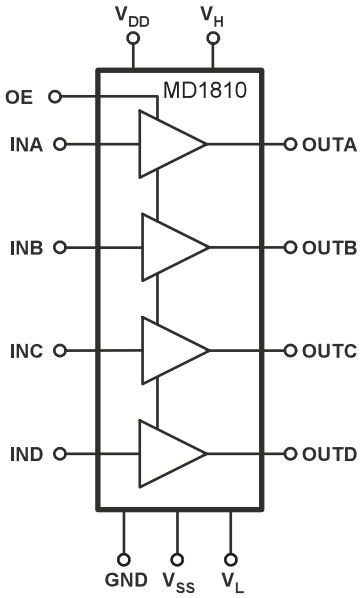
Logic Inputs		Output
OE	IN	
H	L	V_L
H	H	V_H
L	X	High Z

Timing Diagram and V_{TH} / V_{OE} Curve

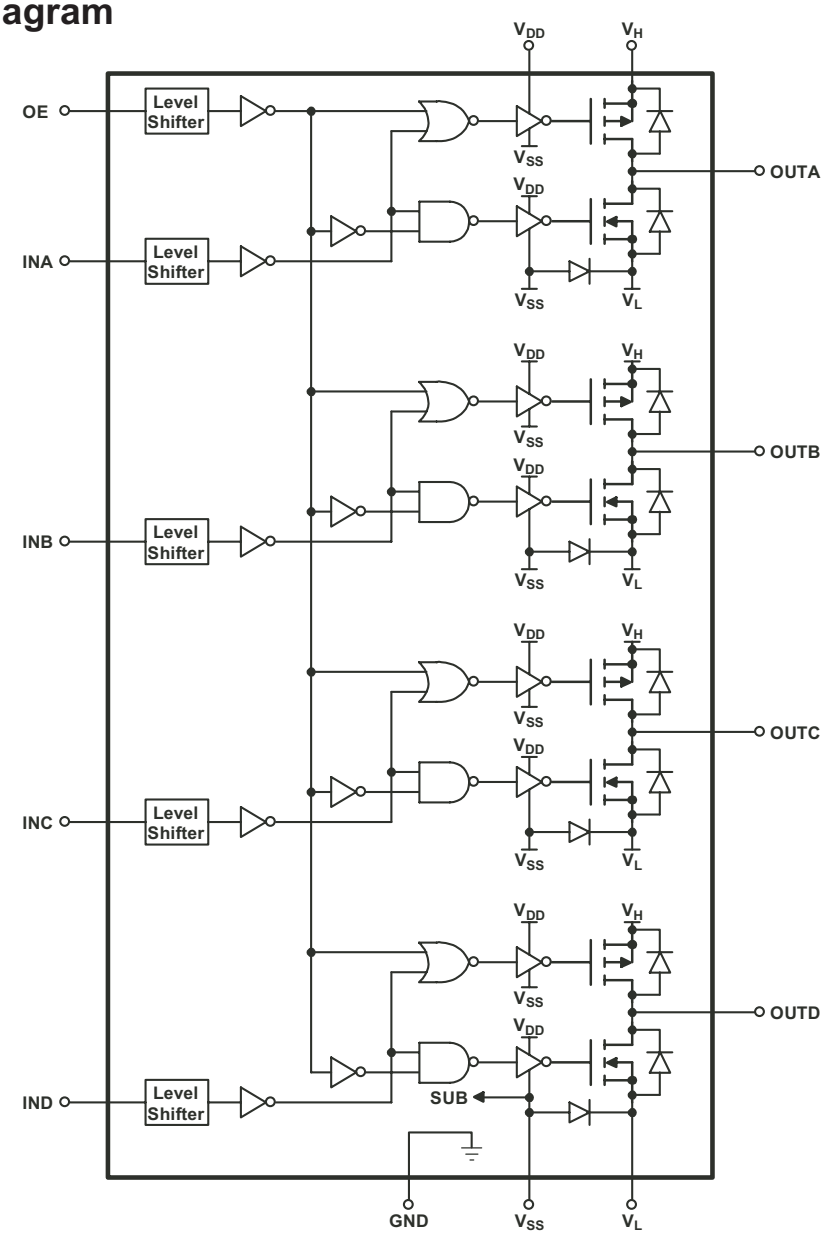




Simplified Block Diagram



Detailed Block Diagram



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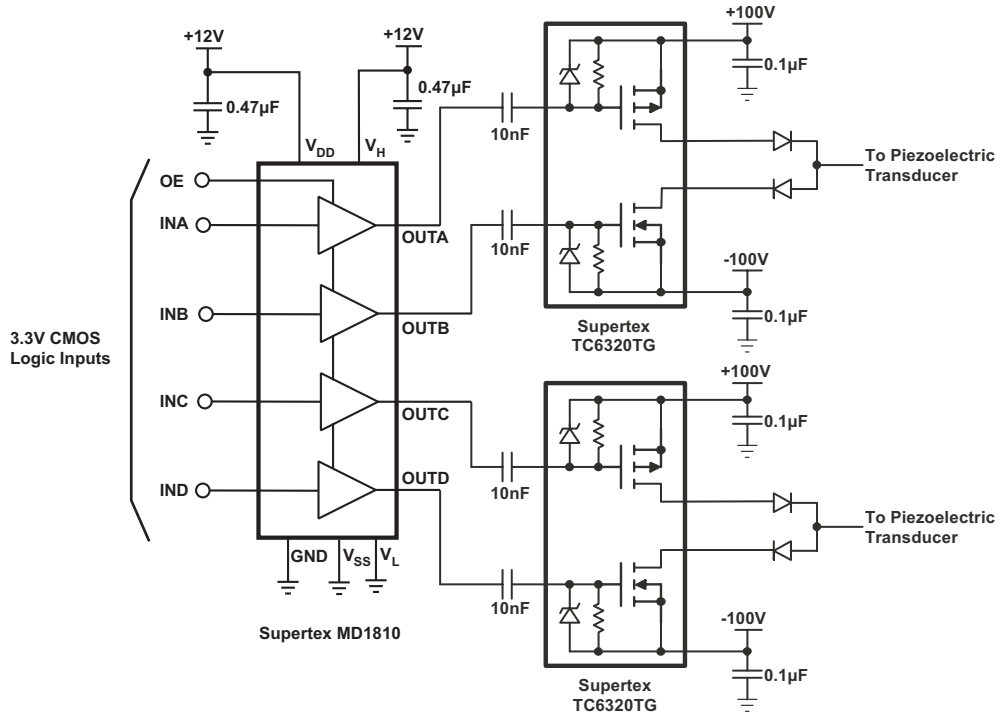
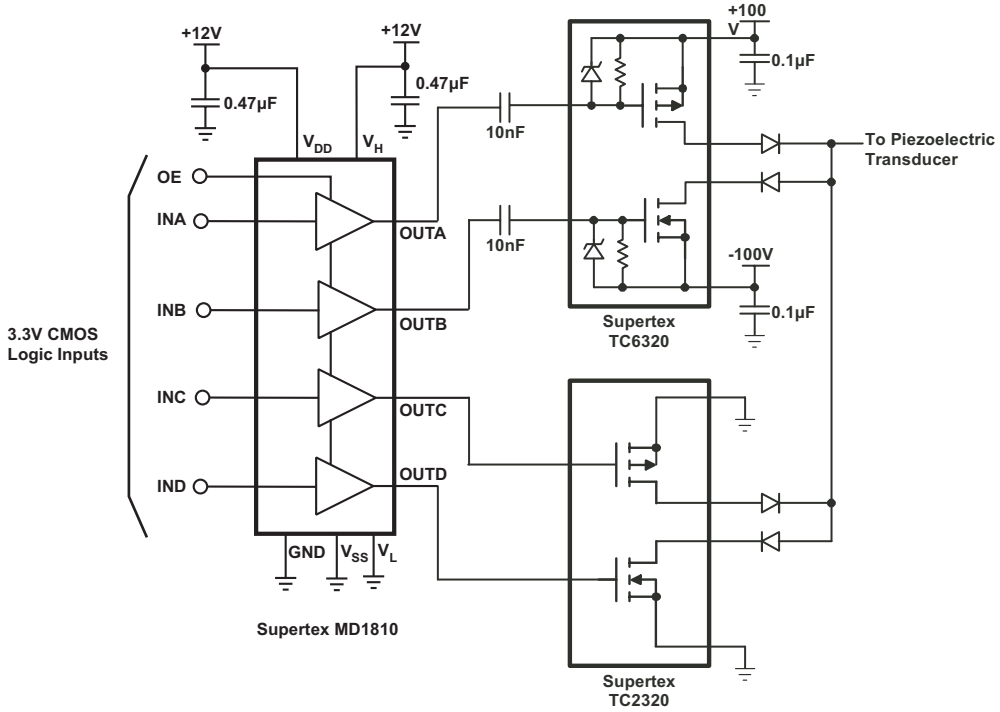
Typical Applications

2-Channel +100V to -100V Pulser



Single Channel ±100V to 0V Pulser



Application Information

For proper operation of the MD1810, low inductance bypass capacitors should be used on the various supply pins. The GND pin should be connected to the logic ground. The INA, INB INC, IND, and OE pins should be connected to a logic source with a swing of GND to V_{LL}, where V_{LL} is 1.2 to 5.0 volts. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1810 is capable of operating up to 100MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents that result with capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the V_{SS}, and V_L pins should have low inductance feed-through connections directly to a ground plane. If these voltages are not zero, then they need bypass capacitors in a manner similar to the positive power supplies. The power connection V_{DD} should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads.

The voltages of V_H and V_L decide the output signal levels. These two pins can draw fast transient currents of up to 2A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1.0µF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead coming to the capacitor. Pay particular attention to minimizing trace lengths, current loop area and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistance in series with the output signal to obtain better waveform transitions at the load terminals. This will of course reduce the output voltage slew rate at the terminals of a capacitive load.

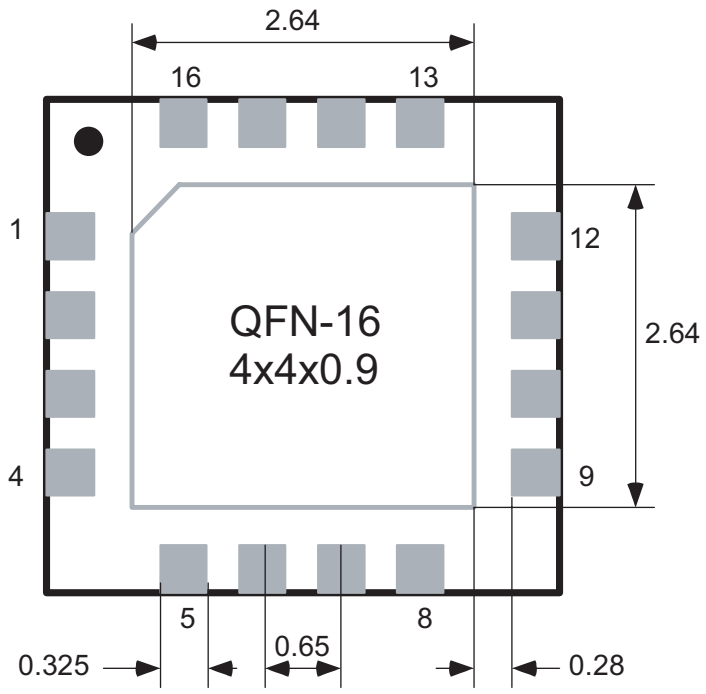
Pay particular attention that parasitic couplings are minimized from the output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.2V even small coupled voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Be careful that a circulating ground return current from a capacitive load cannot react with common inductance to cause noise voltages in the input logic circuitry.

Pin Description

V_{DD}	High side supply voltage.
V_{SS}	Low side supply voltage. V_{SS} is also connected to the IC substrate. It is required to connect to the most negative potential of voltage supplies and powered-up first.
V_H	Supply voltage for P-channel output stage.
V_L	Supply voltage for N-channel output stage.
GND	Logic input ground reference.
OE	Output enable logic input. When OE is high, $(V_{OE}+V_{GND})/2$ sets the threshold transition between logic level high and low. When OE is low, all outputs are at high impedance. Keep OE low until IC powered up.
INA, INB,INC, IND	Logic input. Input logic high will cause the output to swing to V_H. Input logic low will cause the output to swing to V_L. Keep all logic inputs low until IC powered up.
OUTA, OUTB, OUTC, OUTD	Output drivers
Substrate	The IC substrate is internally connected to the thermal pad. Thermal Pad and V_{SS} must be connected externally.

Pin Configuration

Pin #	Function
1	INB
2	V_L
3	GND
4	V_L
5	INC
6	IND
7	V_{SS}
8	OUTD
9	OUTC
10	V_H
11	V_H
12	OUTB
13	OUTA
14	V_{DD}
15	INA
16	OE
Note	Thermal Pad, and Pin #7 (V_{SS}), must be connected externally



(Top View, mm)

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