MD59-0022

PCS CDMA Upconverter / Driver 1710—1910 MHz

Features

- High Integrated Upconverter and Driver IC
- Operates over 2.7 V to 5V Supply Voltage
- +9 dBm Output Power at 51 dBc ACPR
- Low current mode for power saving at low output power
- Balanced IF Input 265 Ω
- Low LO Drive Level -10 dBm
- Operates in US and Korean PCS Bands
- Miniature TSSOP-16 Plastic Package

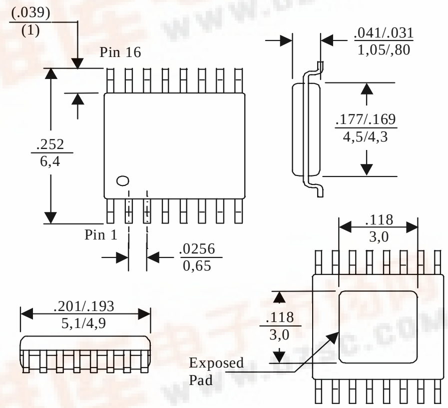
Description

M/A-COM's MD59-0022 is a fully integrated upconverter / Driver IC. It includes a balanced IF amplifier, upconverting mixer, two stage driver amplifier and LO buffer amplifier in a miniature TSSOP-16 plastic package. The backside of the lead frame is exposed to facilitate excellent RF grounding and thermal transfer.

The MD59-0022 is ideally suited for CDMA handset applications where high linearity and low power consumption are important transmitter requirements. The MD59-0022 can also operate in a low power mode to extend system battery life.

The MD59-0022 is fabricated using M/A-COM's 0.5 micron low noise E/D GaAs MESFET process. The process features full passivation for increased performance and reliability.

TSSOP-16 Plastic Package[1]



1. Dimensions are: in / mm

Ordering Information

Part Number	Package
MD59-0022TR	Forward Tape and Reel[1]
MD59-0022RTR	Reverse Tape and Reel[1]
MD59-0022SMB	Sample Board

1. If specific reel size is required, consult factory for part number assignment.

Electrical Specifications T_A = 25°C, V_{DD} = 3.0V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Complete Upconverter[1] / High Power Mode					
Conversion Gain	$V_{CTRL} = V_{DD}$	dB		24	27.2
CDMA Linear Output Power[2]	RF Frequency = 1710 - 1910 MHz	dBm		9	
Noise Figure	LO Frequency = 1580 - 1780 MHz	dB		10	
I_{DD}	LO Power = -10 dBm	mA		66	
VSWR (All Ports)	IF = 130 MHz			1.5:1	
IF Input Impedance		Ohms		265	
LO-to-RF Port Leakage		dBm		-18	
Complete UPconverter[1] / Low Power Mode					
Conversion Gain	V_{CTRL} = (0V)	dB		22	
CDMA Linear Output Power[2]	RF Frequency = 1710 - 1910 MHz	dBm		2	
Noise Figure	LO Frequency = 1580 = 1780 MHz	dB		10	
I_{DD}	LO Power = -10 dBm	mA		46	
VSWR (All Ports)	IF = 130 MHz			1.5:1	
IF Input Impedance		Ohms		265	
LO-to-RF Port Leakage		dBm		-18	
RF Driver Amplifier					
Gain	$V_{CTRL} = V_{DD}$, RF Frequency = 1710 - 1910 MHz	dB		TBD	
Gain	V_{CTRL} = 0V, RF Frequency = 1710 - 1910 MHz	dB		TBD	

1. Complete upconverter / driver measurements taken with a surface mount SAW filter between Mixer Ouput and Driver Input.
2. CDMA Linear power is defined as 51 dBc ACPR at a 1.228 MHz Offset from the carrier frequency.

Specifications subject to change without notice.

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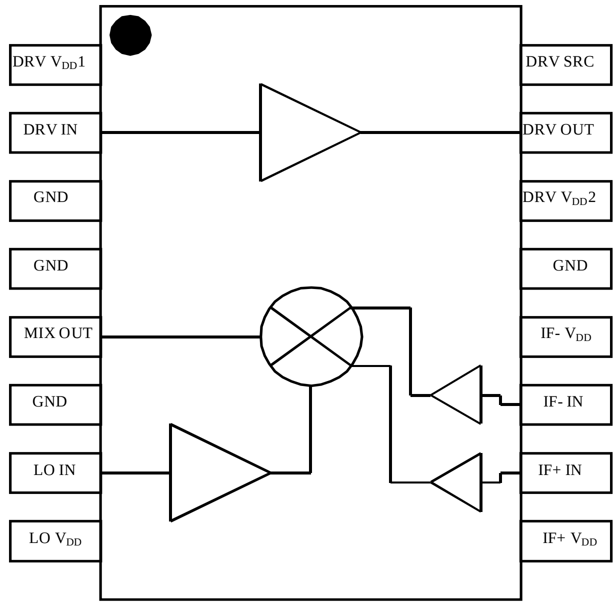
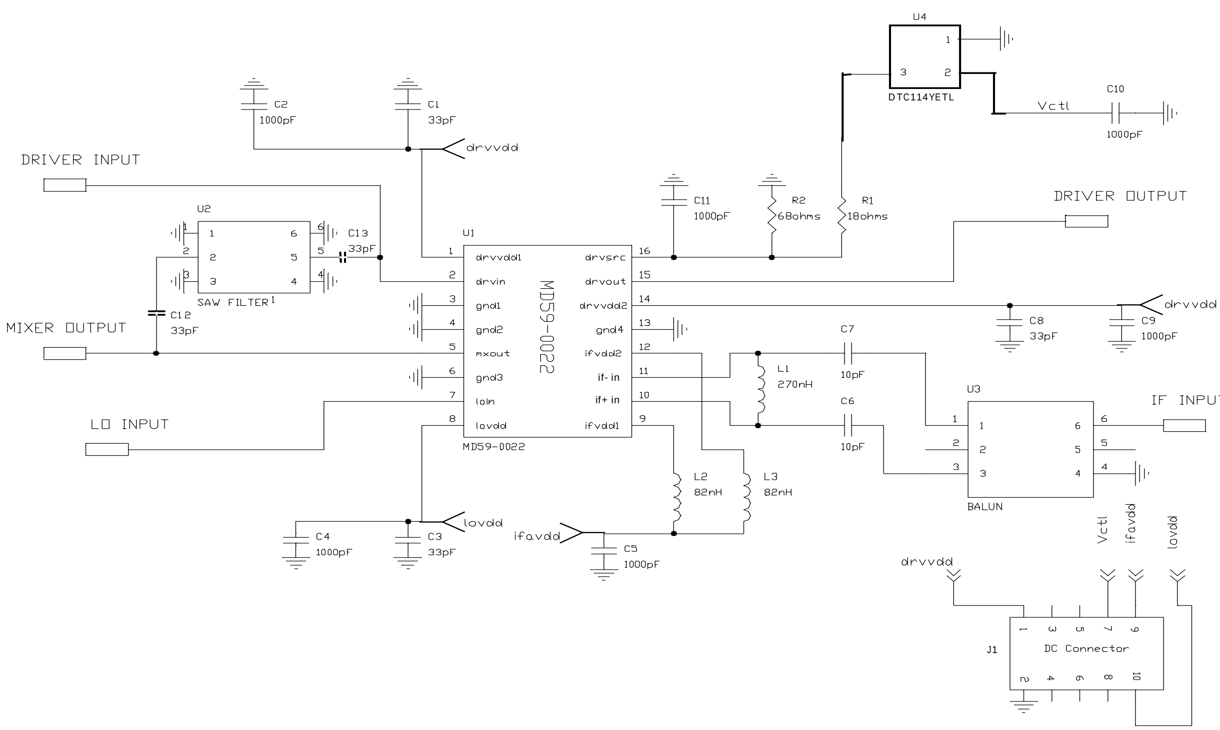
Pin Configuration

PIN No.	PIN	Description
1	DRV V_{DD}1	Driver Amplifier first stage supply voltage. Must be RF bypassed
2	DRV In	50 Ω Input to driver amplifier (DC blocking required)
3	GND	DC and RF Ground
4	GND	DC and RF Ground
5	MIX OUT	50 Ω Output of Mixer (DC blocked)
6	GND	DC and RF Ground
7	LO IN	Local Oscillator Input (-10 to -5 dBm) (DC blocked)
8	LO V_{DD}	LO Amplifier Supply Voltage - Bypassing required
9	IF+ V_{DD}	IF+ supply voltage. Off chip inductor and IF bypassing required
10	IF+ IN	IF+ input port. Off chip matching elements required
11	IF- IN IF- V_{DD}	IF- input port. Off chip matching elements required
12	IF- V_{DD}	IF- supply voltage. Off chip inductor and IF bypassing required
13	GND	DC and RF Ground
14	DRV V_{DD}2	Driver amplifier second stage supply voltage. Must be RF bypassed
15	DRV OUT	50 Ω output of Driver Amplifier (DC blocked internally)
16	DRV SRC	Source bias voltage of driver output stage. Required RF bypassing and may be used to control ouput stage current

Block Diagrams



Sample Board Schematic



1. Saw filter characteristics to be determined by customer, depending on band of operation. Sample boards are supplied without saw filter installed. Data supplied with sample board is measured over US PCS1900 Tx Bond using external K&L BPF (p/n SB121-1850/T450-0/OP) and 2 dB attenuation to emulate typical saw filter characteristics.

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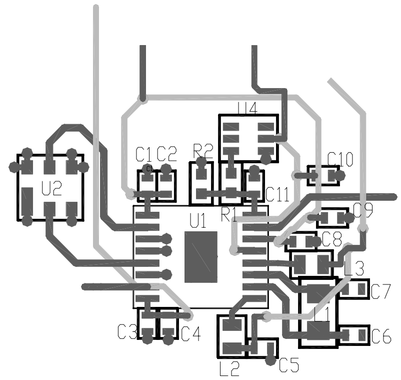
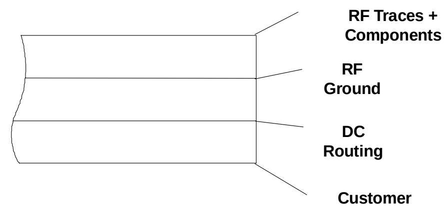
External Circuitry Parts List

Ref. Designation	Value	Purpose
C1, C3 C8	33 pF	RF Bypass
C2, C4, C5, C9, C10, C11, C12, C13	1000 pF	RF / IF Bypass
C6, C7	10 pF	IF Matching
L1	270 nH	IF Matching
L2, L3	82 nH	RF Choke
R1	18 Ω	Source Bias Resistor
R2	68 Ω	Source Bias Resistor for low current mode
U1		MD59-0022 Upconverter / Driver
U2		Filter LO and Image signals
U3	E Series XFMR	5:1 Transformer for IF matching
U4	DCT114Y ETL	Bipolar transistor for current switching (ROHM)
J1	DC Connect	10 PIN DC Connector

Recommended PCB Configuration



Cross Section View



Operating Instructions

The MD59-0022 is a highly integrated MMIC upconverter/driver for the 1710-1910 MHz PCS band. The upconverter/driver provides exceptional RF performance while consuming low DC current and is packaged in a low cost plastic package. It is ideal for light weight battery operated portable radio systems.

The transmit chain consists of a balanced IF amplifier, balanced mixer with single-ended RF output and a two stage RF driver amplifier as shown in the block diagram on the previous page. Surface mount resistors, inductors and capacitors are used in conjunction with the IC for an optimum performance, tunability and ease of use. A schematic, showing the IC and required external components, is shown on page 2.

An external self-bias resistor R1, which is RF bypassed, allows the current in the driver amplifier to be varied to obtain the required linear output power. By placing a bipolar transistor in series with the self-bias resistor, as shown in the schematic, the current consumption in the driver can be dynamically switched to provide a high and low power mode of operation. In high power mode, the bipolar transistor is on and the driver output stage is self-biased through R1 to provide +9 dBm of linear output power. By switching off the transistor, the output stage is biased through the higher resistance R2 thus reducing the current by ~25 mA to give 2 dBm of linear output power. The dual bipolar (U4) shown in the assembly drawing may be replaced by a smaller single transistor package with similar performance.

An external filter is required between the mixer output and driver amplifier input to reduce the amplitude of the image and local oscillator signals coming out of the mixer. This filter should have a 50 Ω input and output impedance. The mixer is a balanced resistive FET mixer which provides exceptional linearity and isolation with low loss and no DC current.

The IFA input ports are externally matched to 265 Ω differential impedance using two off chip capacitors and an off chip inductor. This allows maximum flexibility of intermediate frequency and IF filter. The IFA output ports are matched to the mixer using off chip inductors, which are also used for DC bias injection. A matching network such as that shown below can be used to match both the input and output of the IFA at the required frequency. The inductor also acts as a choke for the DC supply line.

The LO input port is internally matched to 50 Ω. A LO buffer amplifier amplifies the -10 dBm input signal to the level required to drive the mixer. Performance can be enhanced slightly with a drive level of -5 dBm.

All DC supply lines must be properly bypassed at RF frequencies to obtain optimum performance and at lower frequency to maintain unconditional stability. Capacitors C1, C3 and C8 are RF bypass capacitors for the LO amplifier and the driver amplifier. The value and placement of these capacitors are critical in determining the frequency response of these amplifiers. Capacitor C11 is a source bypass capacitor for the second stage of the driver amplifier. The placement of this capacitor will affect the gain of the amplifier. For best performance, all the RF bypass capacitors should be placed as shown in the recommended PCB diagram shown above. Capacitors C2, C4, C5 and C9 are 1000 pF low frequency DC supply bypass capacitors. Their value and placement are less critical than the other capacitors. However, for best results, these capacitors should be located as close to the package leads as possible.

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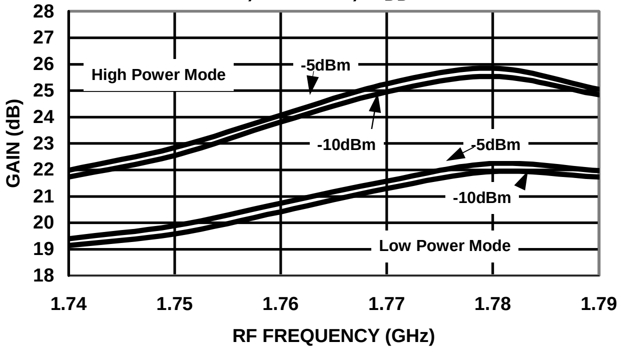
Typical Performance Curves

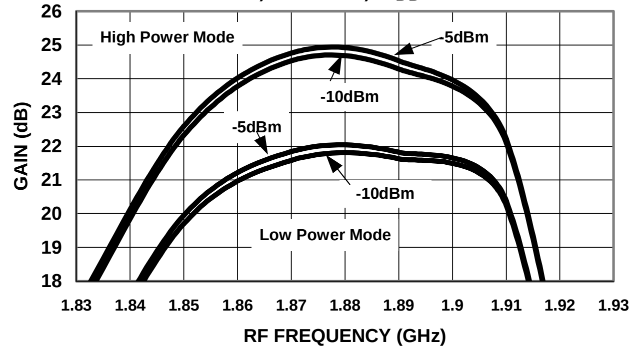
Korean PCS Band

Conversion Gain vs. Frequency
LO = -10dBm, -5 dBm, V_{DD} = 3.0V

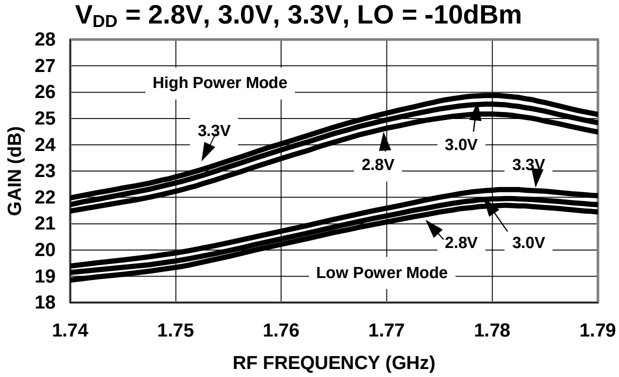


US PCS Band

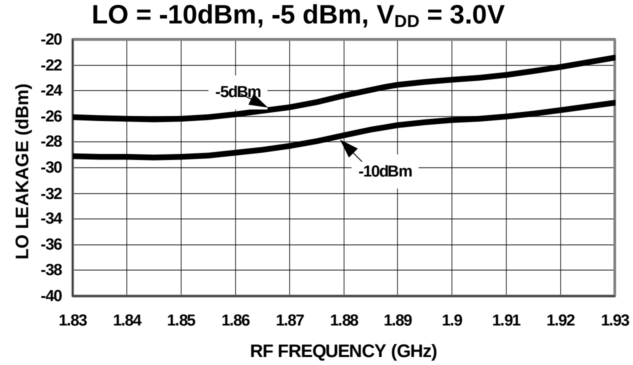
Conversion Gain vs. Frequency
LO = -10 dBm, -5 dBm, V_{DD} = 3.0V



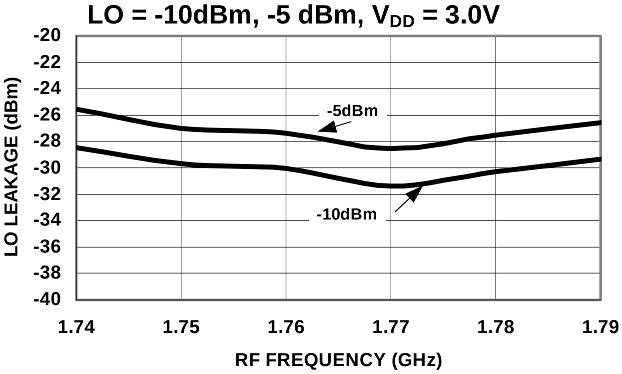
Conversion Gain vs. Frequency
V_{DD} = 2.8V, 3.0V, 3.3V, LO = -10dBm



LO-to-RF Leakage vs. Frequency
LO = -10dBm, -5 dBm, V_{DD} = 3.0V



LO-to-RF Leakage vs. Frequency
LO = -10dBm, -5 dBm, V_{DD} = 3.0V



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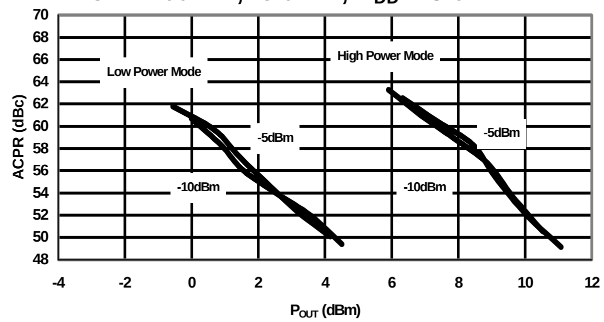
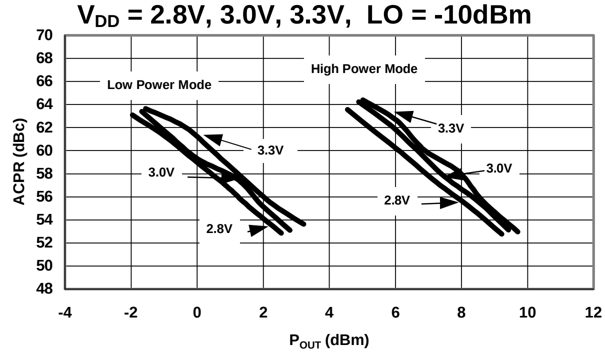
Typical Performance Curves (Cont'd)

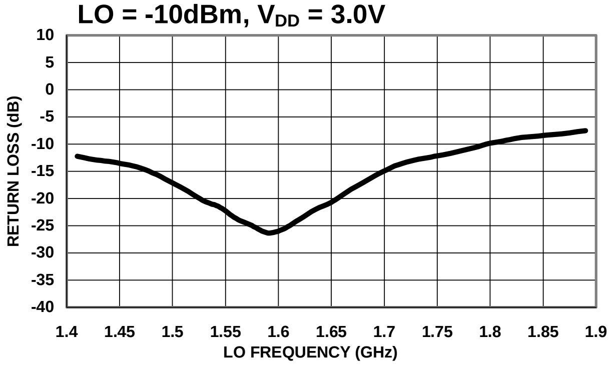
ACPR vs. Output Power
LO = -10dBm, -5 dBm, V_{DD} = 3.0V



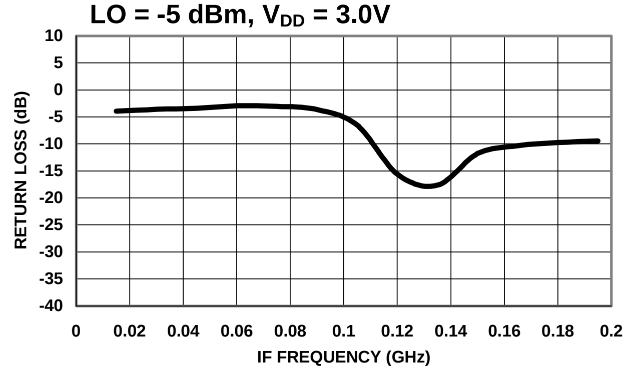
ACPR vs. Output Power
V_{DD} = 2.8V, 3.0V, 3.3V, LO = -10dBm



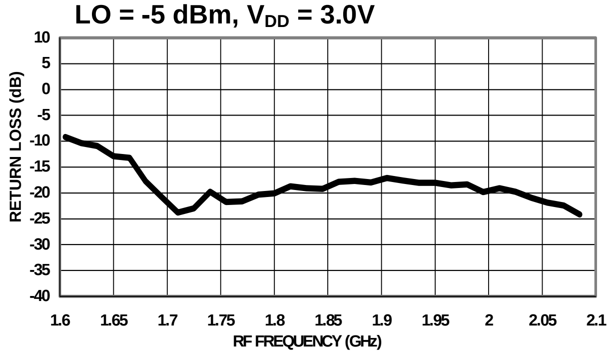
Lo Input Return Loss vs. Frequency
LO = -10dBm, V_{DD} = 3.0V



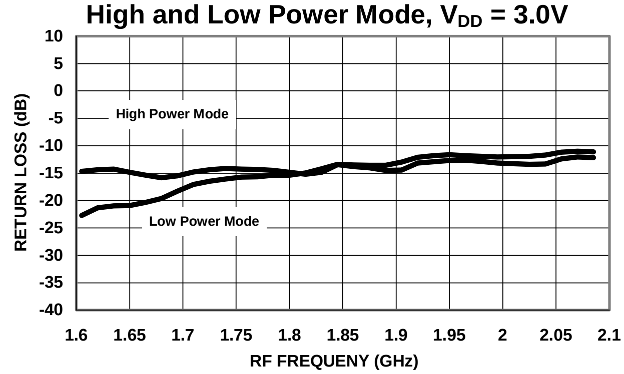
IF Input Return Loss vs. Frequency
LO = -5 dBm, V_{DD} = 3.0V



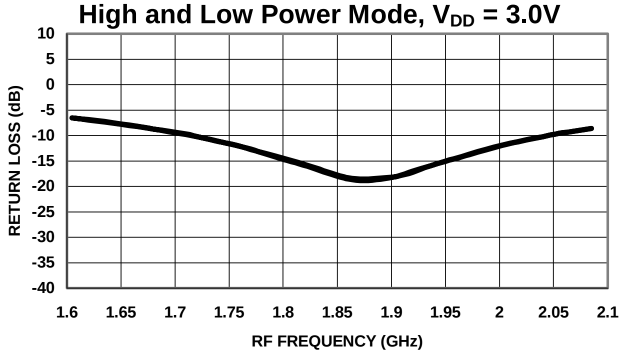
IF Input Return Loss vs. Frequency
LO = -5 dBm, V_{DD} = 3.0V



Driver Output Return Loss vs. Frequency
High and Low Power Mode, V_{DD} = 3.0V



Driver Input Return Loss vs. Frequency
High and Low Power Mode, V_{DD} = 3.0V



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