MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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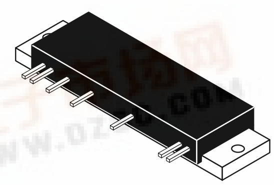
The RF Line
UHF Power Amplifier

MHW932

. . . designed specifically for the Pan European digital 20 watt, GSM mobile radio. The MHW932 is capable of wide power range control, operates from a 12.5 volt supply and requires 100 mW of RF input power.

- Specified 12.5 Volt Characteristics:
  RF Input Power — 100 mW (20 dBm)
  RF Output Power — 32 W
  Minimum Gain — 25 dB
  Harmonics — –35 dBc Max @ 2.0 f_o
- New Biasing and Control Techniques Providing Dynamic Range and Control Circuit Bandwidth Ideal for GSM
- 50 Ohm Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Test fixture circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**32 W
890 to 915 MHz
RF POWER
AMPLIFIER**



CASE 301S–02, STYLE 1

MAXIMUM RATINGS (Flange Temperature = 25°C)

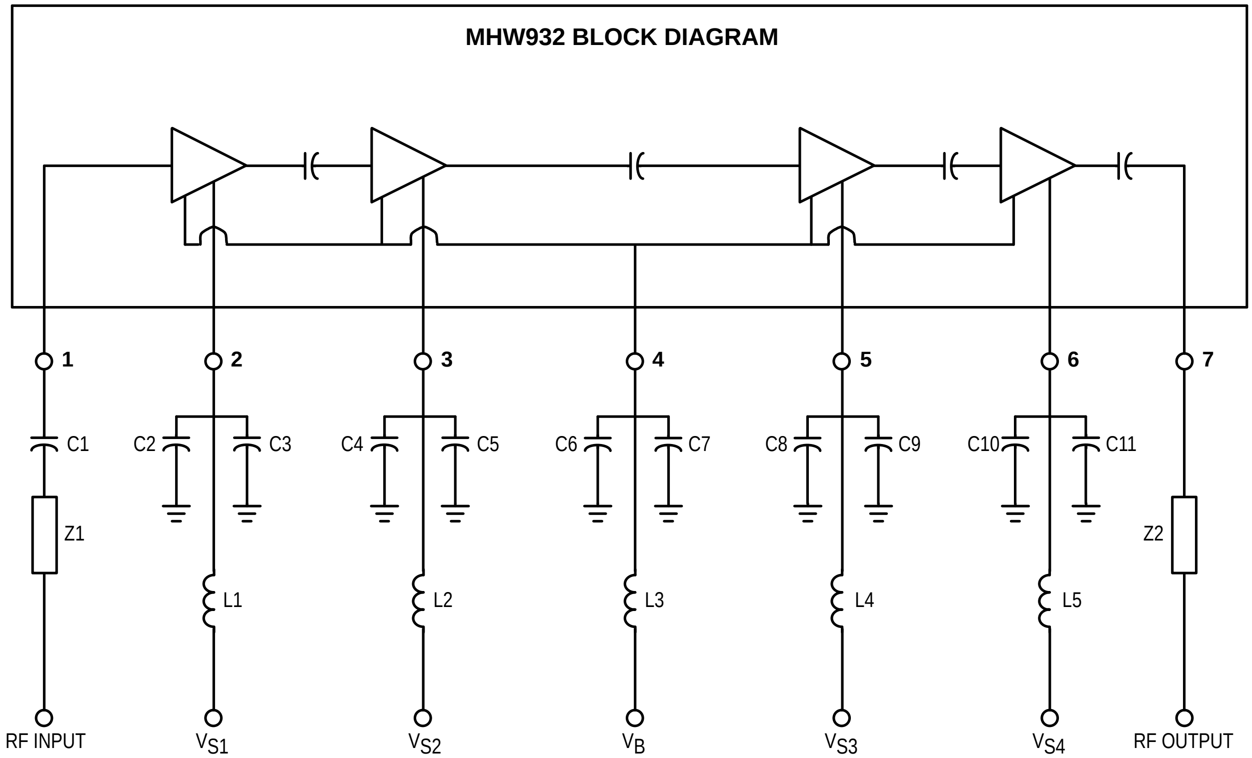
Rating	Symbol	Value	Unit
DC Supply Voltage	V_S	15.6	Vdc
DC Bias Voltage	V_B	5.25	Vdc
RF Input Power	P_{in}	400	mW
RF Output Power	P_{out}	40	W
Operating Case Temperature Range	T_C	–30 to +100	°C
Storage Temperature Range	T_{stg}	–30 to +100	°C

ELECTRICAL CHARACTERISTICS
($V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 12.5 Vdc; V_B = 5.0 Vdc, T_C = +25°C, 50 ohm system, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range	BW	890	915	MHz
Power Gain (P_{out} = 32 W) (1)	G_p	25	—	dB
Leakage Current (P_{in} = 0 mW, V_B = 0 Vdc, $V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 15.6 Vdc)	I_L	—	10	mA
Efficiency (P_{out} = 32 W) (1)	η	23	—	%
Input VSWR (P_{out} = 32 W) (1)	$VSWR_{in}$	—	2.0:1	—
Harmonics (P_{out} = 32 W) (1) 2.0 f_o 3.0 f_o to 5.0 f_o		—	–35 –45	dBc
Noise Power (In 30 kHz Bandwidth, 935 to 960 MHz frequency range; (P_{out} = 0.03 to 32 W; $V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 10.8 to 15.6 Vdc) (1)		—	–65	dBm
Linearity — % AM in Output (P_{out} = 0.02 to 32 W; 135 kHz, 1% AM in Input)	—	—	6.0	%
Output Power, Low Voltage (P_{IN} = 100 mW; $V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 10.8 Vdc)	P_{out2}	24	—	W
Load Mismatch Stress ($V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 15.6 Vdc; P_{out} = 40 W; Load VSWR = 10:1, All Phase Angles at Frequency of Test) (1)	ψ	No Degradation In Output Power Before and After Test		
Stability ($V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 10.8 to 15.6 Vdc; P_{out} = 0.03 to 32 W; Load VSWR = 6:1, Source VSWR = 3:1, All Phase Angles at Frequency of Test) (1)	—	All Spurious Outputs More Than 60 dB Below Desired Signal		

NOTE:
1. Adjust P_{in} for Specified P_{out}; Duty Cycle = 12.5%, Period = 4.6 msec

MOTOROLA



Pin Designations:

Pin 1 — RF Input Power @ 20 dBm Max Adjust for Output Power
Pin 2 — First Stage Collector Voltage @ 12.5 Vdc
Pin 3 — Second Stage Collector Voltage @ 12.5 Vdc
Pin 4 — Trickle Bias Voltage @ 5.0 Vdc
Pin 5 — Third Stage Collector Supply @ 12.5 Vdc
Pin 6 — Fourth Stage Collector Supply @ 12.5 Vdc
Pin 7 — RF Output Power @ 32 W Nominal

Element Values:

C1 = C2 = C4 = C6 = C8 = C10 = 0.018 µF
C3 = C5 = C7 = C9 = C11 = 2.2 µF
L1 – L3 = 0.29 µH
L4 = 0.2 µH
L5 — VR200, Up to 10 A Max IS4
Z1, Z2 = 50 Ohm Microstrip

Figure 1. Test Circuit Diagram

TYPICAL CHARACTERISTICS

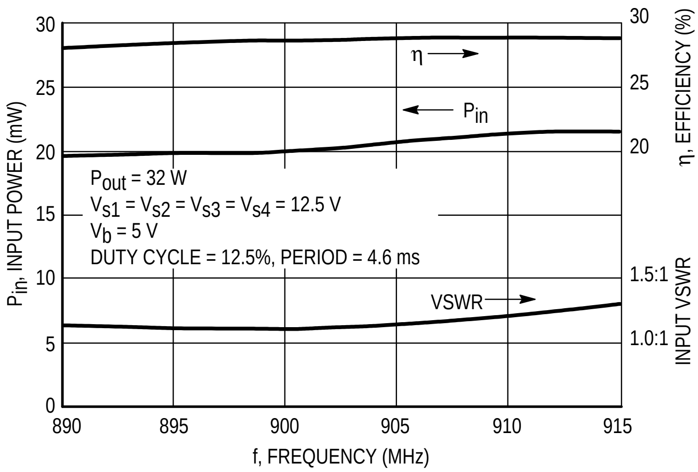


Figure 2. Input Power, Efficiency and Input VSWR versus Frequency

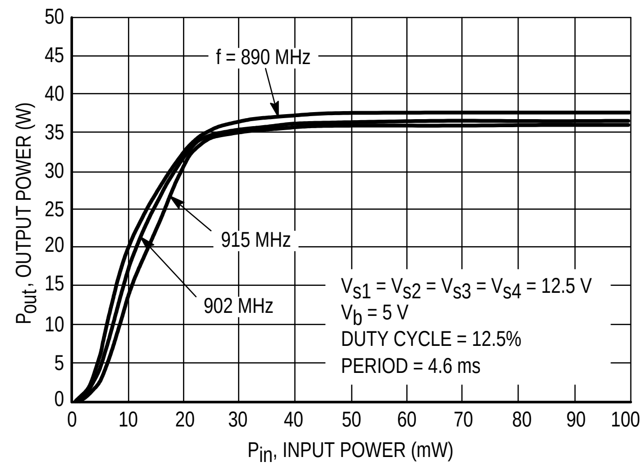


Figure 3. Output Power versus Input Power

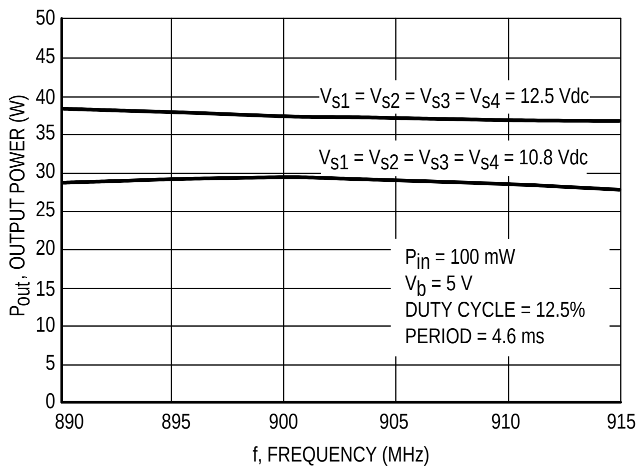


Figure 4. Output Power versus Frequency

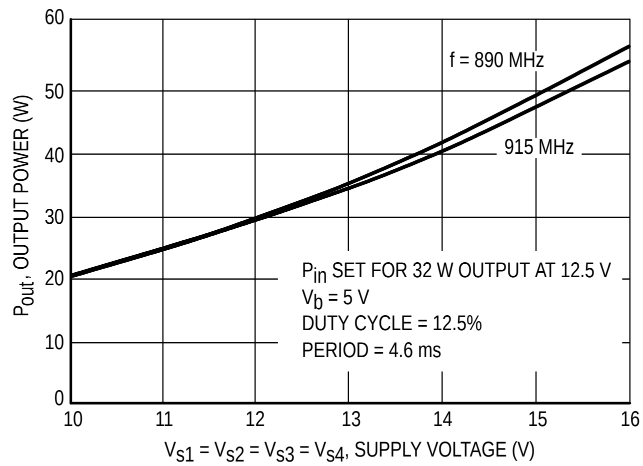


Figure 5. Output Power versus Supply Voltage

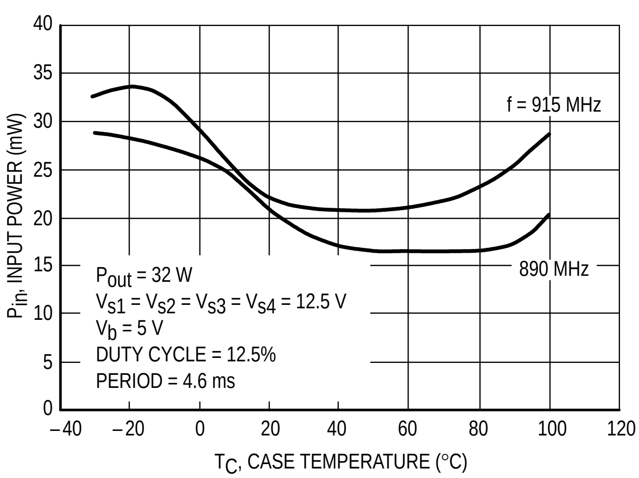


Figure 6. Input Power versus Case Temperature

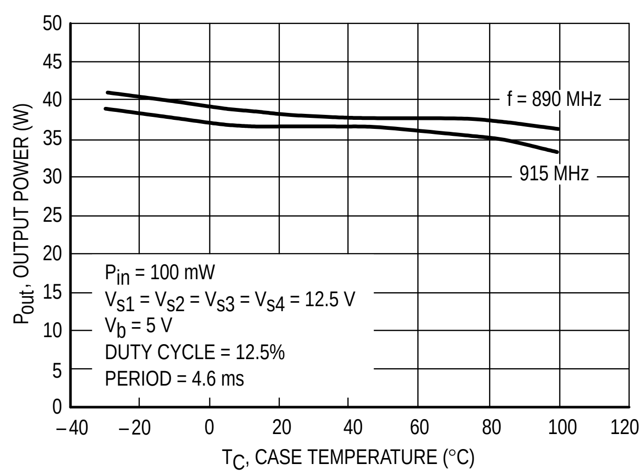


Figure 7. Output Power versus Case Temperature for Maximum Input Power

APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of $V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 12.5 Vdc (Pins 2, 3, 5, 6), and V_b = 5.0 Vdc (Pin 4). With these conditions, maximum current density on any device is 1.5 x 10^5 A/cm^2 and maximum die temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

GAIN CONTROL

The module output power should be limited to specified value. The preferred method of power control is to fix $V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 12.5 Vdc (Pins 2, 3, 5, 6), V_b = 5.0 Vdc (Pin 4), and vary P_{in} (Pin 1) from 0 to 100 mW.

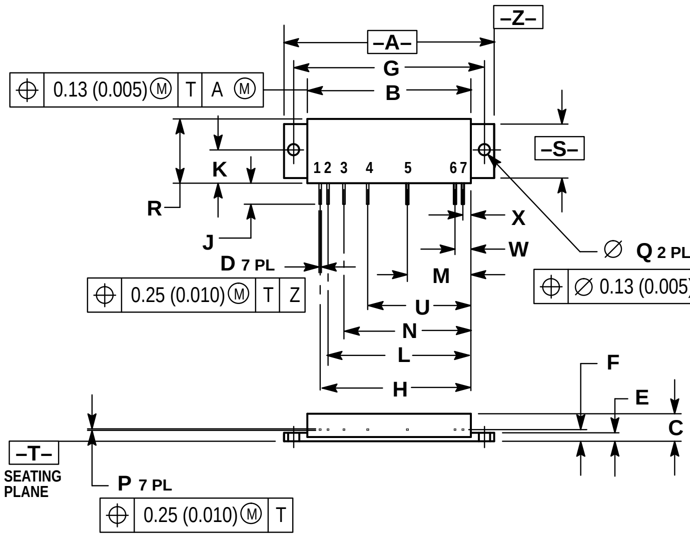
DECOUPLING

Due to the high gain of the four stages and the module size limitation, external decoupling networks require careful consideration, Pins 2, 3, 4, 5, and 6 are internally bypassed with a 0.018 µF chip capacitor which is effective for frequencies from 5.0 MHz through 940 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

LOAD MISMATCH

During final test each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are $V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 15.6 Vdc (Pins 2, 3, 5, 6), and V_b = 5.0 Vdc (Pin 4), VSWR equal to 10:1, and output power equal to 40 watts.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.640	2.660	67.06	67.56
B	2.040	2.085	51.82	52.95
C	0.335	0.360	8.51	9.14
D	0.018	0.022	0.46	0.56
E	0.100	0.115	2.54	2.92
F	0.147 BSC		3.73 BSC	
G	2.405 BSC		61.09 BSC	
H	1.900 BSC		48.26 BSC	
J	0.400	0.440	10.16	11.18
K	0.177	0.217	4.50	5.51
L	1.800 BSC		45.72 BSC	
M	0.800 BSC		20.32 BSC	
N	1.600 BSC		40.64 BSC	
P	0.008	0.012	0.21	0.30
Q	0.136	0.146	3.45	3.71
R	0.800	0.820	20.32	20.83
S	0.670	0.690	17.02	17.53
U	1.300 BSC		33.02 BSC	
W	0.200 BSC		5.08 BSC	
X	0.100 BSC		2.54 BSC	

STYLE 1:
PIN 1. RF INPUT
2. DC TERMINAL, Vs1
3. DC TERMINAL, Vs2
4. DC TERMINAL, Vb
5. DC TERMINAL, Vs3
6. DC TERMINAL, Vs4
7. RF OUTPUT

CASE 301S–02
ISSUE A

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