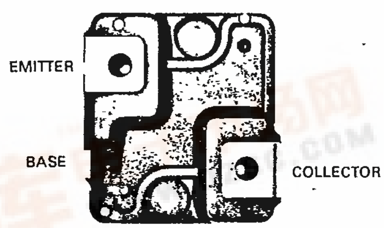
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

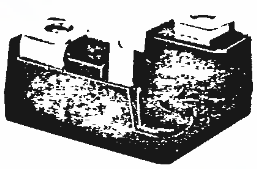
MJ10042
MJ10045
MJ10048

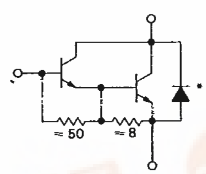
Designer's Data Sheet

25 KVA ENERGY MANAGEMENT SERIES SWITCHMODE DARLINGTON TRANSISTORS 25, 50 and 100 Ampere Operating Current

These Darlington transistors are designed for industrial service under practical operating environments found in switching high power inductive loads off 120, 230 and 460 Volt lines.







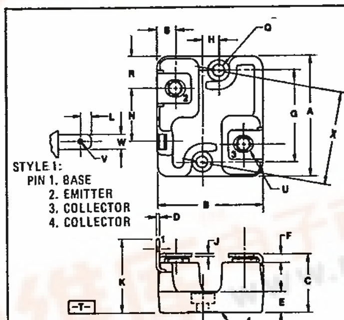
*Emitter-Collector Diode is a high power diode.

25, 50, and 100 AMPERE NPN SILICON POWER DARLINGTON TRANSISTOR

250, 450 and 850 VOLTS 250 WATTS

Designer's Data for "Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ | Ø 0 25 (0 010) Ⓜ | T | A Ⓜ | B Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH EXCEPT FOR METRICALLY THREADED INSERTS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.11	40.13	1.540	1.580
B	33.93	34 95	1 336	1.376
C	–	20.32	–	0.800
D	0.68	0 83	0 027	0 033
E	8 30	8 81	0 327	0 347
F	–	4 44	–	0.175
G	29 67 BSC		1.168 BSC	
H	5 08 BSC		0 200 BSC	
J	0.93	1.09	0 037	0 043
K	–	25 40	–	1.000
L	2 92	3.30	0 115	0.130
N	17.14	17 39	0 675	0 685
Q	3.73	3 88	0.147	0.153
R	10.41	10.79	0.410	0.425
S	5.84	6 35	0 230	0.250
U	M5 .8 (METRIC THRD)			
V	1.27	1.52	0.050	0 060
W	4 69	4 85	0 185	0 191
X	30.15 BSC		1.187 BSC	

CASE 353-01

MAXIMUM RATINGS

Mechanical Ratings		
Rating	Value	Unit
Mounting Torque (To heat sink with 6-32 Screw) (Note 1)	8.0	in.-lb
Lead Torque (Lead to bus with 5 mm Screw) (Note 2)	20	in.-lb
Per Unit Weight	41	grams

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.5	°C/W

Mica Insulators available as separate items.
0.003" thick. Motorola Part Number 14CSB12387B003.

Notes:
1. A Belleville washer of 0.281" O.D., 0.138" I.D., 0.013" thick and 43 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.50".
3. To adapt the collector and emitter terminals to quick connect terminals, AMP 250 Series Faston tab P/N 61499-1 is suggested.
4. The mounting holes of this package are compatible with TO-204 (formerly TO-3) mounting holes.

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MAXIMUM RATINGS (Continued) (T_C = 25°C unless otherwise noted.)

Rating	Symbol	MJ10042	MJ10045	MJ10048	Unit
Collector-Emitter Voltage (I_B = 0)	V_{CEO}	850	450	250	Vdc
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	900	500	300	Vdc
Collector-Base Voltage	V_{CB}	900	500	300	Vdc
Emitter-Base Voltage	V_{EB}		8.0		Vdc
Collector Current — Operating (T_C = 115°C) (T_C = 85°C) (T_C = 85°C)	$I_{C(op)}$	25 — —	— 50 —	— — 100*	A
Collector Current — Continuous — Peak Repetitive — Peak Nonrepetitive	I_C	37.5 75 125	75 150 250	100 300 500	A
Base Current — Continuous — Peak Nonrepetitive	I_B		25 50		A
Total Device Dissipation Derate above T_C = 25°C For 1-minute overload	P_D		250 2.0 333		Watts W/°C Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}		-55 to +150 -55 to 200		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 125 mAdc) MJ10042 MJ10045 MJ10048	$V_{CEO(sus)}$	850 450 250	— — —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	— —	2.0 10	mA
Collector Cutoff Current (V_{CE} = Rated V_{CER}, R_{BE} = 10 Ω, T_C = 100°C)	I_{CER}	—	10	mA
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	350	mA
SAFE OPERATING AREA				
Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figures 32, 34 & 36		
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figures 33, 35 & 37		
Overload Safe Operating Area	OLSOA	See Figures 38, 39, 40, 41, 42 & 43		
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	2000	pF

(1) Pulse Test. Pulse width of 300 μs, duty cycle ≤2.0%.
* This rating is with a 50% duty cycle, and is limited by power dissipation. Higher operating currents are allowable at lower duty cycles.

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ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
MJ10042				
DC Current Gain (I_C = 25 Adc, V_{CE} = 5.0 Vdc) (I_C = 25 Adc, V_{CE} = 10 Vdc)	h_{FE}	 35 40	 — —	
Collector-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 2.0 Adc) (I_C = 37.5 Adc, I_B = 7.5 Adc) (I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 25 Adc, I_B = 2.0 Adc) (I_C = 25 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 3.0 3.0	Vdc
MJ10045				
DC Current Gain (I_C = 50 Adc, V_{CE} = 5.0 Vdc) (I_C = 50 Adc, V_{CE} = 10 Vdc)	h_{FE}	 50 60	 — —	
Collector-Emitter Saturation Voltage (I_C = 50 Adc, I_B = 1.67 Adc) (I_C = 75 Adc, I_B = 6.0 Adc) (I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 2.0 3.3 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 50 Adc, I_B = 1.67 Adc) (I_C = 50 Adc, I_B = 1.67 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 3.0 3.0	Vdc
MJ10048				
DC Current Gain (I_C = 100 Adc, V_{CE} = 5.0 Vdc) (I_C = 100 Adc, V_{CE} = 10 Vdc)	h_{FE}	 75 90	 — —	
Collector-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 2.75 Adc) (I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — —	 2.0 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 100 Adc, I_B = 2.75 Adc) (I_C = 100 Adc, I_B = 2.75 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 3.0 3.0	Vdc

(1) Pulse Test: Pulse width of 300 μs, duty cycle ≤ 2.0%.

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ELECTRICAL CHARACTERISTICS (Continued) (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
MJ10042							
Resistive Load							
Delay Time	(V_{CC} = 300 Vdc, I_C = 25 A, I_{B1} = 2.0 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	1.2	5.0	
Storage Time			t_s	—	35	100	
Fall Time			t_f	—	8.5	35	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 25 A, V_{CEM} = 350 V, R_{BE} = 10 Ω, I_{B1} = 2.0 A)	T_J = 100°C	t_{sv}	—	50	150	μs
Crossover Time			t_c	—	20	60	
Storage Time		T_J = 25°C	t_{sv}	—	35	100	
Crossover Time			t_c	—	10	35	
MJ10045							
Resistive Load							
Delay Time	(V_{CC} = 250 Vdc, I_C = 50 A, I_{B1} = 1.67 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.03	0.25	μs
Rise Time			t_r	—	0.9	3.0	
Storage Time			t_s	—	10	25	
Fall Time			t_f	—	3.0	10	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 50 A, V_{CEM} = 250 V, R_{BE} = 10 Ω, I_{B1} = 1.67 A)	T_J = 100°C	t_{sv}	—	15	50	μs
Crossover Time			t_c	—	4.0	15	
Storage Time		T_J = 25°C	t_{sv}	—	10	25	
Crossover Time			t_c	—	2.7	10	
MJ10048							
Resistive Load							
Delay Time	(V_{CC} = 150 Vdc, I_C = 100 A, I_{B1} = 2.75 A, R_{BE} = 10 Ω, t_p = 50 μs, Duty Cycle ≤ 2.0%)		t_d	—	0.035	0.25	μs
Rise Time			t_r	—	1.2	4.0	
Storage Time			t_s	—	6.3	20	
Fall Time			t_f	—	2.5	8.0	
Inductive Load, Clamped							
Storage Time	(I_{CM} = 100 A, V_{CEM} = 150 V, R_{BE} = 10 Ω, I_{B1} = 2.75 A)	T_J = 100°C	t_{sv}	—	9.0	30	μs
Crossover Time			t_c	—	3.3	12	
Storage Time		T_J = 25°C	t_{sv}	—	6.5	20	
Crossover Time			t_c	—	2.3	8.0	
C-E DIODE CHARACTERISTICS							
Power Dissipation (I_B = 0)			P_D	—	—	125	W
Single Cycle Surge Current (60 Hz)			I_{FSM}	—	—	250	Apk
Forward Voltage (1)			V_F				Vdc
(I_F = 25 Adc)	MJ10042			—	—	1.5	
(I_F = 50 Adc)	MJ10045			—	—	1.5	
(I_F = 100 Adc)	MJ10048			—	—	2.0	
Reverse Recovery Time (d_i/d_t = 25 A/μs)			t_{rr}				μs
(I_F = 25 Adc)	MJ10042			—	4.0	12	
(I_F = 50 Adc)	MJ10045			—	3.3	10	
(I_F = 100 Adc)	MJ10048			—	2.5	8.0	
Forward Turn-On Time (Compliance Voltage = 250 V)			t_{on}				μs
(I_F = 25 Adc)	MJ10042			—	0.3	1.2	
(I_F = 50 Adc)	MJ10045			—	0.3	1.0	
(I_F = 100 Adc)	MJ10048			—	1.0	3.5	

(1) Pulse Test Pulse width of 300 μs, duty cycle ≤2.0%.

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TYPICAL ELECTRICAL CHARACTERISTICS

MJ10042

FIGURE 1 — DC CURRENT GAIN

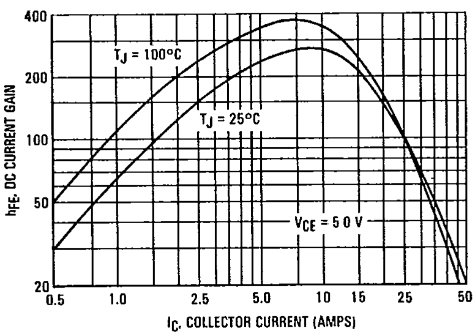
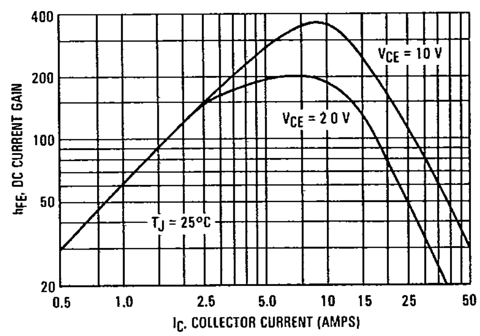


FIGURE 2 — DC CURRENT GAIN



MJ10045

FIGURE 3 — DC CURRENT GAIN

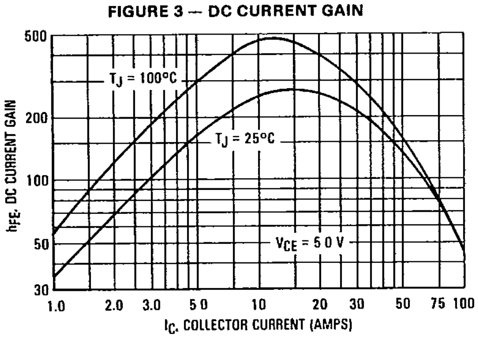
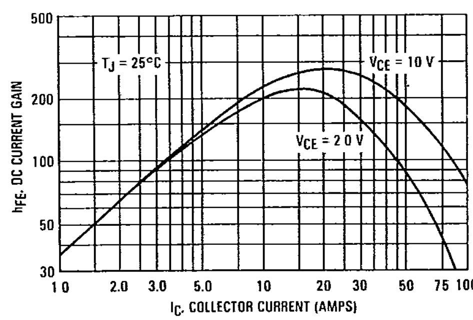


FIGURE 4 — DC CURRENT GAIN



MJ10048

FIGURE 5 — DC CURRENT GAIN

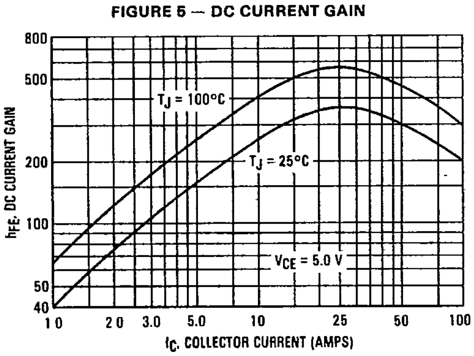
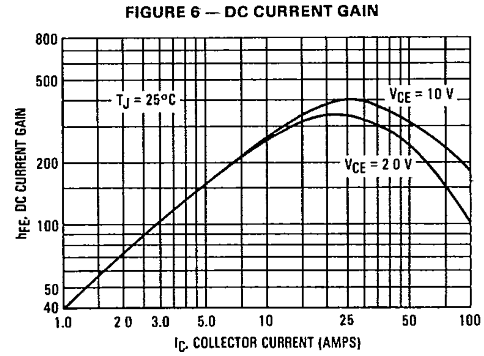


FIGURE 6 — DC CURRENT GAIN



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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 7 — DC CURRENT GAIN

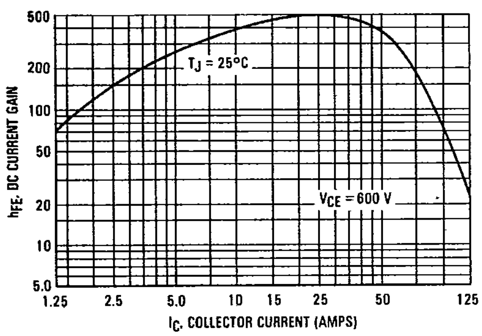

FIGURE 8 — COLLECTOR SATURATION VOLTAGE

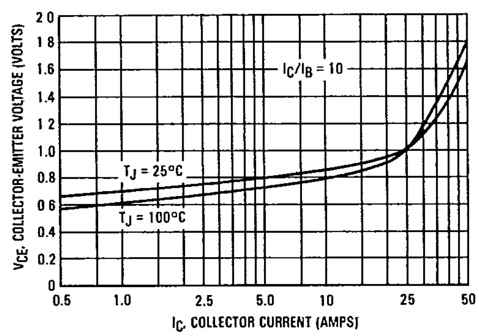

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FIGURE 9 — DC CURRENT GAIN

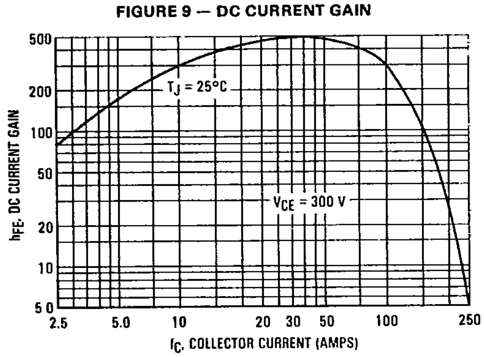

FIGURE 10 — COLLECTOR SATURATION REGION

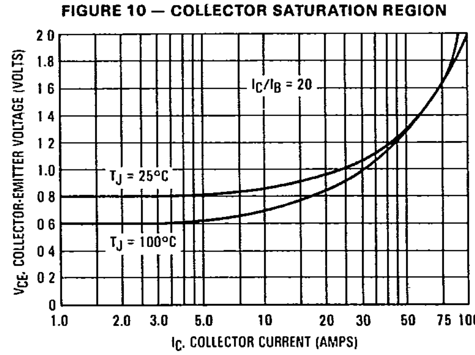

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FIGURE 11 — DC CURRENT GAIN

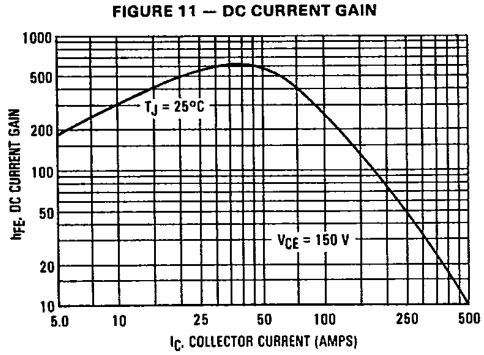
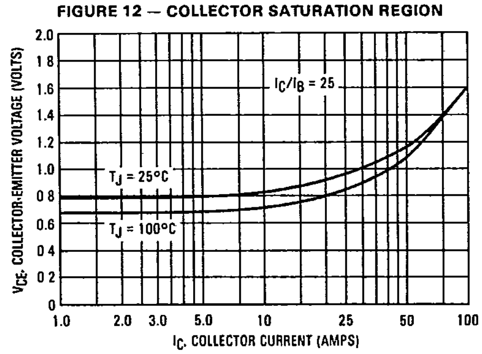


FIGURE 12 — COLLECTOR SATURATION REGION



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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 13 — BASE-EMITTER SATURATION VOLTAGE

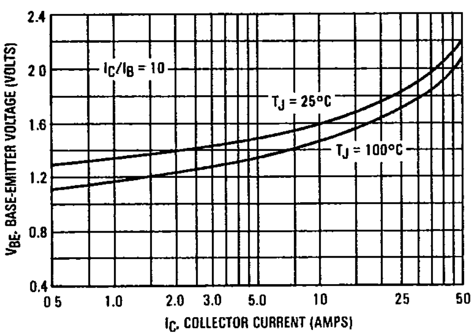
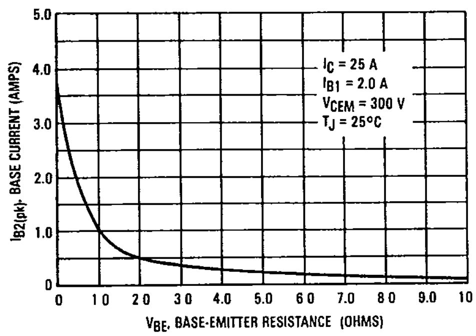


FIGURE 14 — TYPICAL PEAK REVERSE BASE CURRENT



MJ10045

FIGURE 15 — BASE-EMITTER SATURATION VOLTAGE

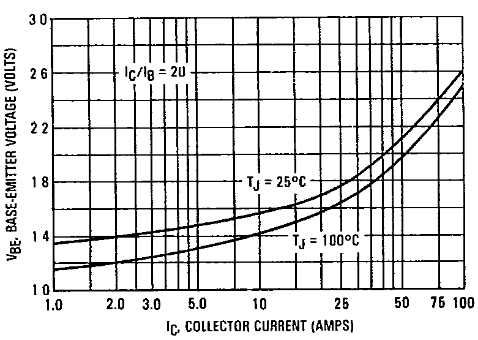
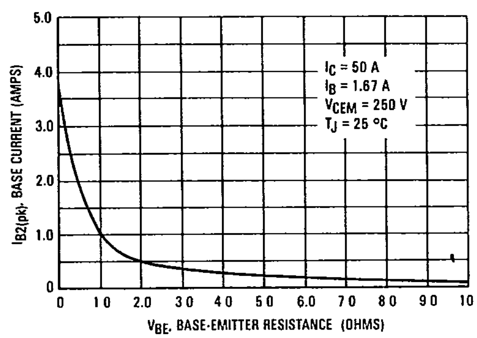


FIGURE 16 — TYPICAL PEAK REVERSE BASE CURRENT



MJ10048

FIGURE 17 — BASE-EMITTER SATURATION VOLTAGE

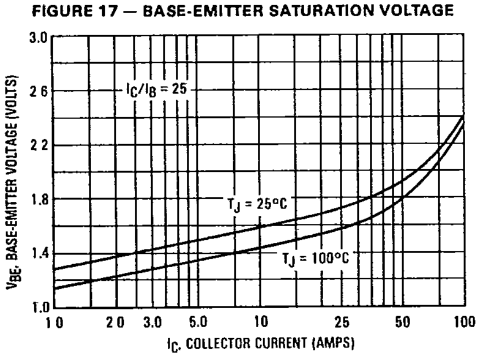
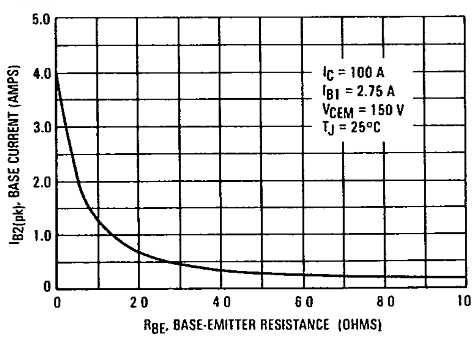


FIGURE 18 — TYPICAL PEAK REVERSE BASE CURRENT



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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 19 — TYPICAL INDUCTIVE SWITCHING TIMES

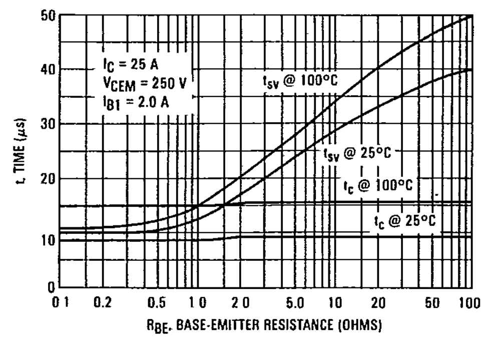
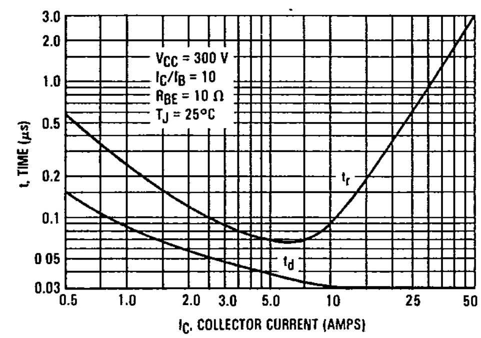


FIGURE 20 — TYPICAL TURN-ON SWITCHING TIMES



MJ10045

FIGURE 21 — TYPICAL INDUCTIVE SWITCHING TIMES

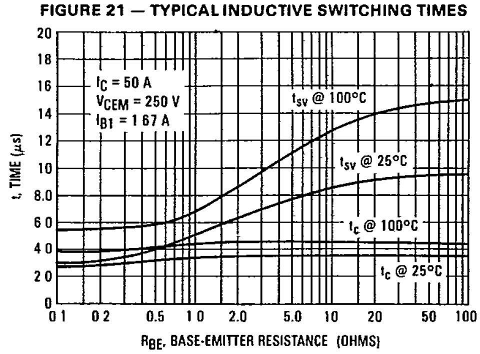
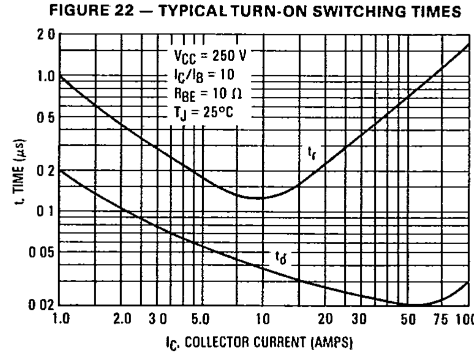


FIGURE 22 — TYPICAL TURN-ON SWITCHING TIMES



MJ10048

FIGURE 23 — TYPICAL INDUCTIVE SWITCHING TIMES

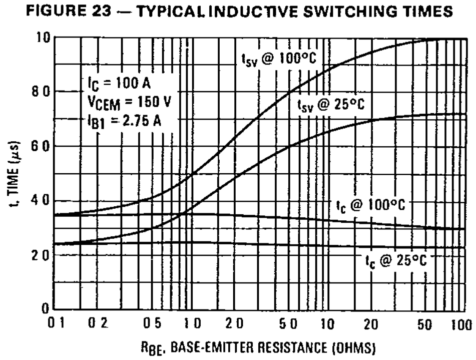
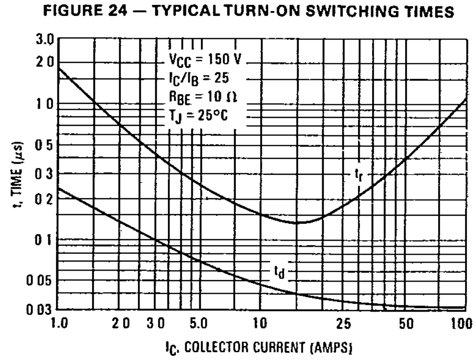


FIGURE 24 — TYPICAL TURN-ON SWITCHING TIMES



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TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 25 — TYPICAL TURN-OFF SWITCHING TIMES MJ10042

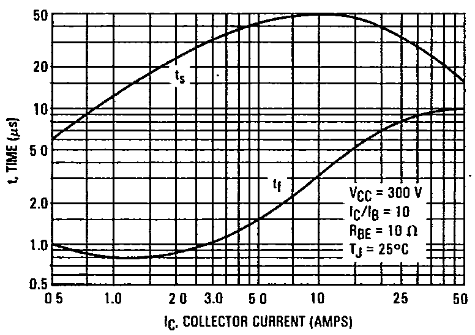

FIGURE 26 — EMITTER-COLLECTOR DIODE FORWARD VOLTAGE

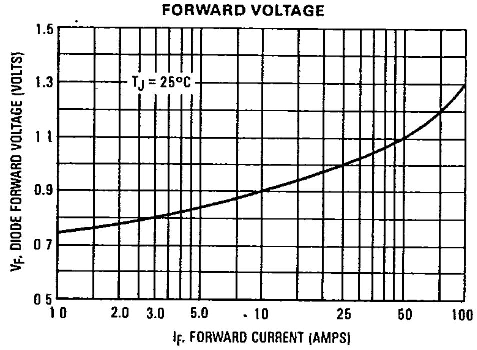

FIGURE 27 — TYPICAL TURN-OFF SWITCHING TIMES MJ10045

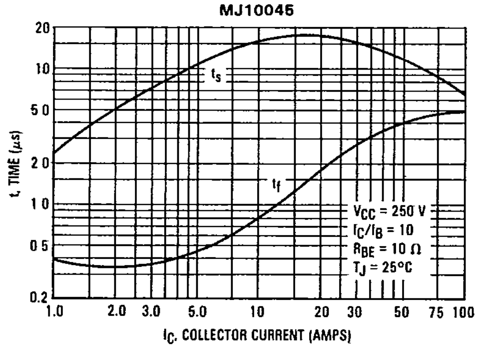

FIGURE 28 — POWER DERATING

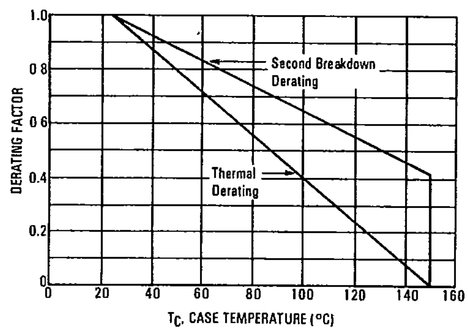

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FIGURE 29 — TYPICAL TURN-OFF SWITCHING TIMES MJ10048

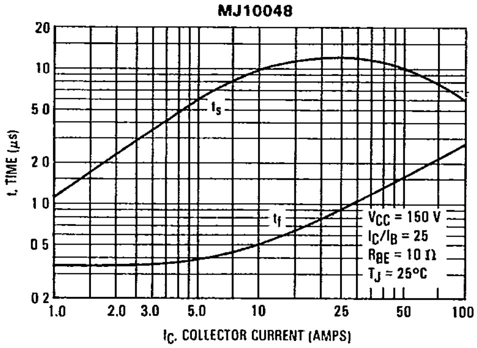
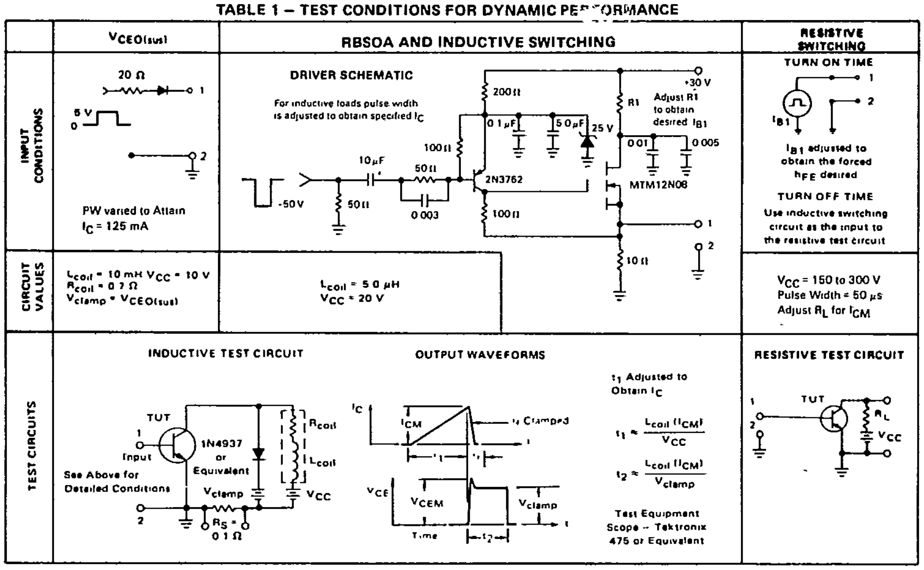


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust — V such that $V_{BE(off)}$ = 5.0 V except as required for RBSOA

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{CEM}
t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
t_{fi} = Current Fall Time, 90—10% I_{CM}
t_{ti} = Current Tail, 10—2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 30 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 30 — INDUCTIVE SWITCHING MEASUREMENTS

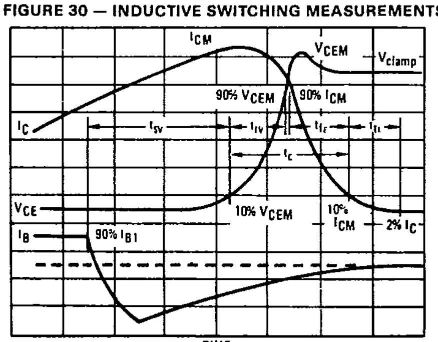
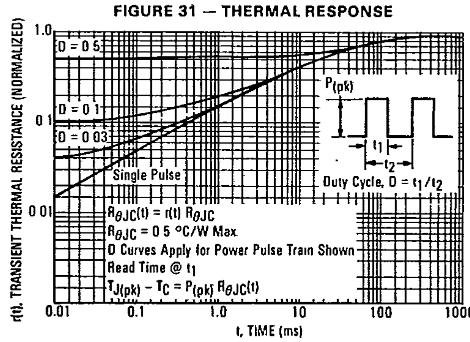


FIGURE 31 — THERMAL RESPONSE



T-33-35

SAFE OPERATING AREA INFORMATION

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FIGURE 32 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

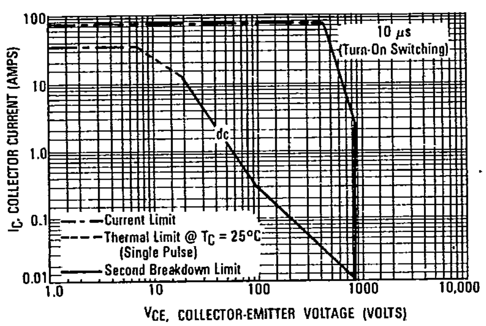
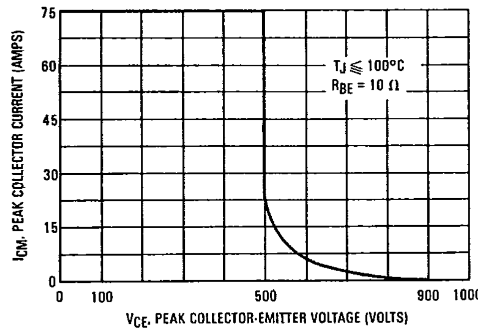


FIGURE 33 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10045

FIGURE 34 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

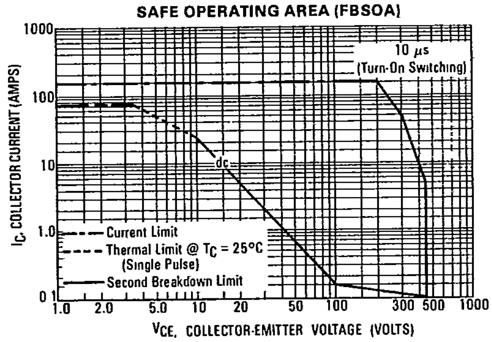


FIGURE 35 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)

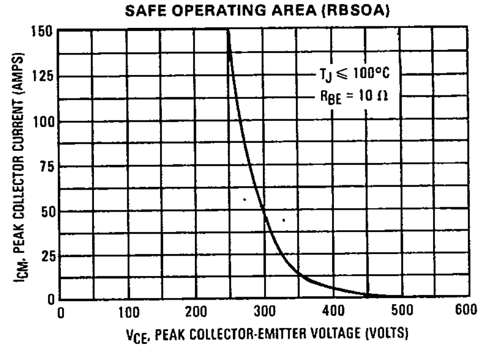


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FIGURE 36 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

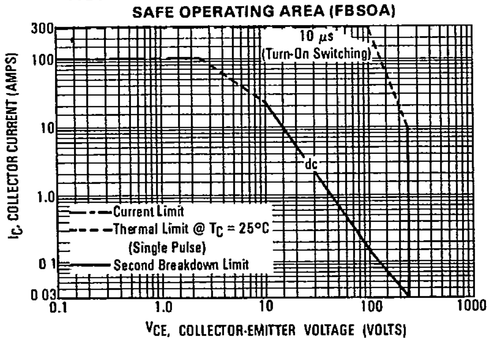
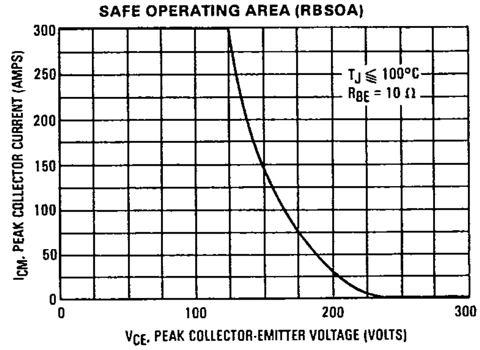


FIGURE 37 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



3

OVERLOAD CHARACTERISTICS

MJ10042

FIGURE 38 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

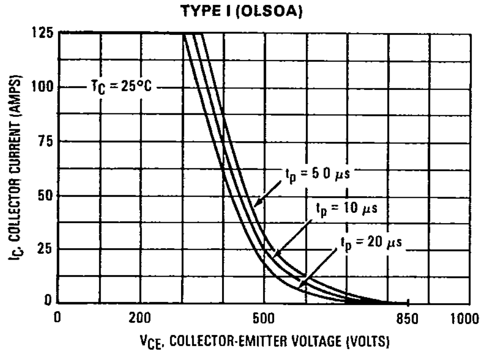


FIGURE 39 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)

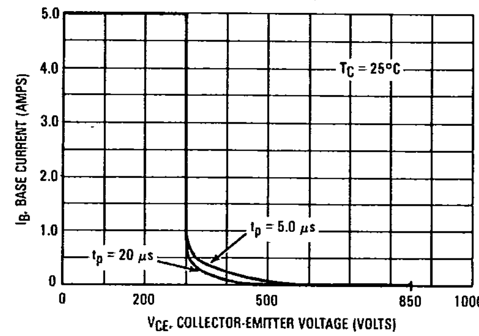


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FIGURE 40 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

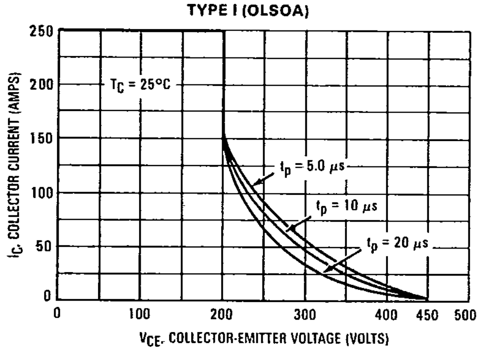

FIGURE 41 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)

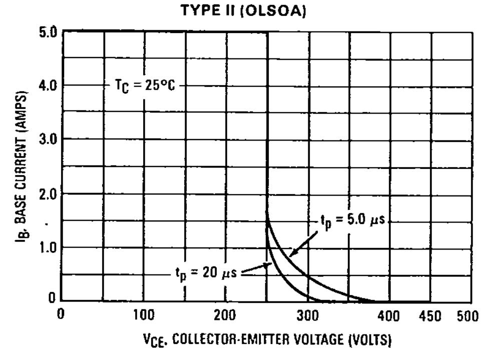

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FIGURE 42 — OVERLOAD SAFE OPERATING AREA TYPE I (OLSOA)

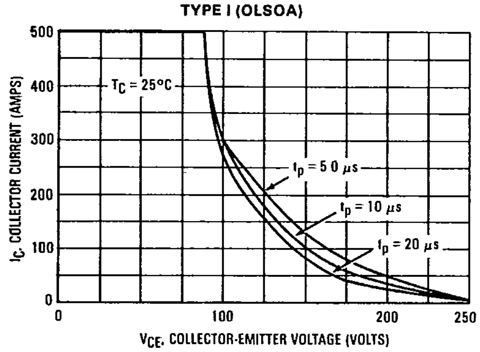
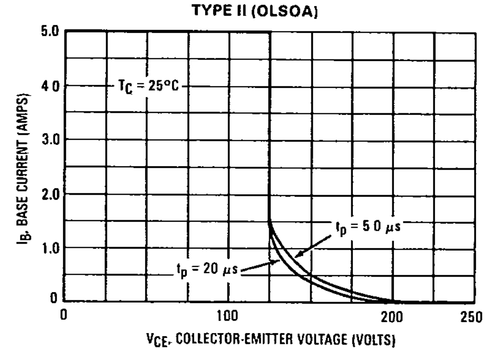


FIGURE 43 — OVERLOAD SAFE OPERATING AREA TYPE II (OLSOA)



3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 32, 34 and 36 are based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on these figures may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figure 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figures 33, 35 and 37 give the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in these figures adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figures 38, 40 and 42 depict the Type I OLSOA rating for these devices. Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, these figures define the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 44) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figures 39, 41 and 43 are measured in the circuit shown in Figure 45, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

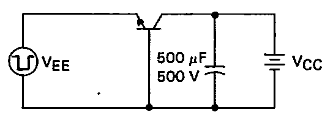
There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NON-REPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for these devices is 100 occurrences. Another factor is the form of turn-off bias. For these devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from I_{B2} = 0 (soft) to $V_{BE(off)}$ = 5 V (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

3

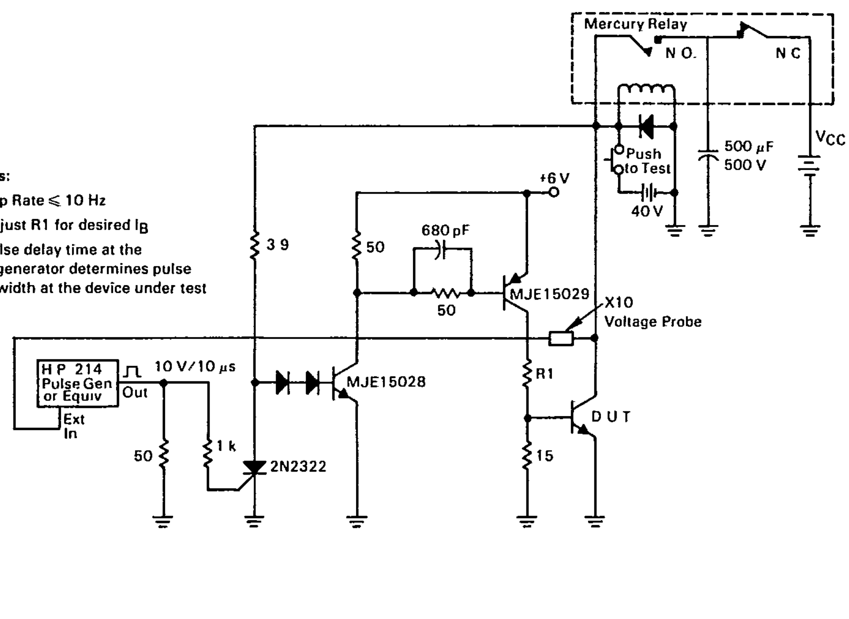
OVERLOAD SAFE OPERATING TEST CIRCUITS

FIGURE 44 — OVERLOAD SOA TEST CIRCUIT TYPE I (OLSOA)



Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

FIGURE 45 — OVERLOAD SOA TEST CIRCUIT TYPE II (OLSOA)



Notes:
- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test