

# MOSPEC

## SWITCHMODE SERIES NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16008 is a selected high-gain version of the MJ16006 for applications where drive current is limited

**Typical Applications:**

- \* Switching Regulators
- \* Inverters
- \* Solenoid and Relay Drives
- \* Motor Controls
- \* Deflection Circuits

**Features:**

- \* Fast Turn-Off Times
- \* Operating Temperature Range - 65 to +200°C
- \* 100°C Performance Specified for:
  - Reverse-Biased SOA With Inductive Loads
  - Switching Times With Inductive Loads
  - Saturation Voltages
  - Leakage Currents

### MAXIMUM RATINGS

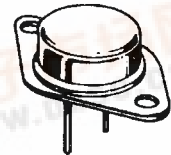
Characteristic	Symbol	MJ16002	MJ16004	Unit
Collector-Emitter Voltage	$V_{CEO}$	450	450	V
Collector-Emitter Voltage	$V_{CEV}$	850	850	V
Emitter-Base Voltage	$V_{EBO}$	6.0		V
Collector Current - Continuous - Peak	$I_C$ $I_{CM}$	5.0 10		A
Base Current-Continuous -Peak	$I_B$ $I_{BM}$	4.0 6.0		A
Total Power Dissipation @ $T_C=25^\circ C$ @ $T_C=100^\circ C$ Derate above 25°C	$P_D$	125 71.5 0.714		W W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{STG}$	-65 to +200		°C

### THERMAL CHARACTERISTICS

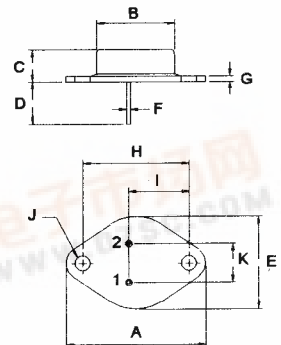
Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	1.4	°C/W

**NPN  
MJ16002  
MJ16004**

**5 AMPERE  
SILICON POWER  
TRANSISTORS  
450 VOLTS  
125 WATTS**



**TO-3**



PIN 1. BASE  
2. EMITTER  
COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	38.75	39.96
B	19.28	22.23
C	7.96	9.28
D	11.18	12.19
E	25.20	26.67
F	0.92	1.09
G	1.38	1.62
H	29.90	30.40
I	16.64	17.30
J	3.88	4.36
K	10.67	11.18

**ELECTRICAL CHARACTERISTICS (  $T_c = 25^\circ\text{C}$  unless otherwise noted )**

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Collector-Emitter Sustaining Voltage(1) ( $I_c = 100\text{ mA}, I_B = 0$ )	$V_{CEO(sus)}$	450		V
Collector Cutoff Current ( $V_{CE} = 850\text{ V}, V_{BE(off)} = 1.5\text{ V}$ ) ( $V_{CE} = 850\text{ V}, V_{BE(off)} = 1.5\text{ V}, T_c = 100^\circ\text{C}$ )	$I_{CEV}$		0.25 1.5	mA
Collector Cutoff Current ( $V_{CE} = 850\text{ V}, R_{BE} = 50\Omega, T_c = 100^\circ\text{C}$ )	$I_{CER}$		2.5	mA
Emitter Cutoff Current ( $V_{EB} = 6.0\text{ V}, I_c = 0$ )	$I_{EBO}$		1.0	mA

**ON CHARACTERISTICS (1)**

DC Current Gain ( $I_c = 5.0\text{ A}, V_{CE} = 5.0\text{ V}$ )	MJ16002 MJ16004	$h_{FE}$	5.0 7.0	
Collector-Emitter Saturation Voltage ( $I_c = 1.5\text{ A}, I_B = 0.2\text{ A}$ ) ( $I_c = 1.5\text{ A}, I_B = 0.15\text{ A}$ ) ( $I_c = 3.0\text{ A}, I_B = 0.4\text{ A}$ ) ( $I_c = 3.0\text{ A}, I_B = 0.3\text{ A}$ )	MJ16002 MJ16004 MJ16002 MJ16004	$V_{CE(sat)}$	1.0 1.0 2.5 2.5	V
Base-Emitter Saturation Voltage ( $I_c = 3.0\text{ A}, I_B = 0.4\text{ A}$ ) ( $I_c = 3.0\text{ A}, I_B = 0.3\text{ A}$ )	MJ16002 MJ16004	$V_{BE(sat)}$	1.5 1.5	V

**DYNAMIC CHARACTERISTICS**

Output Capacitance ( $V_{CB} = 10\text{ V}, I_E = 0, f = 1.0\text{ KHz}$ )	$C_{ob}$		250	pF
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**SWITCHING CHARACTERISTICS**

Delay Time	$V_{CC} = 250\text{ V}, I_c = 3\text{ A}$	$I_{B1} = -I_{B2} = 0.8\text{ A}$ MJ16002	$t_d$	100	ns
Rise Time	$R_{BE} = 8.0\Omega$		$t_r$	300	ns
Storage Time	$P_W = 30\text{ us}$	$I_{B1} = -I_{B2} = 0.6\text{ A}$ MJ16004	$t_s$	3000	ns
Fall Time	Duty Cycle $\leq 2.0\%$		$t_f$	350	ns

(1) Pulse Test: Pulse Width  $\leq 300\text{ us}$ , Duty Cycle  $\leq 2\%$

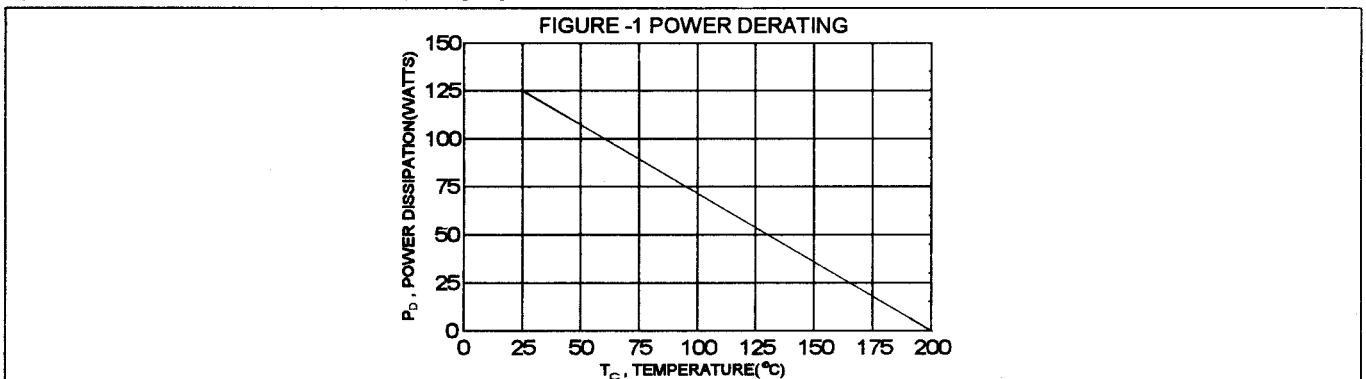


FIG-2 DC CURRENT GAIN

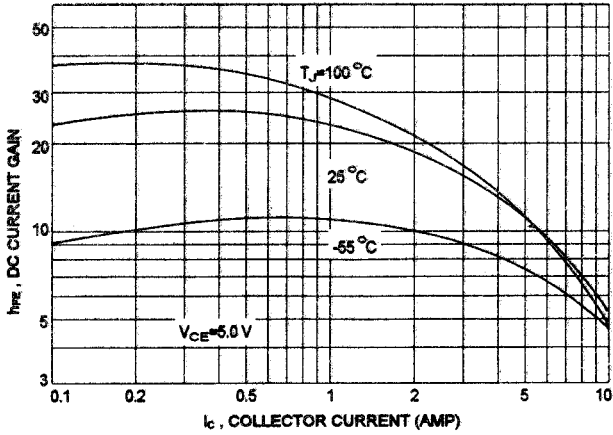


FIG-3 COLLECTOR SATURATION REGION

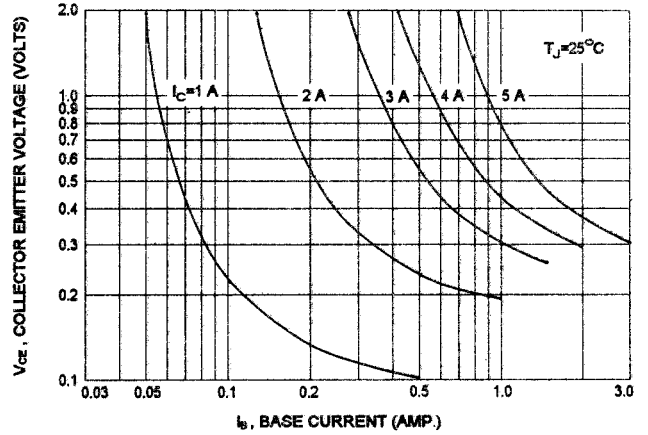


FIG-4 COLLECTOR-EMITTER SATURATION VOLTAGE

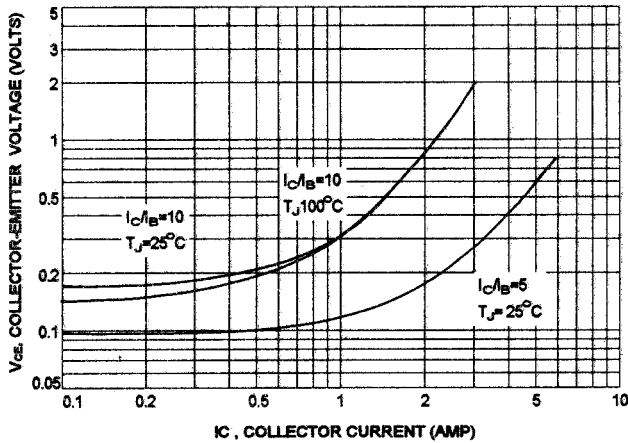


FIG-5 BASE-EMITTER SATURATION VOLTAGE

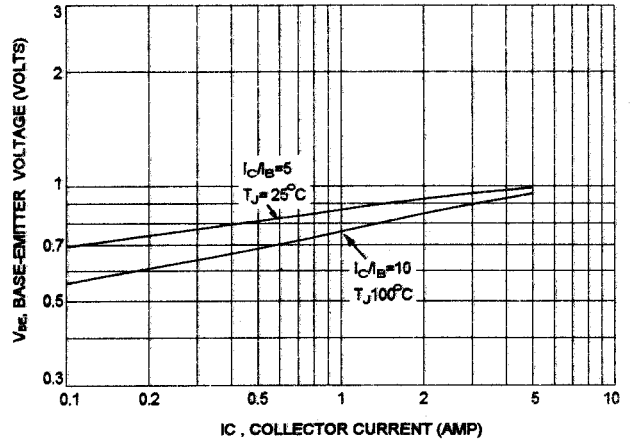


FIG-6 COLLECTOR CUT-OFF REGION

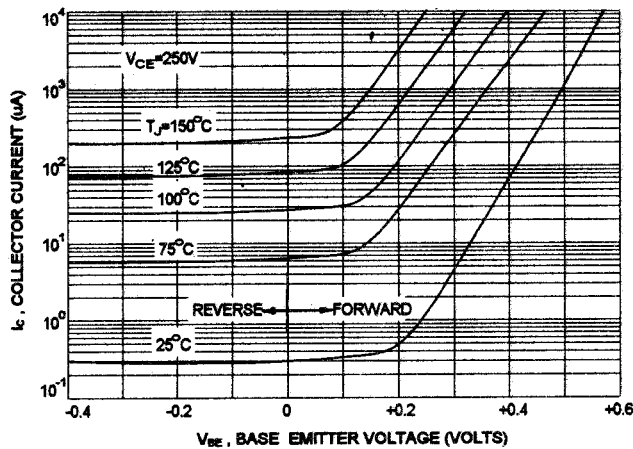


FIG-7 CAPACITANCES

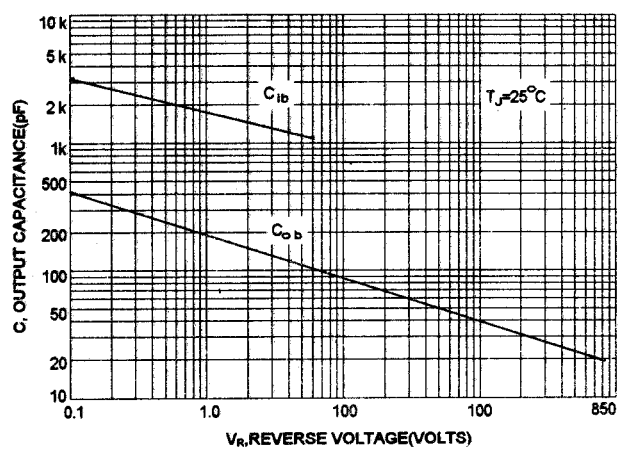
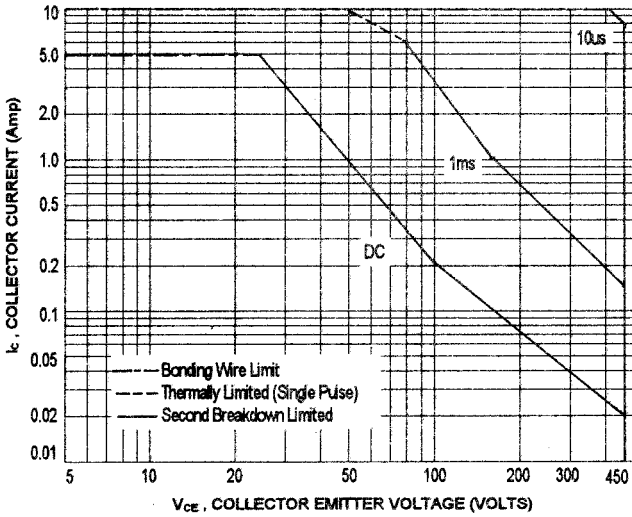


FIG-8 FORWARD BIAS SAFE OPERATING AREA

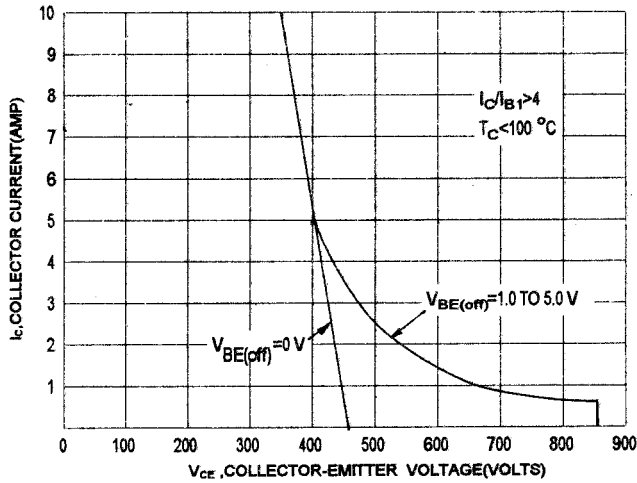


FORWARD BIAS

There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of FIG-8 is base on  $T_{J(PK)}=200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIG-9 REVERSE BIAS SAFE OPERATING AREA



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. FIG-9 gives the RBSOA characteristics.