Plastic Power Transistor

DPAK For Surface Mount Applications

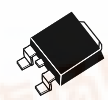
MJD243*

*Motorola Preferred Device

**NPN SILICON
POWER TRANSISTOR
4 AMPERES
100 VOLTS
12.5 WATTS**

. . . designed for low voltage, low–power, high–gain audio amplifier applications.

- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 100 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE} = 40 (Min) @ I_C = 200 mAdc
  = 15 (Min) @ I_C = 1.0 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“–1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.6 Vdc (Max) @ I_C = 1.0 Adc
- High Current–Gain — Bandwidth Product — f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage — I_{CBO} = 100 nAdc @ Rated V_{CB}



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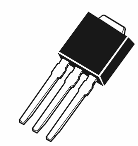


CASE 369–07

MAXIMUM RATINGS

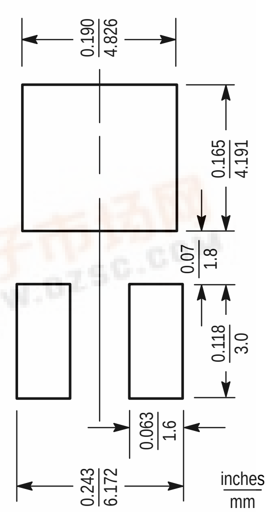
Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	100	Vdc
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Emitter–Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous Peak	I_C	4 8	Adc
Base Current	I_B	1	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	Watts W/°C
Total Device Dissipation @ T_A = 25°C* Derate above 25°C	P_D	1.4 0.011	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Junction to Ambient*	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

* When surface mounted on minimum pad sizes recommended.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



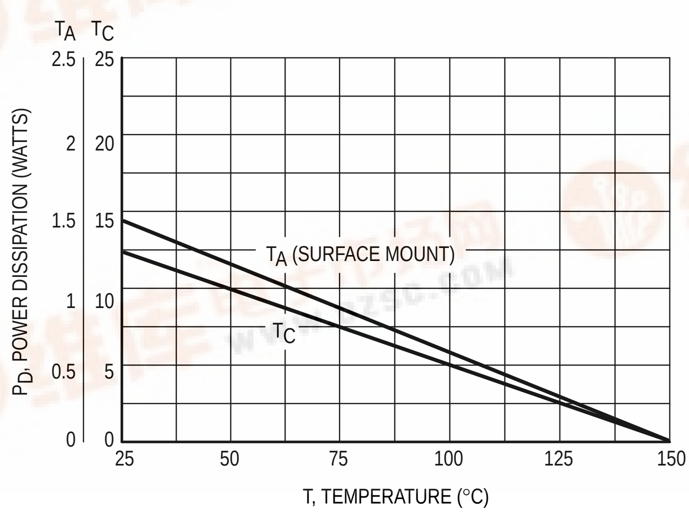


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	— —	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	—	100	nAdc
DC Current Gain (1) (I_C = 200 mAdc, V_{CE} = 1 Vdc) (I_C = 1 Adc, V_{CE} = 1 Vdc)	h_{FE}	40 15	180 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	 — —	 0.3 0.6	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 2 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	—	1.8	Vdc
Base–Emitter On Voltage (1) (I_C = 500 mAdc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	40	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	50	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
(2) $f_T = |h_{FE}| \bullet f_{test}$.

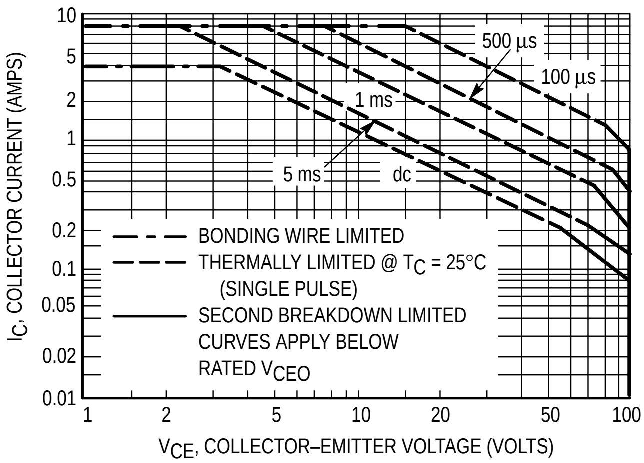


Figure 2. Active Region Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

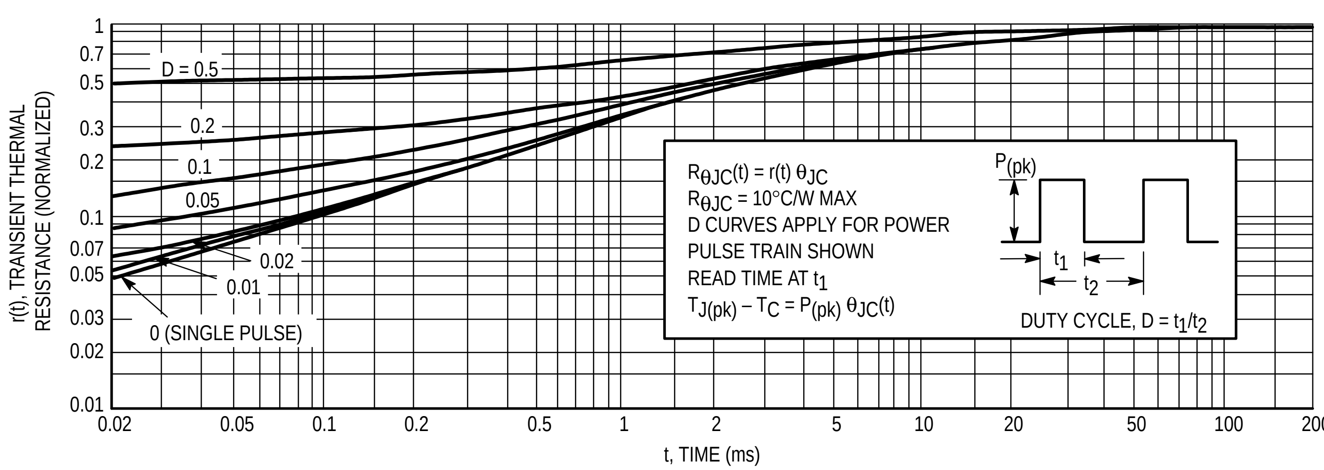


Figure 3. Thermal Response

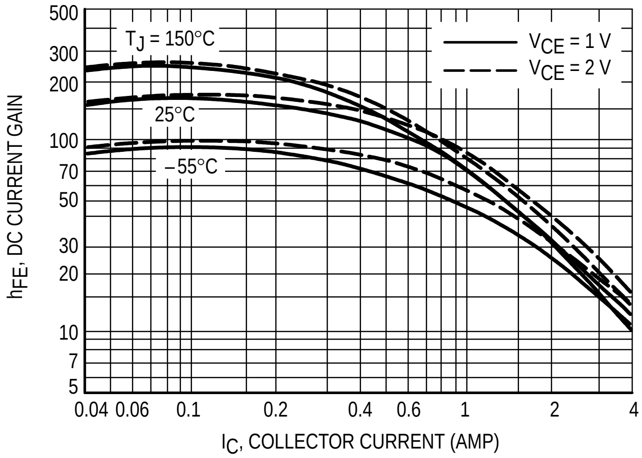


Figure 4. DC Current Gain

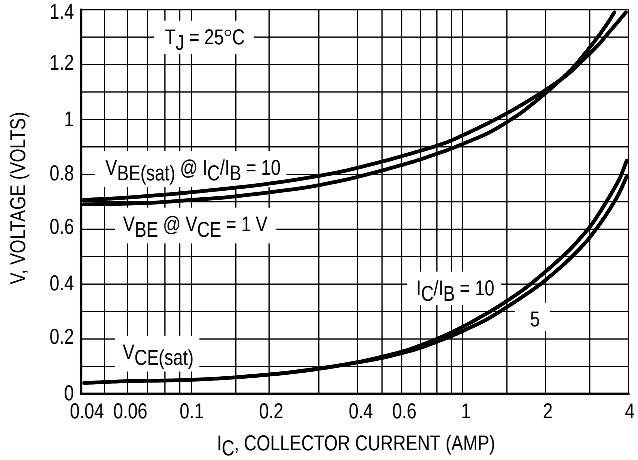


Figure 5. “On” Voltages

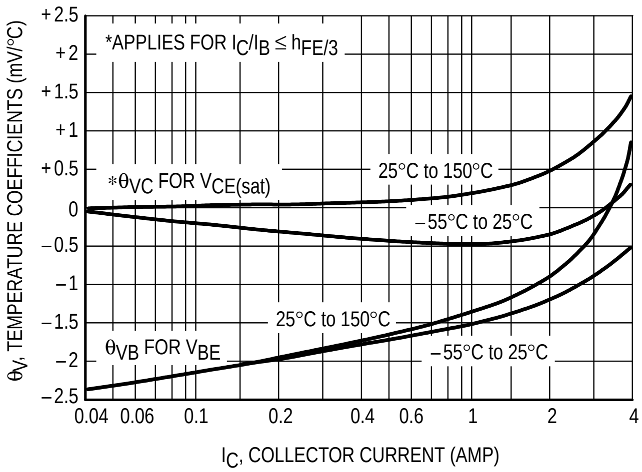


Figure 6. Temperature Coefficients

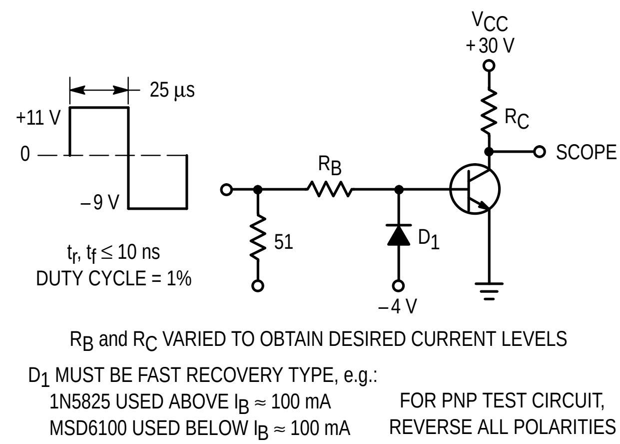


Figure 7. Switching Time Test Circuit

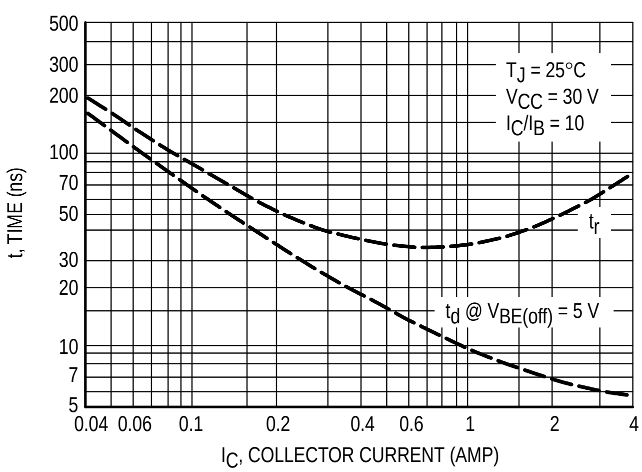


Figure 8. Turn–On Time

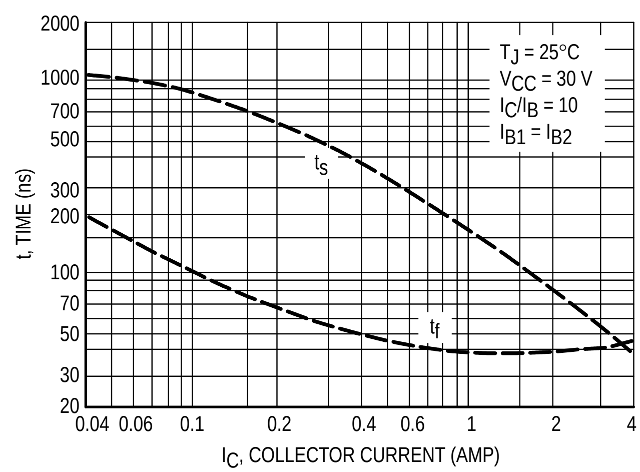


Figure 9. Turn–Off Time

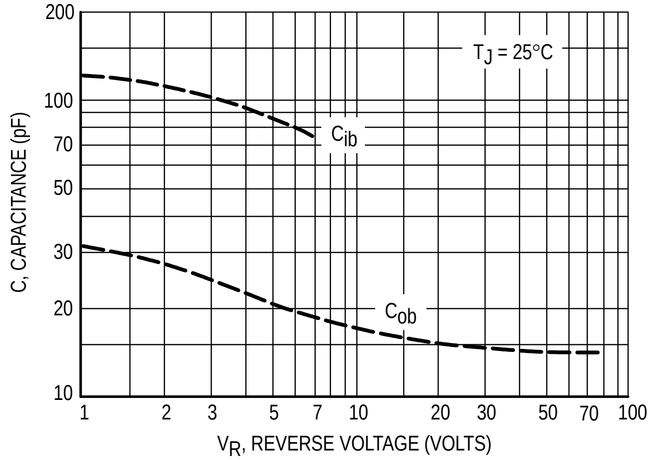
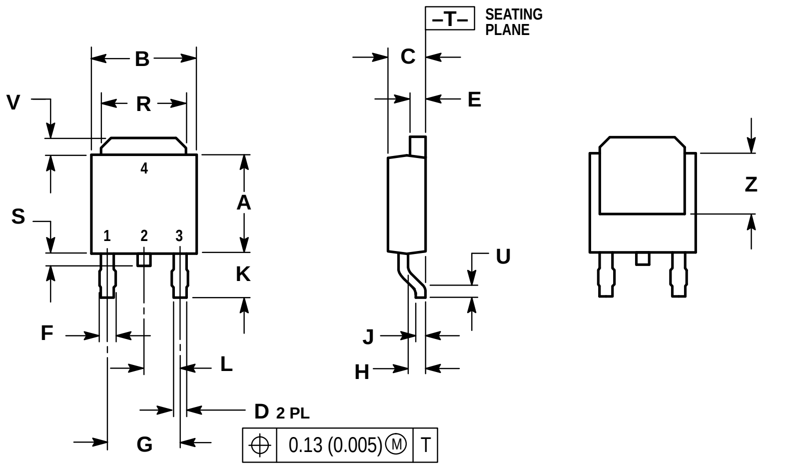


Figure 10. Capacitance

PACKAGE DIMENSIONS

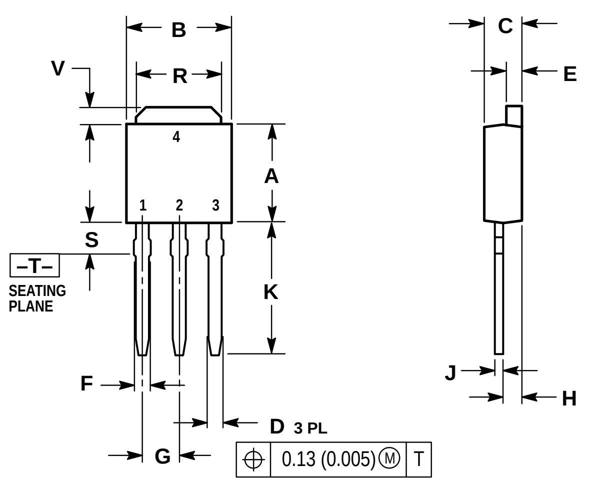


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 369A–13
ISSUE W



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E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 369–07
ISSUE K

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