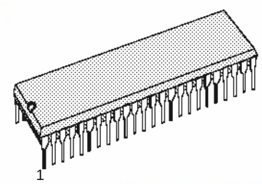
SGS-THOMSON MICROELECTRONICS

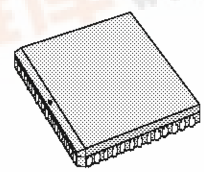
MK68564

SERIAL INPUT OUTPUT

- COMPATIBLE WITH MK68000 CPU
- COMPATIBLE WITH MK68000 SERIES DMA's
- TWO INDEPENDENT FULL-DUPLEX CHANNELS
- TWO INDEPENDENT BAUD-RATE GENERATORS
  - Crystal oscillator input
  - Single-phase TTL clock input
- DIRECTLY ADDRESSABLE REGISTERS (all control registers are read/write)
- DATA RATE IN SYNCHRONOUS OR ASYNCHRONOUS MODES
  - 0-1.25M bits/second with 5.0MHz system clock rate
- SELF-TEST CAPABILITY
- RECEIVE DATA REGISTERS ARE QUADRUPLY BUFFERED ; TRANSMIT REGISTERS ARE DOUBLY BUFFERED
- DAISY-CHAIN PRIORITY INTERRUPT LOGIC PROVIDES AUTOMATIC INTERRUPT VECTORING WITHOUT EXTERNAL LOGIC
- MODEM STATUS CAN BE MONITORED
  - Separate modem controls for each channel
- ASYNCHRONOUS FEATURES
  - 5, 6, 7, or 8 bits/character
  - 1, 1 1/2, or 2 stop bits
  - Even, odd, or no parity
  - x1, x16, x32, and x64 clock modes
  - Break generation and detection
  - Parity, overrun, and framing error detection
- BYTE SYNCHRONOUS FEATURES
  - Internal or external character synchronization
  - One or two sync characters in separate registers
  - Automatic sync character insertion
  - CDC-16 or CRC-CCITT block check generation and checking
- BIT SYNCHRONOUS FEATURES
  - Abort sequence generation and detection
  - Automatic zero insertion and deletion
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - Valid receive messages protected from overrun
  - CRC-16 or CRC-CCITT block check generation and checking



PDIP48
(Plastic Package)



PLCC52
(Chip Carrier)

DESCRIPTION

The MK68564 SIO (Serial Input Output) is a dual-channel, multi-function peripheral circuit, designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller ; however within that role, it is systems software configurable so that its "personality" may be optimized for any given serial data communications application.

The MK68564 is capable of handling asynchronous protocols, synchronous byte-oriented protocols (such as IBM Bisync), and synchronous bit-oriented protocols (such as HDLC and IBM SDLC). This versatile device can also be used to support virtually any serial protocol for applications other than data communications (cassette or floppy disk interface, for example).

The MK68564 can generate and check CRC codes in any synchronous mode and may be programmed to check data integrity in various modes. The device also has facilities for modem controls in each channel. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O.

SIO PIN DESCRIPTION

GND :	Ground
V_{CC}:	+ 5 Volts (± 5%)
$\overline{CS}$:	Chip Select (input, active low). $\overline{CS}$ is used to select the MK68564 SIO for accesses to the internal registers. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.
R/$\overline{W}$:	Read/write (input). R/$\overline{W}$ is the signal from the bus master, indicating wether the current bus cycle is a Read (high) or Write (low) cycle.
$\overline{DTACK}$:	Data Transfer Acknowledge (output, active low, three stateable). $\overline{DTACK}$ is used to signal the bus master that data is ready or that data has been accepted by the MK68564 SIO.
A1-A5 :	Address Bus (inputs). The address bus is used to select one of the internal registers during a read or write cycle.
D0-D7	Data Bus (bidirectional, threee-stateable). The data bus is used to transfer data to or from the internal registers during a read or write cycle. It is also used to pass a vector during an interrupt acknowledge cycle.
CLK :	Clock (input). This input is used to provide the internal timing for the MK68564 SIO.
$\overline{RESET}$:	Device Reset (input, active low). $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB to a marking condition, forces the modem controls high and disables all interrupts. With the exception of the status registers, data registers, and the vector register, all internal registers are cleared. The vector register is reset to ”0FH”.
$\overline{INTR}$:	Interrupt Request (output, active low, open drain). $\overline{INTR}$ is asserted when the MK68564 SIO is requesting an interrupt. $\overline{INTR}$ is negated during an interrupt acknowledge cycle or by clearing the pending interrupt(s) through software.
$\overline{IACK}$:	Interrupt acknowledge (input, active low). $\overline{IACK}$ is used to signal the MK68564 SIO that the CPU is acknowledging an interrupt. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.
$\overline{IEI}$:	Interrupt Enable In (input, active low). $\overline{IEI}$ is used to signal the MK68564 SIO that no higher priority device is requesting interrupt service.
$\overline{IEO}$:	Interrupt Enable Out (output, active low). $\overline{IEO}$ is used to signal lower priority peripherals that neither the MK68564 SIO nor another higher priority peripheral is requesting interrupt service.
XTAL1, XTAL2 :	Baud Rate Generator inputs. A crystal may be connected between XTAL1 and XTAL2, or XTAL1 may be driven with a TTL level clock. When using a crystal, external capacitors must be connectd. When driving XTAL1 with a TTL level clock, XTAL2 must be allowed to float.
$\overline{RxRDYA}$, $\overline{RxRDYB}$:	Receiver Ready (outputs, active low). Programmable DMA output for the receiver. The RxRDY pins pulse low when a character is available in the receive buffer.
$\overline{TxRDYA}$, $\overline{TxRDYB}$:	Transmitter Ready (outputs, active low). Programmable DMA output for the transmitter. The TxRDY pins pulse low when the transmit buffer is empty.
$\overline{CTSA}$, $\overline{CTSB}$:	Clear to Send (inputs, active low). If Tx Auto Enables is selected, these inputs enable the transmitter of their respective channels. If Tx Auto Enables is not selected, these inputs may be used as general purpose input pins. The inputs are Scmit-trigger buffered to allow slow rise-time input signals.
$\overline{DCDA}$, $\overline{DCDB}$:	Data Carrier Detect (inputs, active low). If Rx Auto Enables is selected, these inputs enable the receiver of their respective channels. If Rx Auto Enables is not selected, these inputs may be used as general purpose input pins. The inputs are Schmit-trigger buffered to allow slow rise-time input signals.
RxDA, RxDB :	Receive Data (inputs, active high). Serial data input to the receiver.
TxDA, TxDB :	Transmit Data (outputs, active high). Serial data output of the transmitter.

SIO PIN DESCRIPTION (continued)

RxCA, RxCB :	Receiver Clocks (input/output). Programmable pin, receive clock input, or baud rate generator output. The inputs are Schmit-trigger buffered to allow slow rise-time input signals.
TxCA, TxCB :	Transmitter Clocks (input/output). Programmable pin, transmit clock input, or baud rate generator output. The inputs are Schmit-trigger buffered to allow slow rise-time input signals.
RTSA, RTSB :	Request to Send (outputs, active low). These outputs follow the inverted state programmed into the RTS bit. When the RTS bit is reset in the asynchronous mode, the output will not change until the character in the transmitter is completely shifted out. These pins may be used as general purpose outputs.
$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$:	Data Terminal Ready (outputs, Active low). These outputs follow the inverted state programmed into the DTR bit. These pins may also be used as general purpose outputs.
$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$:	Synchronization (input/output, active low). The $\overline{\text{SYNC}}$ pin is an output when Monosync, Bisync, or SDLC mode is programmed. It is asserted when a sync/flag character is detected by the receiver. The SYNC pin is a general purpose input in the Asynchronous mode and an input to the receiver in the External Sync Mode.

Figure 1a : Dual In Line Pin Configuration.

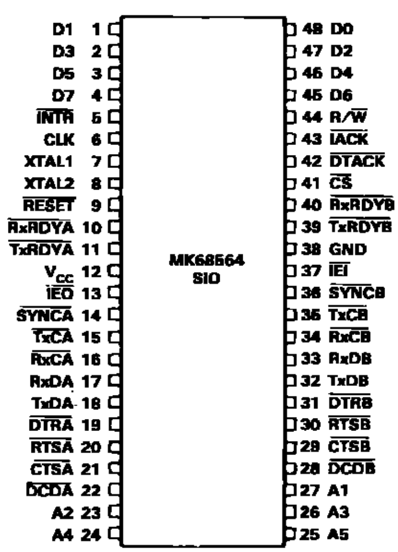
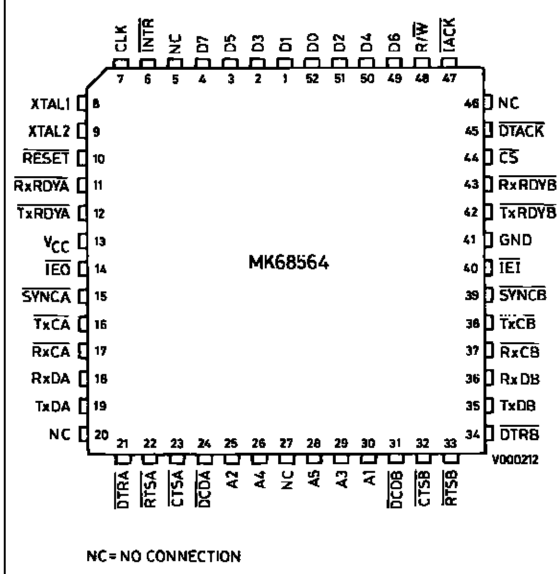


Figure 1b : Chip Carrier Pin Configuration.



SIO SYSTEM INTERFACE

INTRODUCTION

The MK68564 SIO is designed for simple and efficient interface to a MK68000 CPU system. All data transfers between the SIO and the CPU are asynchronous to the system clock. The SIO system timing is derived from the chip select input (CS) during normal read and write sequences, and from the interrupt acknowledge input (IACK) during an exception processing sequence. CS is a function of address decode and (normally) lower data strobe (LDS). IACK is a function of the interrupt level on address lines A1, A2, and A3, an interrupt acknowledge function code (FC0-FC2), and LDS.

Note : CS and IACK can never be asserted at the same time.

Note : Unused inputs should be pulled up or down, but never left floating.

READ SEQUENCE

The SIO will begin a read cycle if, on the falling edge of CS, the read-write (R/W) pin is high. The SIO will respond by decoding the address bus (A1-A5) for the register selected, by placing the contents of that register on the data bus pins (D0-D7), and by driving the data transfer acknowledge (DTACK) pin low. If the register selected is not implemented on the SIO, the data bus pins will be driven high, and then DTACK will be asserted. When the CPU has acquired the data, the CS signal is driven high, at which time the SIO will drive DTACK high and then three-state DTACK and D0-D7.

WRITE SEQUENCE

The SIO will begin a write cycle if, on the falling edge of CS, the R/W pin is low. The SIO will respond by latching the data bus, by decoding the address bus for the register selected, by loading the register with the contents of the data bus, and by driving DTACK low. When the CPU has finished the cycle, the CS input is driven high. At this time, the SIO will drive DTACK high and will then three-state DTACK. If the register selected is not implemented on the SIO, the normal write sequence will proceed, but the data bus contents will not be stored.

INTERRUPT SEQUENCE

The SIO is designed to operate as an independent, interrupting peripheral, or, when interconnected with other components, an interrupt priority daisy chain can be formed.

Independent Operation. Independent operation requires that the interrupt enable in pin (IEI) be connected to ground. The SIO starts the interrupt sequence by driving the interrupt request pin (INTR) low. The CPU responds to the interrupt by starting an interrupt acknowledge cycle, in which the SIO IACK pin is driven low. The highest priority interrupt request in the SIO, at the time IACK goes low, places its vector on the data bus pins. The SIO releases the INTR pin and drives DTACK low. When the CPU has acquired the vector, the IACK signal is driven high. The SIO responds by driving DTACK to a high level and then three-stating DTACK and D0-D7. If more than one interrupt request is pending at the start of an interrupt acknowledge sequence, the SIO will drive the INTR pin low following the completion of the interrupt acknowledge cycle. This sequence will continue until all pending interrupts are cleared. If the SIO is not requesting an interrupt when IACK goes low, the SIO will not respond to the IACK signal ; DTACK and the data bus will remain three-stated.

Daisy Chain Operation. The interrupt priority chain is formed by connecting the interrupt enable out pin (IEO) of a higher priority part to IEI of the next lower priority part. The highest priority part in the chain should have IEI tied to ground. The Daisy Chaining capability (figures 2 and 3) requires that all parts in a chain have a common IACK signal. When the common IACK goes low, all parts freeze and prioritize interrupts in parallel. Then priority is passed down the chain, via IEI and IEO, until a part which has a pending interrupt, once IEI goes low, passes a vector, does not propagate IEO, and generates DTACK.

The state of the IEI pin does not affect the SIO interrupt control logic. The SIO can generate an interrupt request any time its interrupts are enabled. The IEO pin is normally high ; it will only go low during an IACK cycle if IEI is low and no interrupt is pending in the SIO. The IEO pin will be forced high whenever IACK or IEI goes high.

Figure 2 : Conceptual Circuit of the MK68564 SIO Daisy Chaining Logic.

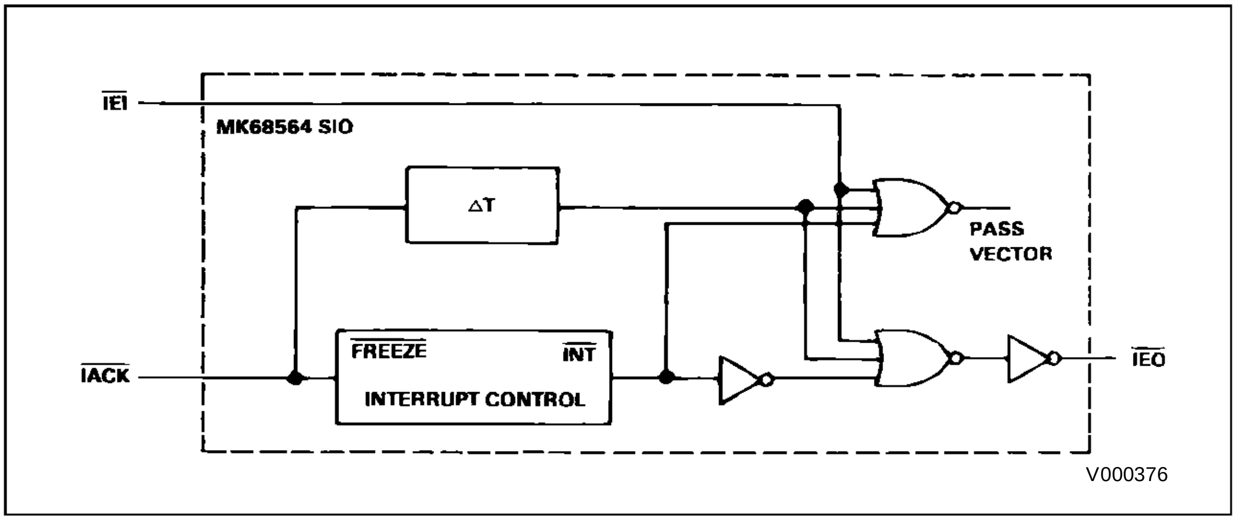


Figure 3 : Daisy Chaining.

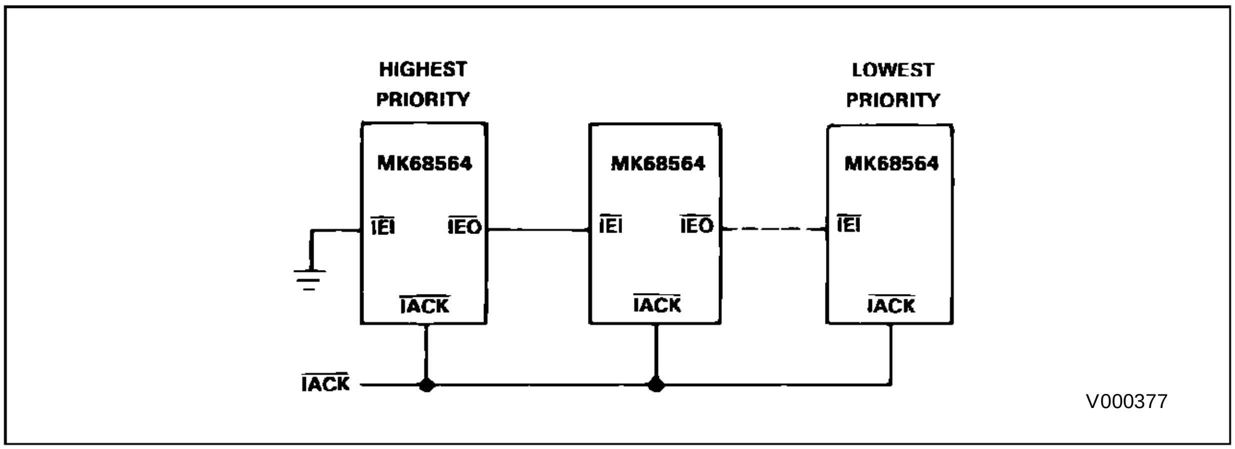
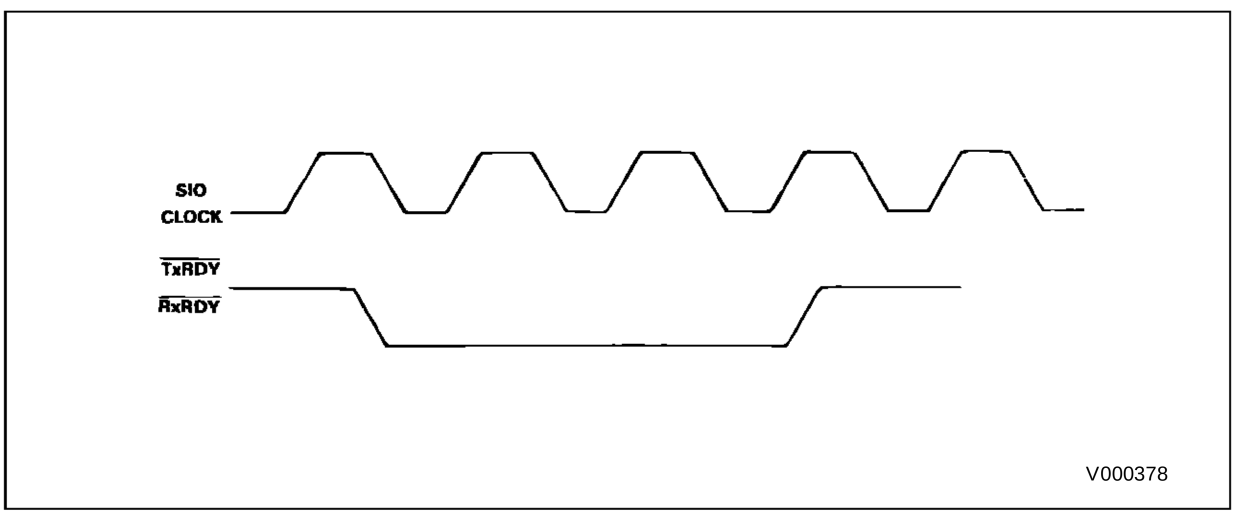


Figure 4 : DMA Interface Timing.



DMA INTERFACE

The SIO is designed to interface to the 68000 family DMA's as a 68000 compatible device, using the cycle steal mode. The SIO provides four outputs (TxRDYA, RxRDYA, TxRDYB, RxRDYB) for requesting service from the DMA. The SIO issues a request for service by pulsing the RDY pin low for three clock (CLK) cycles (see figure 4). TxRDY (when enabled) will be active when the transmit buffer becomes empty. RxRDY (when enabled) will be active when a character is available in the receive buffer. If Receive Interrupt On First Character Only is enabled during a DMA operation and a special receive condition is detected, the RxRDY pin will not become active. Instead, a special receive condition interrupt will be generated by the channel.

RESET

There are two ways of resetting the SIO : an individual, programmable channel reset and an external hardware reset.

The individual channel reset is generated by writing "18H" to the Command Register for the channel selected. All outputs associated with the channel are reset high, TxC and RxC are inputs, SYNC is an output, and TxD is forced marking. All R/W registers for the channel are reset to "00H", except the vector register and the data register, which are not affected.

Read only status register 1 is reset to "01H" (All Sent set). Break/Abort, Interrupt Pending, and Rx Character Available bits in read only status register 0 are reset ; Underrun/EOM, Hunt/Sync, and Tx Buffer Empty are set ; CTS and DCD bits are set to the inverted state of their respective input pins. Any interrupts pending for the channel are reset (any pending interrupts in the other channel will not be affected).

An external hardware reset occurs when the RESET pin is driven low for at least one clock (CLK) cycle. Both channels are reset as listed above, and the vector register is reset to "0FH".

ARCHITECTURE

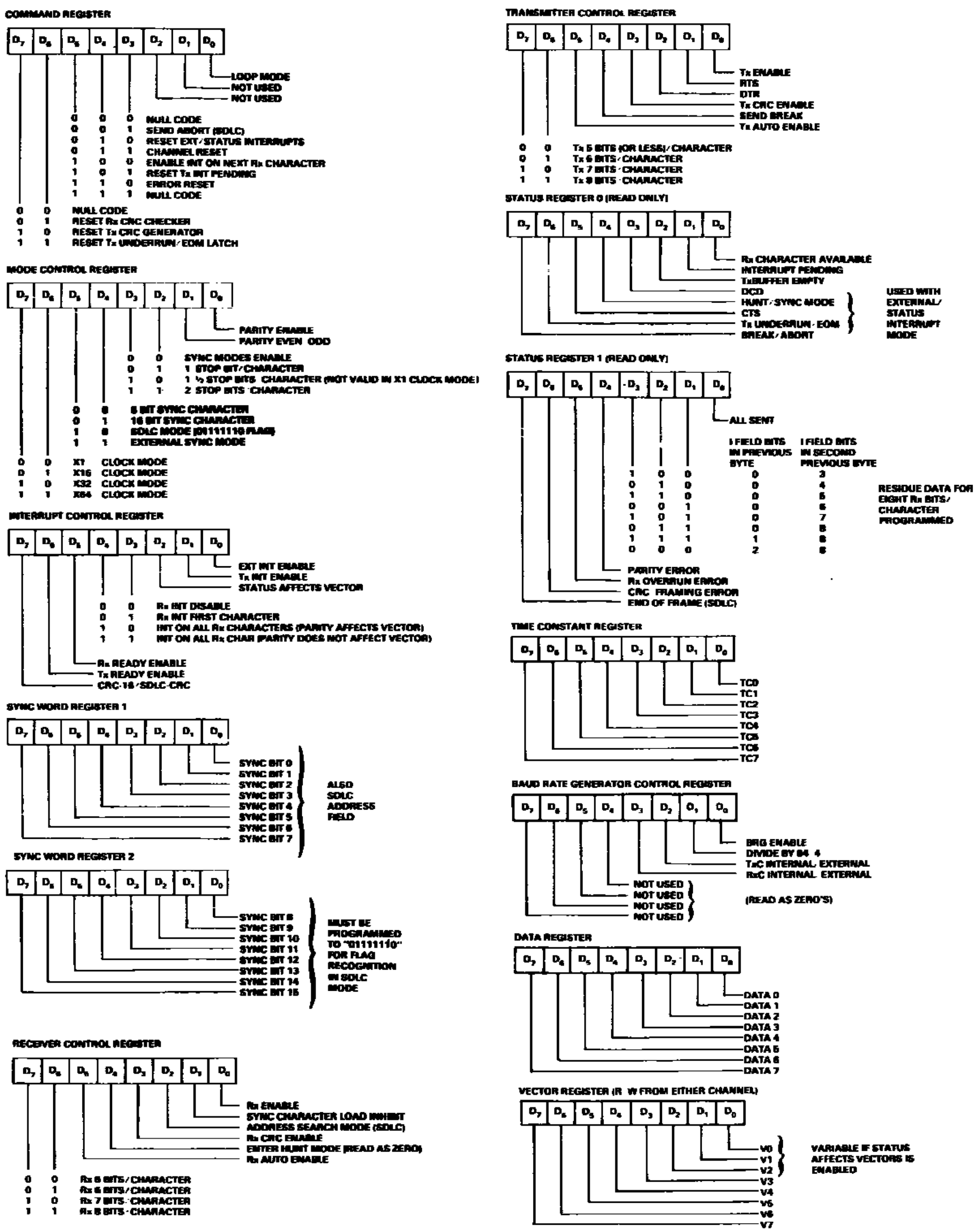
The MK68564 SIO contains two independent, full-duplex channels. Each channel contains a transmitter, receiver, modem control logic, interrupt control logic, a baud rate generator, ten Read/Write registers, and two read only status registers. Each channel can communicate with the bus master using polling, interrupts, DMA, or any combination of these three techniques. Each channel also has the ability to connect the transmitter output into the receiver without disturbing any external hardware.

Register Set. The register set is the heart of each channel. A channel is configured for different communication protocols and interface options by programming the registers. Table 1 lists all the registers available in the SIO and their addresses.

Data Register. The Data Register is composed of two separate registers : a write only register, which is the Transmit Buffer, and a read only register, which is the Receive Buffer. The Receive Buffer is also the top register of a three register stack called the receive data FIFO.

Vector Register. The Vector Register is different from the other 24 registers, because it may be accessed through either Channel A or Channel B during a R/W cycle. During an Interrupt Acknowledge cycle, the contents of the Vector Register are passed to the CPU to be used as a pointer to an interrupt service routine. If the Status Affects Vector bit is Low in the Interrupt Control Register, any data written to the Vector Register will be returned unmodified during a Read Cycle or an IACK cycle. If the Status Affects Vector bit is High, the lower three bits of the vector returned during a Read or IACK cycle are modified to reflect the highest priority interrupt pending in the SIO at that time. The upper five bits written to the Vector Register are unaffected. After a hardware reset only, this register contains a "0FH" value, which is the MK68000's uninitialized interrupt vector assignment.

Figure 5 : Register Bit Functions.



SIO INTERNAL REGISTERS

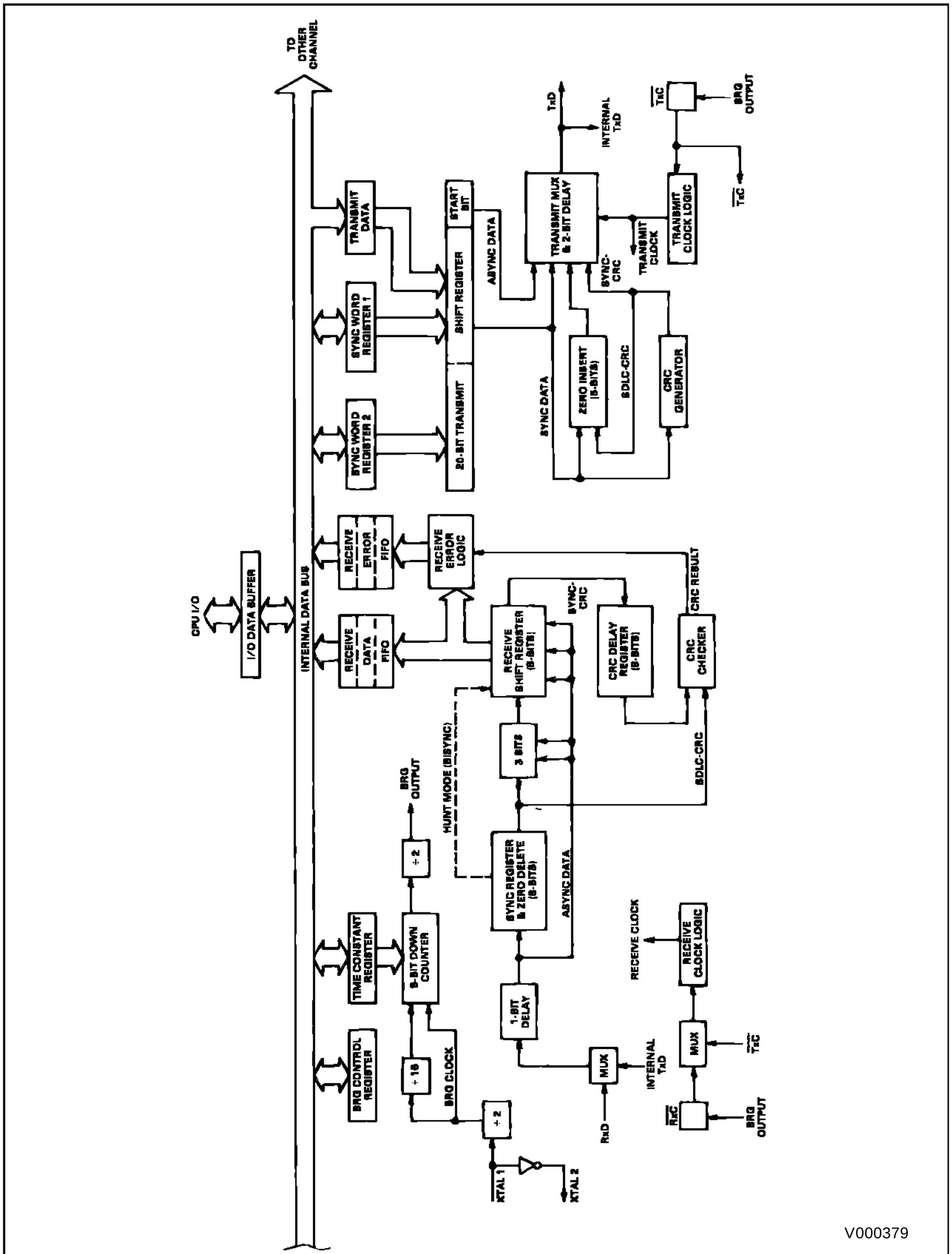
The MK68564 SIO has 25 internal registers. Each channel has ten R/W registers and two read only registers associated with it. The vector register may be accessed through either channel.

Table 1 : Register Map**.**

Address					Abbreviation	Channel	Register Name	Access	
5	4	3	2	1				Read/ write	Read Only
0	0	0	0	0	CMDREG	A	Command Register	X	
0	0	0	0	1	MODECTL	A	Mode Control Register	X	
0	0	0	1	0	INTCTL	A	Interrupt Control Register	X	
0	0	0	1	1	SYNC 1	A	Sync Word Register 1	X	
0	0	1	0	0	SYNC 2	A	Sync Word Register 2	X	
0	0	1	0	1	RCVCTL	A	Receiver Control Register	X	
0	0	1	1	0	XMTCTL	A	Transmitter Control Register	X	
0	0	1	1	1	STAT 0	A	Status Register 0		X
0	1	0	0	0	STAT 1	A	Status Register 1		X
0	1	0	0	1	DATARG	A	Data Register	X	
0	1	0	1	0	TCREG	A	Time Constant Register	X	
0	1	0	1	1	BRGCTL	A	Baud Rate Generator Control Reg	X	
0	1	1	0	0	VECTRG	A/B	Interrupt Vector Register (note 2)	X	
0	1	1	0	1		A	(note 1)	X	
0	1	1	1	0		A	(note 1)	X	
0	1	1	1	1		A	(note 1)	X	
1	0	0	0	0	CMDREG	B	Command Register	X	
1	0	0	0	1	MODECTL	B	Mode Control Register	X	
1	0	0	1	0	INTCTL	B	Interrupt Control Register	X	
1	0	0	1	1	SYNC 1	B	Sync Word Register 1	X	
1	0	1	0	0	SYNC 2	B	Sync Word Register 2	X	
1	0	1	0	1	RCVCTL	B	Receiver Control Register	X	
1	0	1	1	0	XMTCTL	B	Transmitter Control Register	X	
1	0	1	1	1	STAT 0	B	Status Register 0		X
1	1	0	0	0	STAT 1	B	Status Register 1		X
1	1	0	0	1	DATARG	B	Data Register	X	
1	1	0	1	0	TCREG	B	Time Constant Register	X	
1	1	0	1	1	BRGCTL	B	Baud Rate Generator Control Reg	X	
1	1	1	0	0	VECTRG	A/B	Interrupt Vector Register (note 2)	X	
1	1	1	0	1		B	(note 1)	X	
1	1	1	1	0		B	(note 1)	X	
1	1	1	1	1		B	(note 1)	X	

Notes : 1. Not Used, Read as "FFH".
2. Only One Vector Register, Accessible through Either Channel.

Figure 6 : Transmit and Receive Data Paths.



DATA PATH

The transmit and receive data paths for each channel are shown in figure 6. The receiver has three 8-bit buffer registers in a FIFO arrangement (to provide a 3-byte delay) in addition to the 8-bit receive shift register. This arrangement creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. The receiver error FIFO stores parity and framing errors and other types of status information for each of the three bytes in the receive data FIFO. The receive error FIFO is loaded at the same time as the receive data FIFO. The contents of the receive error are read through the upper four bits in Status Register 1.

Incoming data is routed through one of several paths, depending on the mode and character length. In the Asynchronous modes, serial data is entered into the 3-bit buffer, if it has a character length of seven or eight bits, or the data is entered into the 8-bit receive shift register, if it has a length of five or six bits.

In the Synchronous mode, the data path is determined by the phase of the receive process currently in operation. A Synchronous Receive operation begins with the receiver in the Hunt phase, during which time the receiver searches the incoming data stream for a bit pattern that matches the preprogrammed sync characters (or flags in the SDLC mode). If the device is programmed for Monosync Hunt, a match is made with a single sync character stored in Sync Word Register 2. In Bisync Hunt, a match is made with the dual sync characters stored in Sync Word Registers 1 and 2. In either case, the incoming data passes through the receive sync register and is compared against the programmed sync characters in Sync Word Registers 1 and 2.

In the Monosync mode, a match between the sync character programmed into Sync Word Register 2 and the character assembled in the receive sync register establishes synchronization.

In the Bysync mode, incoming data is shifted to the receive shift register, while the next eight bits of the message are assembled in the receive sync register. The match between the assembled character in the sync register and the programmed character in Sync Word Register 2, and between the character in the shift register and the programmed character in Sync Word Register 1 establishes synchronization. Once synchronization is established, incoming data bypasses the receive sync register and directly enters the 3-bit buffer.

In the SDLC mode, all incoming data passes through the receive sync register, which continuously monitors the receive data stream and performs zero deletion when indicated. Upon receiving five contiguous ones, the sixth bit is inspected. If the sixth bit is a 0, it is deleted from the data stream. If the sixth bit is a 1, the seventh bit is inspected. If the seventh bit is a 0, a Flag sequence has been received ; if the seventh bit is a 1, an Abort sequence has been received.

The reformatted data from the receive sync register enters the 3-bit buffer and is transferred to the receive shift register. Note that the SDLC receive operation also begins in the Hunt Phase, during which time the SIO tries to match the assembled character in the receive sync register with the flag pattern in Sync Word Register 2. Once the first flag character is recognized, all subsequent data is routed through the path described above, regardless of character length.

Although the same CRC checker is used for both SDLC and synchronous data, the path taken for each mode is different. In Bisync protocol, the byte-oriented operation requires that the CPU decide whether or not to include the data character in the CRC calculation. To allow the CPU ample time to make this decision, the SIO provides an 8-bit delay before the data enters the CRC checker. In the SDLC mode, no delay is provided, since CRC is calculated on all data between the opening and closing flags.

The transmitter has an 8-bit transmit data register, which is loaded from the internal bus, and a 20-bit transmit shift register, which can be loaded from Sync Word Register 1, Sync Word Register 2, and the transmit data register. Sync Word Registers 1 and 2 contain sync characters in the Monosync, Bisync, or External Sync modes, or address field (one character long) and flag, respectively, in the SDLC mode. During Synchronous modes, information contained in Sync Word Registers 1 and 2 is loaded into the transmit shift register at the beginning of the message and, as a time filler, in the middle of the message if a Transmit Underrun condition occurs. In SDLC mode, the flags are loaded into the transmit shift register at the beginning and end of the message.

Asynchronous data in the transmit shift register is formatted with start and stop bits, and it is shifted out to the transmit multiplexer at the selected clock rate.

Synchronous (Monosync, Bisync, or External Sync) data is shifted out to the transmit multiplexer and also the CRC generator at the x1 clock rate.

SDLC/HDLC data is shifted out through the zero insertion logic, which is disabled while flags are being sent. For all other fields (address, control, and frame check), a 0 is inserted following five contiguous ones in the data stream. Note that the CRC generator result (frame check) for SDLC data is also routed through the zero insertion logic.

I/O CAPABILITIES

The SIO offers the choice of Polling, Interrupt (vectored or non-vectored), and DMA Transfer modes to transfer data, status, and control information to and from the CPU or other bus master.

Polling. The Polled mode avoids interrupts. Status Registers 0 and 1 are updated at appropriate times for each function being performed (for example, CRC Error status valid at the end of the message). All the interrupt modes of the SIO must be disabled to operate the device in a polled environment.

While in its Polling sequence, the CPU examines the status contained in Status Register 0 for each channel. The state of the status bits in Status Register 0 serves as an acknowledge to the Poll inquiry. Status bits D0 and D2 indicate that a receive or transmit data transfer is needed. The rest of the status bits in Status Register 0 indicate special status conditions. The receiver error condition bits in Status Register 1 do not have to be read until the Rx Character Available status bit in Status Register 0 is set to a one.

Interrupts. The SIO offers an elaborate interrupt scheme to provide fast interrupt response in real-time applications. The interrupt vector points to an interrupt service routine in the memory. To service operations in both channels and to eliminate the necessity of writing a status analysis routine (as required for a polling scheme), the SIO can modify the interrupt vector so it points to one of eight interrupt service routines. This is done under program control by setting the Status Affects Vector bit in the Interrupt Control Register of channel A or channel B, to a one. When this bit is set, the interrupt vector is modified according to the assigned priority of the various interrupting conditions.

Note : If the Status Affects Vector bit is set in either channel, the vector is modified for both channels. This is the only control bit that operates in this manner in the SIO.

Transmit interrupts, Receive interrupts, and External/Status interrupts are the sources of interrupts. Each interrupt source is enabled under program control with Channel A having a higher priority than Channel B, and with Receiver, Transmitter, and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted by the transmit buffer becoming empty. This implies that the transmitter must have had a data character written into it so t can become empty. When enabled, the receiver can interrupt the CPU in one of three ways :

Interrupt On First Character Only

Interrupt On All Receive Characters

Interrupt On A Special Receive Condition.

Interrupt On First Character Only.This mode is normally used to start a software Polling loop or a DMA transfer routine using the RxRDY pin. In this mode, the SIO generates an interrupt on the first character received after this mode is selected and, thereafter, only generates an interrupt if a Special Receive Condition occurs. The Special Receive Conditions that can cause an interrupt in this mode are : Rx Overrun Error, Framing Error (in Asynchronous modes), and End Of Frame (in SDLC mode). This mode is reinitialized by the Enable Interrupt On Next Rx Character command. If a Special Receive Condition interrupt occurs in this interrupt mode, the data with the special condition is held in the receive data FIFO until an Error Reset Command is issued.

Interrupt On All Receive Characters. In this mode, an interrupt is generated whenever the receive data FIFO contains a character or a Special Receive Condition occurs. The Special Receive Conditions that can cause an interrupt in this mode are : Rx Overrun Error, Framing Error (in Asynchronous modes), End of Frame (in SDLC mode), and Parity Error (if selected).

Interrupt On A Special Receive Condition. The Special Receive Condition interrupt is not, as such, a separate interrupt mode. Before a Special Receive Condition can cause an interrupt, either the Interrupt On First Character Only or Interrupt On All Receive Characters mode must be selected. The Special Receive Condition interrupt will modify the receive interrupt vector if Status Affects Vector is enabled. The Special Receive Condition status is displayed in the upper four bits of Status Register 1. Two of the conditions causing a special receive interrupt are latched when they occur ; they are : Parity Error and Rx Overrun Error. These status bits may only be reset by an Error Reset command. When either of these conditions occur, a read of Status Register 1 will reflect any errors in the current word in the receive buffer plus any parity or overrun errors since the last Error Reset command was issued.

External/Status Interrupts. The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins ; however, an External/Status interrupt is also caused by a Transmit Underrun condition or by the detection of a Break (Asynchronous mode) or Abort (SDLC mode) sequence in the received data stream. When any one of the above conditions occur, the external/status logic latches the current state of all five input conditions, and generates an interrupt. To reinitialize the external/status logic to detect another transition, a Reset External/Status Interrupts command must be issued. The Break/Abort condition allows the SIO to generate an interrupt when the Break/Abort sequence is detected and terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Break/Abort condition in external logic.

DMA Transfer

The SIO provides two output signals per channel for connection to a DMA controller ; they are TxRDY and RxRDY. The outputs are enabled under software control by writing to the Interrupt Control Register. Both outputs will pulse Low for three system clock cycles when their input conditions are active. TxRDY will be active when the Transmit Buffer becomes empty. RxRDY will be active when a character is available in the Receive Buffer. If a Special Receive Condition occurs when Interrupt On First Character Only mode is selected, a receiver interrupt will be generated and RxRDY will not become active. This will automatically inform the CPU of a discrepancy in the data transfer.

SELF TEST

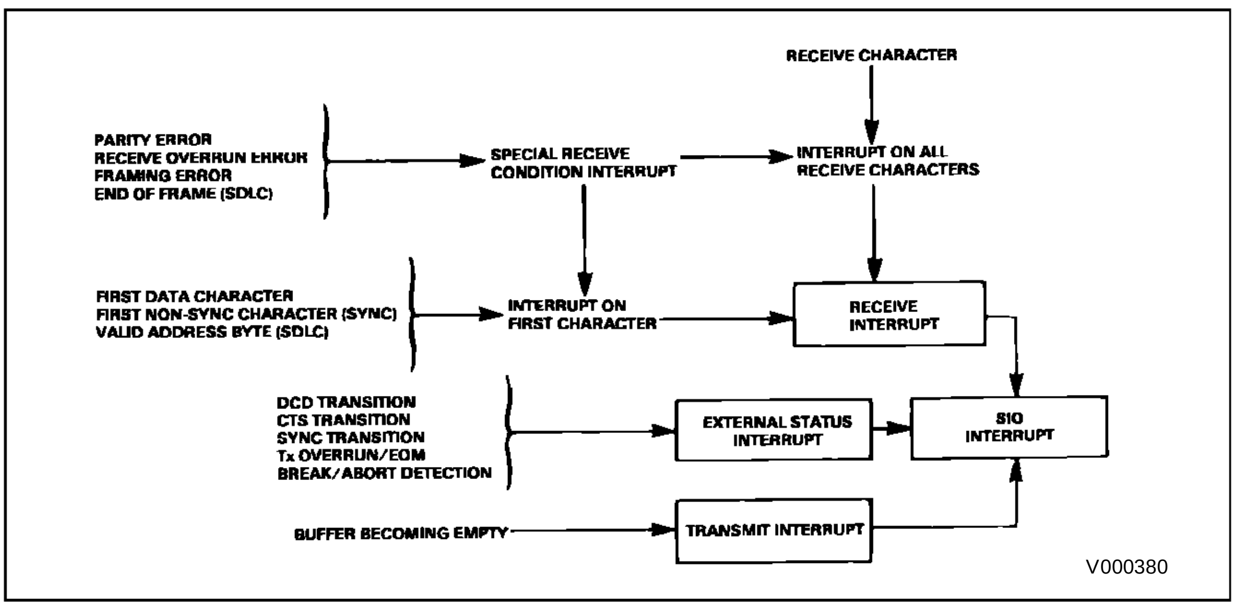
When the Loop Mode bit is set in the Command Register, the receiver shift clock input pin (RxC) and the receiver data input pin (RxD) are electrically disconnected from the internal logic. The transmit data output pin (TxD) is connected to the internal receiver data logic, and the transmit shift clock pin (TxC) is connected to the internal receiver shift clock logic. All other features of the SIO are unaffected.

BAUD RATE GENERATORS

Each channel in the SIO contains a programmable baud rate generator (BRG). Each BRG consists of an 8-bit time constant register, an 8-bit down counter, a control register, and a flip-flop on the output to provide a square wave signal out. In addition to the flip-flop on the output, there is also a flip-flop on the input clock ; therefore, the maximum output frequency of the BRG is one-forth of the input clock frequency. This maximum output frequency occurs when divide by four mode is selected, and the time constant register is loaded with the minimum count of "01H". The equation to determine the output frequency is :

$$\frac{\text{Output}}{\text{Frequency}} = \frac{\text{Input Frequency}}{\text{(divide by selected) X (time constant value in decimal)}}$$

Figure 7 : Interrupt Structure.



For example, when the time constant register is loaded with "01H" and divide by four is selected, one output clock will occur for every four input clocks. If the time constant value loaded is "00H" (256 decimal) instead of "01H" and divide by 64 is selected, one output clock will occur for every 16384 input clocks. Note that the minimum count value is "01H" (1 decimal), and the maximum count value is "00H" (256 decimal).

The output of the baud rate generator may be programmed to drive the transmitter (BRG output on TxC), the receiver (BRG output on RxC), both (BRG output on TxC and RxC), or neither (TxC and RxC are inputs). After a reset, the baud rate generator is disabled, divide by four is selected, and TxC and RxC are inputs.

The baud rate generator should be disabled before the CPU writes to the time constant register. This is necessary because no attempt was made to synchronize the loading of a new time constant with the clock used to drive the BRG.

Figure 8 indicates the external components needed to connect a crystal oscillator to the SIO XTAL inputs. The allowed crystal parameters are also listed.

For a 3.6864MHz input signal to the baud rate generator, the time constants, listed in table 2, are loaded to obtain the desired baud rates (in x1 clock mode).

ASYNCHRONOUS OPERATION

INTRODUCTION

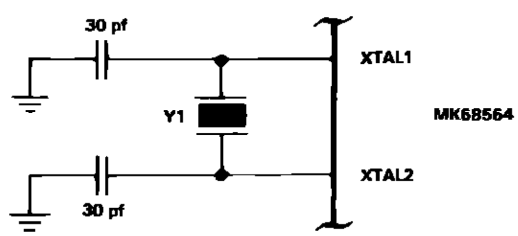
Many types of Asynchronous operations are performed by the MK68564 SIO. Figure 9 represents a typical Asynchronous message format and some of the options available on the SIO. The transmit process inserts start, stop, and parity bits to a variable data format and supplies a serial data stream to the Transmit Data output (TxD). The receiver takes the data from the Receive Data input (RxD) and strips away expected start and stop bits at a programmed clock rate. It provides error checking for overrun, parity, and carrier-loss errors, and, if desired, provides interrupts for these conditions.

To set up the SIO for Asynchronous operation, the following registers need to be initialized : Mode Control Register, Interrupt Control Register, Receiver Control Register, and Transmitter Control Register. The Mode Control Register must be programmed before the other registers to assure proper operation of the SIO. The following registers are used to transfer data or to communicate status between the SIO and the CPU or other bus master when operating in Asynchronous modes : Command Register, Status Register 0, Status Register 1, Data Register, and the Vector Register.

Table 2 : Time-Constant Values.

Rate	Time Constant	Divide By	Error
19200	48	4	
9600	96	4	
7200	128	4	
4800	192	4	
3600	256	4	
2400	24	64	
2000	29	64	69 %
1800	32	64	
1200	48	64	
600	96	64	
300	192	64	

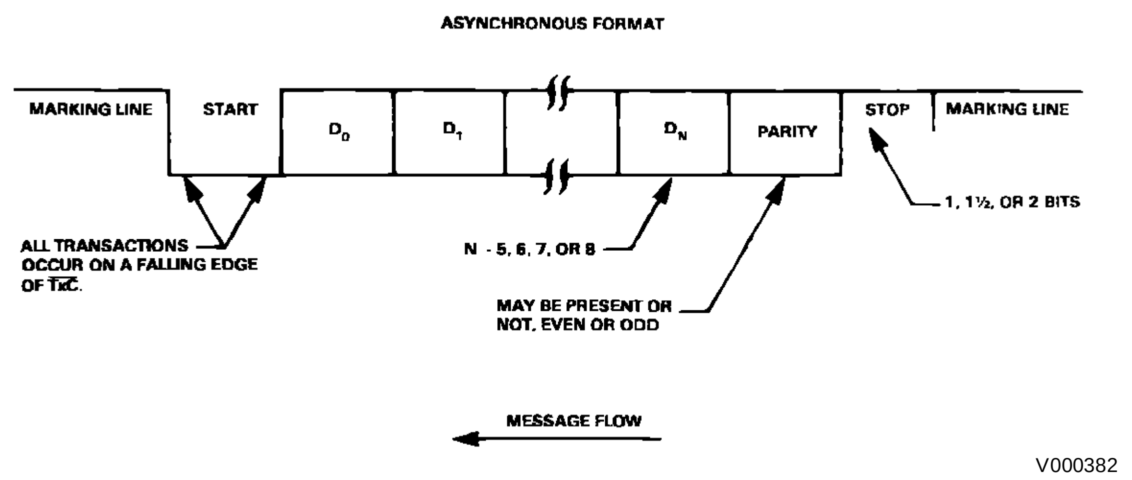
Figure 8 : SIO External Oscillator Components.



CRYSTAL PARAMETERS :

Parallel Resonance, Fundamental Mode AT Cut
Rs â 150Ω (Fr = 2.8 - 5.0MHz)
Rs â 300Ω (Fr = 2.0 - 2.7MHz)
Cl = 18pf ; Cm = 0.02pF ; Ch = 5pF ; Lm = 96MHz
Fr (typ) = 2.457MHz

Figure 9 : Asynchronous Message Format.



The SIO provides five I/O lines that may be used for modem control, for external interrupts, or as general purpose I/O. The Request To Send (RTS) and Data Terminal Ready (DTR) pins are outputs that follow the inverted state of their respective bits in the Transmitter Control Register. The RTS pin can also be used to signal the end of a message in Asynchronous modes, as explained below in the transmitter section. The Data Carrier Detect (DCD), Clear To Send (CTS), and SYNC pins are inputs to the SIO in Asynchronous modes. DCD and CTS can be used as auto enables to the receiver and transmitter, respectively, or if External/Status Interrupts are enabled all three input pins will be monitored for a change of status. If these inputs change for a period of time greater than the minimum specified pulse width, an interrupt will be generated.

In the following discussion, all interrupt modes are assumed enabled.

ASYNCHRONOUS TRANSMIT

Start of Transmission. The SIO will start transmitting data when the Transmit Enable bit is set to a one, and a character has been loaded into the transmit buffer. If the TxAuto Enables bit is set, the SIO will wait for a Low on the Clear To Send input (CTS) before starting data transmission. The Tx Auto Enables feature allows the programmer to send the first data character of the message to the SIO without waiting for CTS to go Low. In all cases, the Transmit Enable bit must be set before transmission can begin. The transitions on the CTS pin will generate External/Status interrupt requests and also latch up the external/status logic. The external/status logic should be rearmed by issuing a Reset External/Status Interrupts command.

Transmit Characteristics. The SIO automatically inserts a start bit, the programmed parity bit (odd, even, or no parity), and the programmed number of stop bits to the data character to be transmitted. The transmitter can transmit from one to eight data bits per character. All characters are transmitted least-significant bit first. When the character length programmed is six or seven bits, the unused bits of the transmit buffer are automatically ignored. When a character length of five bits or less is programmed, the data loaded into the transmit buffer must be formatted as described in the Transmitter Control Register part of the Register Description section. Serial data is shifted out of the TxD pin on the falling edge of the Transmit Clock (TxC) at a rate equal to 1, 1/16th, 1/32nd, or 1/64th of TxC.

Data Transfer. The SIO will signal the CPU or other bus master with a transmit interrupt request and set the Tx Buffer Empty bit in Status Register 0, every time the contents of the transmit buffer are loaded into the transmit shift register. The interrupt request will be cleared when a new character is loaded into the transmit buffer, or a Reset Tx Interrupt Pending command (Command 5) is issued. If Command 5 is issued, the transmit buffer will have to be loaded before any additional transmit interrupt requests are generated. The Tx Buffer Empty bit is reset when a new character is loaded into the transmit buffer.

The All Sent bit in Status Register 1 is used to indicate when all data in the shift register has been transmitted, and the transmit buffer is empty. This bit is Low, while the transmitter is sending characters, and it will go High one bit time after the transmit clock that clocks out the last stop bit of the character on the TxD pin. No interrupts are generated by the All Sent bit transitions. The Request To Send (RTS) bit in the Transmitter Control Register may also be used to signal the end of transmission. If this bit is set to a one, its associated output pin (RTS) will go Low. When this bit is reset to a zero, the RTS pin will go High one bit time after the transmit clock that clocks out the last stop bit, only if the transmit buffer is empty.

The Transmit Data output (TxD) is held marking (High) after a reset or when the transmitter has no data to send. Under program control, the Send Break command can be issued to hold TxD spacing (Low) until the command is cleared, even if the transmitter is not enabled.

ASYNCHRONOUS RECEIVE

Asynchronous operation begins when the Receiver Enable bit in the Receiver Control Register is set to a one. If the Rx Auto Enables bit is also set, the Data Carrier Detect (DCD) input pin must be Low as well. The receiver will start assembling a character as soon as a valid start bit is detected, if a clock mode other than x1 is selected. A valid start bit is a High-to-Low transition on the Receive Data input (RxD) with the Low time lasting at least one-half bit time. The High-to-Low transition starts an internal counter and, at mid-bit time, the counter output is used to sample the input signal to detect if it is still Low. When this condition is satisfied, the following data bits are sampled at mid-bit time until the entire character is assembled. The start bit detection logic is then rearmed to detect the next High-to-Low transition. If the x1 clock mode is selected, the start bit detection logic is disabled, and bit synchronization must be accomplished externally. Receive data is sampled on the rising edge of the Receiver Clock (RxC).

The receiver may be programmed to assemble five to eight data bits, plus a parity bit, into a character. The character is right-justified in the shift register and then transferred to the receive data FIFO. All data transfers to the FIFO are in eight-bit groups. If the character length assembled is less than eight bits, the receiver inserts ones in the unused bits. If parity is enabled, the parity bit is transferred with the character, unless eight bits per character is programmed, in which case, the parity bit is stripped from the character before transfer.

A Receiver Interrupt request is generated every time a character is shifted to the top of the receive data FIFO, if Interrupt On All Receive Characters mode is selected. The Rx Character Available bit in Status Register 0 is also set to a one every time a character is shifted to the top of the receive data FIFO. The Rx Character Available bit is reset to a zero when the receive buffer is read.

After a character is received, it is checked for the following error conditions :

Parity Error. If parity is enabled, the Parity Error bit in Status Register 1 is set to a one whenever the parity bit of the received character does not match the programmed parity. Once this bit is set, it remains set (latched), until an Error Reset command (Command 6) is issued. A Special Receive Condition interrupt is generated when this bit is set, if parity is programmed as a Special Receive Condition.

Framing Error. The CRC/Framing Error bit in Status Register 1 is set to a one, if the character is assembled without a stop bit (a Low level detected instead of a stop bit). This bit is set only for the character on which the framing error occurred ; it is updated at every character time. Detection of a framing error adds an additional one-half of a bit time to the character time, so the framing error is not interpreted as a new start bit. A Special Receive Condition interrupt is generated when this bit is set..

Overrun Error. If four or more characters are received before the CPU (or other bus master) reads the receive buffer, the fourth character assembled will replace the third character in the receive data FIFO. If more than four characters have been received, the last character assembled will replace the third character in the data FIFO. The character that has been written over is flagged with an overrun error in the error FIFO.

When this character is shifted to the top of the receive data FIFO, the Receive Overrun Error bit in Status Register 1 is set to a one ; the error bit is latched in the status register, and a Special Receive Condition interrupt is generated. Like Parity Error, this bit can only be reset by an Error Reset Command.

Break Condition. A break character is defined as a start bit, an all zero data word, and a zero in place of the stop bit. When a break character is detected in the receive data stream, the Break/Abort bit in Status Register 0 is set to a one, and an External/Status interrupt is requested. This interrupt is then followed by a Framing Error interrupt request when the CRC/Framing Error bit in Status Register 1 is set. A Reset External/Status Interrupts command (Command 2) should be issued to reinitialize the break detection interrupt logic. The receiver will monitor the data stream input for the termination of the break sequence. When this condition is detected, the Break/Abort bit will be reset, if

Command 2 has been issued, and another External/Status interrupt request will be generated. This interrupt should also be handled by issuing Command 2 to reinitialize the external/status logic. At the end of the break sequence, a single null character will be left in the receive data FIFO. This character should be read and discarded.

Because Parity Error and Receive Overrun Error flags are latched, the error status that is read from Status Register 1 reflects an error in the current word in the receive data FIFO, plus any parity or overrun errors received since the last Error Reset command. To keep correspondence between the state of the error FIFO and the contents of the receive data FIFO, Status Register 1 should be read before the receive buffer. If the status is read after the data and more than one character is stacked in the data FIFO during the read of the receive buffer, the status flags read will be for the next word. Keep in mind that when a character is shifted up to the top of the data FIFO (the receive buffer), its error flags are shifted into Status Register 1

.An exception to the normal flow of data through the receive data FIFO occurs when the Receive Interrupt On First Character Only mode is selected. A Special Receive Condition interrupt in this mode holds the error data, and the character itself (even if read from the data FIFO) until the Error Reset command (command 6) is issued. This prevents further data from becoming available in the receiver, until Command 6 is issued, and allows CPU intervention on the character with the error even if DMA or block transfer techniques are being used.

SYNCHRONOUS OPERATION

INTRODUCTION

Before describing byte-oriented, synchronous transmission and reception, the three types of character synchronization - Monosync, Bysync, and External Sync - require some explanation. These modes use the x1 clock for both Transmit and Receive operations. Data is sampled on the rising edge of the Receive Clock input ($\overline{\text{RxC}}$). Transmitter data transitions occur on the falling edge of the Transmit Clock input ($\overline{\text{TxC}}$).

The differences between Monosync, Bisync, and External Sync are in the manner in which initial receive character synchronization is achieved. The mode of operation must be selected before sync characters are loaded, because the registers are used differently in the various modes. Figure 10 shows the formats for all three synchronous modes.

MONOSYNC. In the Monosync mode (8-bit sync mode), the transmitter transmits the sync character in Sync Word Register 1. The receiver compares the single sync character with the programmed sync character stored in Sync Word Register 2. A match implies character synchronization and enables data transfer. The $\overline{\text{SYNC}}$ pin is used as an output in this mode and is active for the part of the receive clock that detects the sync character.

BISYNC. In the Bisync mode (16-bit sync mode), the transmitter transmits the sync character in Sync Word Register 1 followed by the sync character in Sync Word Register 2. The receiver compares the two contiguous sync characters with the programmed sync characters stored in Sync Word Registers 1 and 2. A match implies character synchronization and enables data transfer. The $\overline{\text{SYNC}}$ pin is used as an output in this mode and is active for the part of the receive clock that detects the sync characters.

External Sync. In the External Sync mode, the transmitter transmits the sync character in Sync Word Register 1. Character synchronization for the receiver is established externally. The $\overline{\text{SYNC}}$ pin is an input that indicates that external character synchronization has been achieved. After the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{\text{SYNC}}$ input pin (see figure 11). The $\overline{\text{SYNC}}$ input pin must be held Low until character synchronization is lost. Character assembly begins on the rising edge of the Receive Clock that precedes the falling edge of the $\overline{\text{SYNC}}$ input pin.

In all cases, after a reset (hardware or software), the receiver is in the Hunt phase, during which time the SIO looks for character synchronization. The Hunt phase can begin only when the receiver is enabled, and data transfer can begin only when character synchronization has been achieved. If character synchronization is lost, the Hunt phase can be re-entered by setting the Enter Hunt Mode bit in the Receiver Control Register. In the transmit mode, the transmitter always sends the programmed number of sync bits (8 or 16), regardless of the bits per character programmed.

In the Monosync, Bisync, and External Sync modes, assembly of received data continues until the SIO is reset, or until the receiver is disabled (by command or the DCD pin in the Rx Auto Enables mode), or until the CPU sets the Enter Hunt Mode bit.

After initial synchronization has been achieved, the operation of the Monosync, Bisync, and External Sync modes is quite similar. Any differences are specified in the following text.

To set up the SIO for Synchronous operations, the following registers need to be initialized : Mode

Control Register, Interrupt Control Register, Receiver Control Register, Transmitter Control Register, Sync Word 1, and Sync Word 2. The Mode Control Register must be programmed before other registers to assure proper operation of the SIO. The following registers are used to transfer data or communicate status between the SIO and the CPU or other bus master : Command Register, Status Register 0, Status Register 1, Data Register, and the Vector Register.

The SIO provides four I/O lines in Synchronous modes that may be used for modem control, for external interrupts, or as general purpose I/O. The Request To Send (RTS) and Data Terminal Ready (DTR) pins are outputs that follow the inverted state of their respective bits in the Transmit Control Register. The Data Carrier Detect (DCD) and Clear To Send (CTS) pins are inputs that can be used as auto enables to the receiver and transmitter, respectively. If External/Status Interrupts are enabled, the DCD and CTS pins will be monitored for a change of status. If these inputs change for a period of time greater than the minimum specified pulse width, an interrupt will be generated.

In the following discussion, all interrupt modes are assumed enabled.

SYNCHRONOUS TRANSMIT

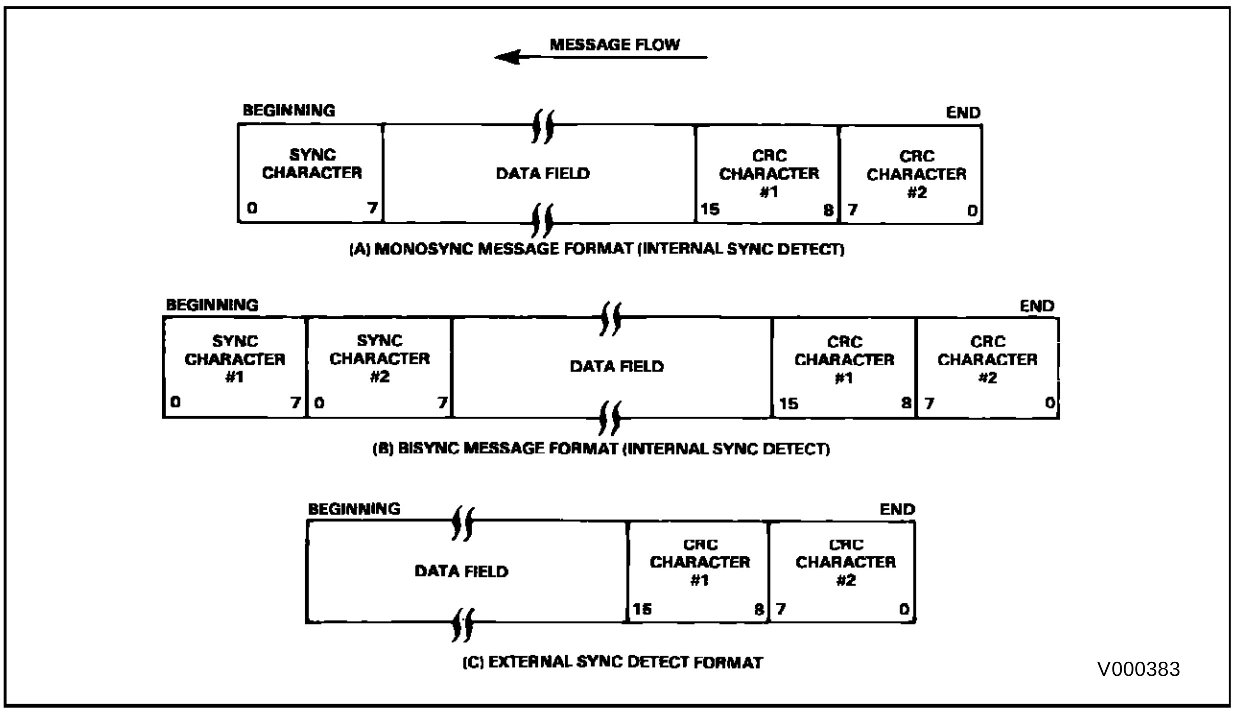
Initialization. Byte-oriented transmitter programs are usually initialized with the following parameters : odd-even or no parity, x1 clock mode, 8- or 16-bit sync character(s), CRC polynomial, Transmit Enables, interrupt modes, and transmit character length. If Parity is enabled, the transmitter will only add a parity bit to a character that is loaded into the transmit buffer ; it will not add a parity bit to the automatically inserted sync character(s) or the CRC characters.

One of two polynomials may be used with Synchronous modes, CRC-16 ($X^{16} + X^{15} + X^2 + 1$) or SDLC-CRC ($X^{16} + X^{12} + X^5 + 1$). For either polynomial (SDLC mode not selected), the CRC generator and checker are reset to all zeros. Both the receiver and transmitter use the same polynomial.

After reset (hardware or software), or when the transmitter is not enabled, the Transmit Data (TxD) output pin is held High (marking). Under program control, the Send Break bit in the Transmitter Control Register can be set to a one, forcing the TxD output pin to a Low level (spacing), even if the transmitter is not enabled. The spacing condition will persist until the Send Break bit is reset to a zero. A programmed break is effective as soon as it is written into the Transmit Control Register ; any characters in the transmit buffer and transmit shift register are lost.

If the transmit buffer is empty when the Transmit Enable bit is set to a one, the transmitter will start sending 8- or 16-bit sync characters. Continuous syncs will be transmitted on the TxD output pin, as long as no data is loaded into the transmit buffer. Note, if a

Figure 10 : Synchronous Formats.



character is loaded into the transmit buffer before enabling the transmitter, that character will be sent in place of the sync character(s).

Start of Transmission. Transmission will begin with the loading of the first data character into the transmit buffer, if the transmitter is already enabled. For CRC to be calculated correctly on each message, the CRC generator must be reset to all zeros before the first data character is loaded into the transmit buffer. This is accomplished by issuing a Reset Tx CRC Generator command in the Command Register.

Synchronous Transmit Characteristics. In all Synchronous modes, characters are sent with the least-significant bits first. All data is shifted out of the Transmit Data pin (TxD) on the falling edge of the Transmit Clock (TxC). The transmitter can transmit from one to eight data bits per character. This requires right-hand justification of data written to the transmit buffer, if the selected word length is less than eight bits per character. When the programmed character length is six or seven bits, the unused bits in the transmit buffer are ignored. If a word length of five bits per character or less is selected, the data loaded into the transmit buffer must be formatted as described in the Transmit Control register part of the Register Description section.

The number of bits per character to be transmitted can be changed on the fly. Any data written to the transmit buffer, after the bits per character field is changed, are affected by the change. The same is true of any characters in the buffer at the time the bits per character field is changed. The change in the number of bits per character does not affect the character in the process of being shifted out.

A transmitted message can be terminated by CRC and sync characters, by sync characters only, or by pad characters (replacing the sync character(s) in the Sync Word Registers with pad characters). How a message is terminated is controlled by the Tx Underrun/EOM latch in Status Register 0.

Figure 11a : External Sync Timing.

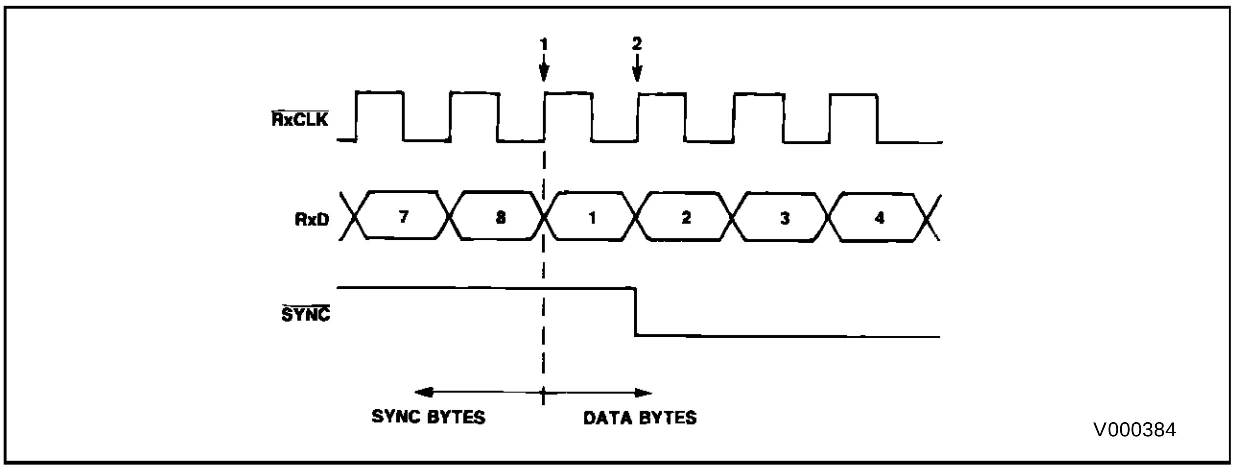
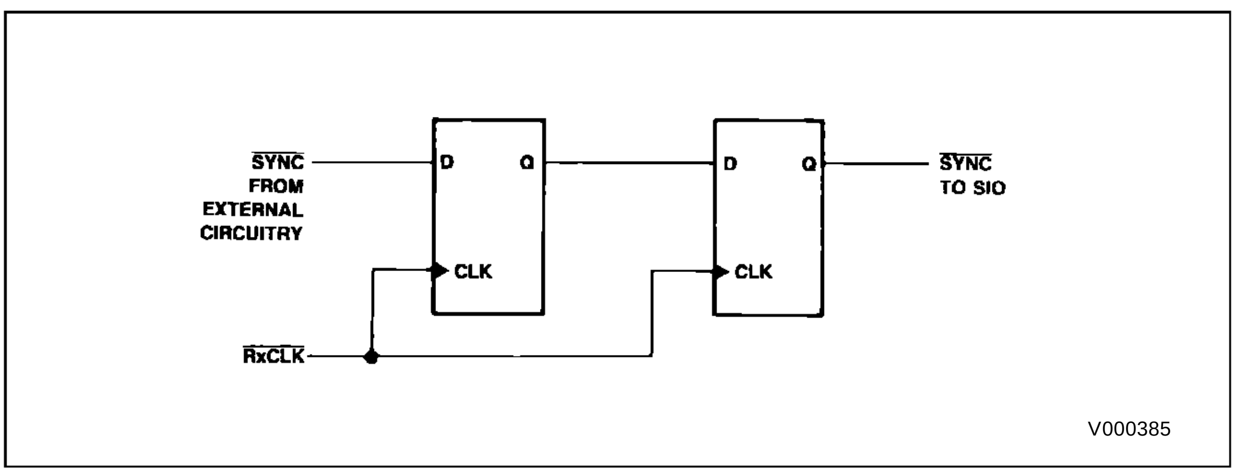


Figure 11b : Simple External Sync Delay.



Data Transfer. A Transmit Interrupt is generated each time the transmit buffer becomes empty. The interrupt may be satisfied either by writing another character into the transmit buffer or by resetting the Transmit Interrupt Pending latch with a Reset Tx Interrupt Pending command. If the interrupt is satisfied with this command, and nothing more is written into the transmit buffer, there can be no further Transmit Interrupts due to a Buffer Empty condition, because it is the process of the buffer becoming empty that causes the interrupts. This situation does cause a Transmit Underrun condition when the data in the shift register is shifted out.

Another way of detecting when the transmitter requires service is to poll the Tx Buffer Empty bit in Status Register 0. This bit is set to a one every time the data in the transmit buffer is downloaded into the transmit shift register. When data is written to the transmit buffer, this bit is reset to zero.

The SIO has all the signals and controls necessary to implement a DMA transfer routine for the transmitter. The routine may be configured to enable the DMA controller, after the first character is written to the transmit buffer, and then using the $\overline{TxRDY}$ output pin to signal the DMA that the transmitter requires service. If a data character is not loaded into the transmit buffer by the time the transmit shift register is empty, the SIO enters the Transmit Underrun condition.

Transmit Underrun/End of Message. When the transmitter has no further data to transmit, the SIO inserts filler characters to maintain synchronization. The SIO has two programmable options for handling this situation : sync characters can be inserted, or the CRC characters generated so far can be sent, followed by sync characters. These options are controlled by the state of the Transmit Underrun/EOM Latch in Status Register 0.

Following a hardware or software reset, the Transmit Underrun/EOM Latch is set to a one. This allows sync characters to be inserted when there is no data to send. CRC is not calculated on the automatically inserted sync characters. To allow CRC characters to be sent when the transmitter has no data, the Transmit Underrun/EOM Latch must be reset to zero. This latch is reset by issuing a Reset Tx Underrun/EOM Latch command in the Command Register. Following the CRC characters, the SIO sends sync characters to terminate the message.

There is no restriction as to when, in the message, the Transmit Underrun/EOM Latch can be reset, but once the reset command is issued, the 16-bit CRC is sent and followed by sync characters the first time the transmitter has no data to send. A Transmit Underrun condition will cause an External/Status Interrupt to be generated whenever the Transmit Underrun/EOM Latch is set.

For sync character insertion only, at the termination of a message, a Transmit Interrupt is generated only after the first automatically inserted sync character is loaded into the transmit shift register. The status bits in Status Register 0 indicate that the Transmit Underrun/EOM Latch and the Tx Buffer Empty bit are set.

For CRC insertion, followed by sync characters, at the termination of a message, the Transmit Underrun/EOM Latch is set, and the Tx Buffer Empty bit is reset while the CRC characters are being sent. When the CRC characters are completely transmitted, the Tx Buffer Empty status bit is set, and a Transmit Interrupt is generated, indicating to the CPU that another message can begin. This Transmit Interrupt occurs when the first sync character following the CRC characters is loaded into the transmit shift register. If no more messages are to be transmitted, the program can terminate transmission by disabling the transmitter.

CRC Generation. Setting the Tx CRC Enable bit in the Transmit Control Register initiates CRC accumulation when the program sends the first data character to the SIO. To ensure CRC is calculated correctly on each message, the Reset Tx CRC Generator command should be issued before the first data character of the message is sent to the SIO.

The Tx CRC Enable bit can be changed on the fly at any point in the message to include or exclude a particular data character from CRC accumulation. The Tx CRC Enable bit should be in the desired state when the data character is loaded from the transmit data buffer into the transmit shift register. To ensure this bit is in the proper state, the Tx CRC Enable bit should be loaded before sending the data character to the SIO.

Transmit Termination. The SIO is equipped with a special termination feature that maintains data integrity and validity. If the transmitter is disabled (by resetting the Transmit Enable bit or using the Tx Auto Enable signal) while a data or sync character is being transmitted, the character is transmitted as usual but is followed by a marking line instead of sync or CRC characters. When the transmitter is disabled, a character in the transmit buffer remains in the buffer. If the transmitter is disabled while CRC characters are being transmitted, the 16-bit transmission is completed, but the remaining bits of the CRC characters are replaced by sync characters.

Bisync Protocol Transmission. In a Bisync Protocol operation, once synchronization is achieved between the transmitter and receiver, fill characters are inserted to maintain that synchronization when the transmitter has no more data to send. The different options available in the SIO are described in the Transmit Underrun/End Of Message part of this section. If pad characters are to be sent in place of sync characters following the transmission of the CRC, the program can set the SIO transmitter to eight bits per character and then load "FFH" to the transmit buffer while the CRC characters are being sent. Alternatively, the sync characters in Sync Word Registers 1 and 2 can be redefined to be pad characters during this time. The following example is included to clarify this point :

The SIO interrupts the CPU with a Transmit Interrupt when the Tx Buffer Empty bit is set.

The CPU recognizes that the last character (ETX) of the message has already been sent to the SIO transmit buffer by examining the internal program status.

To force the SIO to send CRC, the CPU issues the Reset Tx Underrun/EOM Latch command and clears the current Transmit Interrupt with the Reset Tx Interrupt Pending command. Resetting the interrupt with this command prevents the SIO from requesting more data. The SIO then begins to send CRC (because the transmitter is in an underrun condition) and sets the Transmit Underrun/EOM Latch, which causes an External/Status Interrupt.

The CPU satisfies the External/Status Interrupt by loading pad characters into the transmit buffer and clears the interrupt by issuing the Reset External/Status Interrupt command.

The pad character will follow the CRC characters in this sequence, instead of the usual sync characters. A Transmit Interrupt is generated when the pad character is loaded into the transmit shift register.

From this point on, the CPU can send more pad characters or sync characters.

The transparent mode of operation in Bisync Protocol is made possible with the SIO's ability to change the Tx CRC Enable bit at any time during program sequencing and with the additional capability of inserting 16-bit sync characters. Exclusion of DLE (Data Link Escape) characters from CRC calculation can be achieved by disabling CRC calculations immediately preceding the DLE character transfer to the transmit buffer. In the case of a transmit underrun condition in the transparent mode, a pair of DLE-SYN characters is sent. The SIO can be programmed to send the DLE-SYNC sequence by loading a DLE character into Sync Word Register 1 and a SYNC character into Sync Word Register 2.

The SIO always transmits two sync characters (16 bits) in Bisync mode. If additional sync characters are to be transmitted before a message, the CPU can delay loading data to the transmit buffer until the required number of syncs have been sent. No CRC calculations are done on any automatically inserted sync characters. An alternate method of sending additional sync characters is to load the sync characters into the transmit buffer, in which case the transmitter will treat the characters as data. The Tx CRC Enable bit should not be set, until true data is going to be loaded into the buffer, to avoid performing CRC calculations on the additional sync characters.

SYNCHRONOUS RECEIVE

Initialization. Byte-oriented receive programs are usually initialized with the following parameters : odd-even or no parity, x1 clock mode (necessary because of the start bit detection logic), 8- or 16-bit sync character(s), CRC polynomial, Receiver Enables, interrupt modes, and receive character length. Care must be taken if Parity is enabled. The receiver will usually detect a Parity Error on all sync characters, after synchronization is achieved, and on the CRC characters.

Receiver Hunt Mode. After the SIO is initialized for a Synchronous receive operation, the receiver is in the Hunt phase. During the Hunt phase, the receiver does a bit-by-bit comparison of the incoming data stream and the sync character(s) stored in the Sync Word Register 2 (for Monosync mode) and Sync Word Registers 1 and 2 (for Bisync mode). When a match occurs, the Hunt phase is terminated, and the following data bits are assembled into the programmed character length and loaded into the receive data FIFO.

Receive Characteristics. The receiver may be programmed to assemble five to eight data bits into a character. The character is right-justified in the shift register and transferred to the receive data FIFO. All data transfers to the FIFO are in 8-bit groups. When the programmed character length is less than eight bits, the most significant bit(s) transferred with a character will be the least significant bit(s) of the next character. The programmed character length may be changed on the fly during a message ; however, care must be taken to assure that the change is effective before the number of bits specified for the character length have been assembled.

When the Sync Character Load Inhibit bit in the Receiver Control Register is set, all characters in the receive data stream that match the byte loaded into Sync Word Register 1 will be inhibited from loading into the receive data FIFO. The comparison between Sync Word Register 1 and the incoming data occurs at a character boundary time. This is an 8-bit comparison, regardless of the bits per character programmed. CRC calculations will be performed on all bytes, even if the characters are not transferred to the receive data FIFO, as long as the Rx CRC Enable bit is set.

Data Transfer and Status Monitiring. After character synchronization is achieved, the assembled characters are transferred to the receive data FIFO, and the status information for each character is transferred to the receive error FIFO. The following four modes are available to transfer the received data and its associated status to the CPU.

No Receive Interrupts Enabled. This mode is used either for polling operations or for off-line conditions. When transferring data, using a polling routine, the Rx Character Available bit in Status Register 0 should be checked to determine if a receive character is available for transfer. Only when a character is available should the receive buffer and Status Register 1 be read. The Rx Character Available bit is set when a character is loaded to the top of the receive data FIFO. This bit is reset during a read of the receive buffer.

Interrupt On First Character Only. This interrupt mode is normally used to start a DMA transfer routine or, in some cases, a polling loop. The SIO will generate an interrupt the first time a character is shifted to the top of the receive data FIFO after this mode is selected or reinitialized. An interrupt will be generated thereafter only if a Special Receive Condition is detected. This mode is reinitialized with the Enable Interrupt On Next Receive Character command. Parity Errors do not cause interrupts in this mode ; however, a Receive Overrun Error will.

Interrupt On Every Character. This interrupt mode will generate a Receiver Interrupt every time a character is shifted to the top of the receive data FIFO. A Special Receive Condition interrupt on a parity error is optional in this mode.

Special Receive Condition Interrupt. The special condition interrupt mode is not an interrupt mode as such, but works in conjunction with Interrupt On Every Character or Interrupt On First Character Only modes. When the Status Affects Vector bit in either channel is set, a Special Receive condition will modify the Receive Interrupt vector to signal the CPU of the special condition. Receive Overrun Error and Parity Error are the only Special Receive Conditions in Synchronous receive mode. The overrun and parity error status bits in Status Register 1 are latched when they occur ; they will remain latched until an Error Reset command is issued. As long as either one of these bits is set, a Special Receive Condition Interrupt will be generated at every character available time. Since these two status bits are latched, the error status in Status Register 1, when read, will reflect an error in the current word in the receive buffer, in addition to any Parity or Overrun errors received since the last Error Reset command.

CRC Error Checking and Receiver Message Termination. A CRC error check on the received message can be performed on a per character basis under program control. The Rx CRC Enable bit must set/reset by the program before the next character is transferred from the receive shift register to the receive data FIFO. This ensures proper inclusion or exclusion of data characters in the CRC check.

There is an 8-bit delay between the time a character is transferred to the receive data FIFO and the time the same character starts to enter the CRC checker. An additional 8-bit times are needed to perform CRC calculations on the character. Due to this serial nature of CRC calculations, the Receive Clock ($\overline{RxC}$) must cycle 16 times after the second CRC character has been loaded into the receive data FIFO or 20 times (the previous 16 plus 3-bit buffer delay and 1-bit input delay) after the last bit is at the RxD input, before CRC calculation is complete. The CRC Framing Error bit in Status Register 1 will contain the comparison results of the CRC checker. The comparison results should be zero, indicating error-free transmission. The results in the status bit are valid only at the end of CRC calculation. If the result is examined before this time, it usually indicates an error (the bit is High). The comparison is made at each character available time and is valid until the character is read from the receive data FIFO.

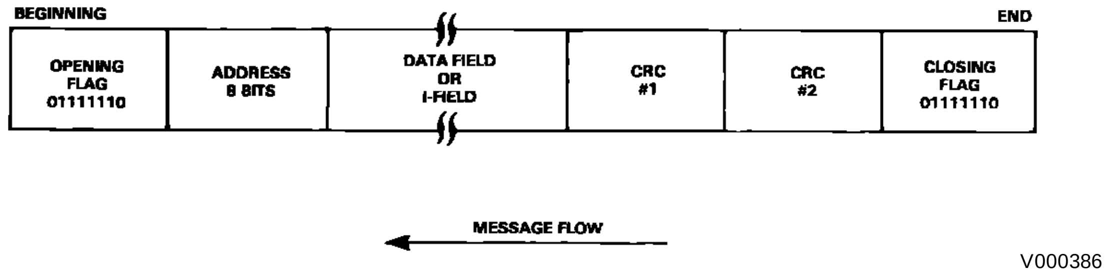
SDLC/HDLC OPERATION

INTRODUCTION

The MK68564 SIO is capable of handling both High-level Synchronous Data Link Control (HDLC) and IBM Synchronous Data Link Control (SDLC) protocols. In the following discussion, only SDLC is referenced because of the high degree of similarity between SDLC and HDLC.

The SDLC mode is considerably different from Monosync and Bisync protocols, because it is bit oriented rather than character oriented. Bit orientation makes SDLC a flexible protocol in terms of mes-

Figure 12 : Transmit/Receive SDLC/HDLC Message Format.



sage length and bit patterns. The SIO has several built-in features to handle variable message length. Detailed information concerning SDLC protocol can be found in literature on this subject, such as IBM document GA27-3093.

The SDLC message, called the frame (figure 12), is opened and closed by flags, which are similar to the sync characters used in other Synchronous protocols. The SIO handles the transmission and recognition of the flag characters that mark the beginning and end of the frame. Note that the SIO can receive shared-zero flags but cannot transmit them. The 8-bit address field of a SDLC frame contains the secondary station address. The SIO receiver has an Address Search mode, which recognizes the secondary station so that it can accept or reject a frame.

The control field of the SDLC frame is transparent to the SIO ; it is simply transferred to the CPU. The SIO handles the Frame Check sequence in a manner that simplifies the program by incorporating features such as initializing the CRC generator to all ones, resetting the CRC checker when the opening flag is detected in the receive mode, and sending the Frame Check/Flag sequence in the transmit mode. Controller hardware is simplified by automatic zero insertion and deletion logic, contained in the SIO.

To set up the SIO for SDLC operation, the following registers need to be initialized : Mode Control Register, Interrupt Control Register, Receiver Control Register, Transmitter Control Register, Sync Word Register 1, and Sync Word Register 2. The Mode Control Register must be programmed before the other registers to assure proper operation of the SIO. The following registers are used to transfer data or communicate status between the SIO and the CPU or other bus master when operating in SDLC mode : Command Register, Status Register 0, Status Register 1, Data Register, and the Vector Register.

Sync Word Register 1 contains the secondary station address, and Sync Word Register 2 stores the flag character and must be programmed to "01111110".

The SIO provides four I/O lines in SDLC mode that may be used for modem control, for external interrupts, or as general purpose I/O. The Request To Send (RTS) and Data Terminal Ready (DTR) pins are outputs that follow the inverted state of their respective bits in the Transmit Control Register. The Data Carrier Detect (DCD) and Clear To Send (CTS) pins are inputs that can be used as auto enables to the receiver and transmitter, respectively. If External/Status Interrupts are enabled, the DCD and CTS pins will be monitored for a change of status. If these inputs change for a period of time greater than the minimum specified pulse width, an interrupt will be generated.

In the following discussion, all interrupt modes are assumed enabled.

SDLC TRANSMIT

Initialization. The SIO is initialized for SDLC mode by selecting these parameters in the Mode Control Register : x1 Clock Mode, SDLC Mode, and Sync Modes Enabled. Parity is normally not used in SDLC mode, because the transmitter will not add parity to the flag character or the CRC characters, thus causing Parity Errors in the receiver. If CRC is to be calculated on the transmitted data, the SDLC-CRC polynomial must be selected in the Interrupt Control Register (CRC-16 polynomial in SDLC Mode will produce unknown results).

After reset (hardware or software), or when the transmitter is not enabled, the Transmit Data (TxD) output pin is held High (marking). Under program control, the Send Break bit in the Transmit Control Register can be set to a one, forcing the TxD output to a Low level (spacing), even if the transmitter is not enabled. The spacing condition will persist until the Send Break bit is reset to a zero. If the transmit buffer is empty when the Transmit Enable bit is set to a one, the transmitter will start sending flag characters. Continuous flags will be transmitted on the TxD output pin as long as no data is loaded into the transmit buffer.

Note : If a character is loaded into the transmit buffer before enabling the transmitter, that character will be sent in place of a flag.

An abort sequence may be transmitted at any time by issuing the Send Abort command (command 1). This causes at least eight, but less than fourteen, ones to be sent before the output reverts back to continuous flags. It is possible that the Abort sequence (eight 1's) could follow up to five continuous ones (allowed by the zero insertion logic) and, thus, cause as many as thirteen ones to be sent. Any data being transmitted and any data in the transmit buffer is lost when an abort is issued.

The zero insertion logic in the transmitter will automatically insert a 0 after five continuous ones in the data stream. This does not apply to flags or aborts.

Start of Transmission. Transmission will begin with the loading of the first character into the transmit buffer if the transmitter is already enabled. For CRC to be calculated correctly on each frame, the CRC generator must be initialized to all ones before the first character is loaded. This is accomplished by issuing a Reset Tx CRC Generator command in the Command Register. The first non-flag character transmitted is the address field. The SIO does not automatically transmit a station address, this is left to the programmer. The SIO will only transmit flags and CRC characters automatically.

SDLC Transmit Characteristics. Any length SDLC frame can be transmitted. All characters are transmitted with the least-significant bits first. All data is shifted out of the Transmit Data pin (TxD) on the falling edge of the Transmit Clock (TxC). The transmitter transmit from one to eight data bits per character. This requires right-hand justification of data written to the transmit buffer, if the word length selected is less than eight bits per character. When the programmed character length is six or seven bits, the unused bits in the transmit buffer are ignored. If a word length of five bits per character or less is selected, the data loaded into the transmit buffer must be formatted as described in the Transmit Control Register part of the Register Description section.

The number of bits per character to be transmitted can be changed on the fly. Any data, written to the transmit buffer after the bits per character field is changed, are affected by the change. The same is true of any characters in the buffer at the time the bits per character field is changed. The change in the number of bits per character does not affect the character in the process of being shifted out. Flag characters are always eigth bits in length, and CRC is always 16 bits in length, regardless of the programmed bits per character. A transmitted frame can be terminated by CRC and a flag, by a flag only, or by an abort. This is controlled by the Tx Underrun/EOM Latch and the Send Abort command.

Data Transfers. A Transmit Interrupt is generated each time the transmit buffer becomes empty. The interrupt may be satisfied either by writing another character into the transmit buffer or by resetting the Transmit Interrupt Pending latch with a Reset Tx Interrupt Pending command. If the interrupt is satisfied with this command, and nothing more is written into the transmit buffer, there are no further transmitter interrupts, and a Transmit Underrun condition will occur when the data in the shift register is shifted out. When another character is written to the buffer and loaded into the shift register, the transmit buffer can again become empty and interrupt the CPU. Following the flags in an SDLC operation, the 8-bit address field, control field, and information field may be sent to the SIO, using the Transmit Interrupt mode. The SIO transmits the frame check sequence using the Transmit Underrun feature.

When the transmitter is first enabled, the transmit buffer is already empty and obviously cannot then become empty. Therefore, no transmit interrupt can occur until after the first data character is written to the transmit buffer.

Another way of detecting when the transmitter requires service is to poll the Tx Buffer Empty bit in Status Register 0. This bit is set to a one every time the data in the transmit buffer is downloaded into the transmit shift register. When data is written to the transmit buffer, this bit is reset to zero.

The SIO has all the signals and controls necessary to implement a DMA transfer routine for the transmitter. The routine may be configured to enable the DMA controller, after the first character is written into the transmit buffer, using the TxRDY output pin to signal the DMA that the transmitter requires service. The DMA transfer can be terminated, when the DMA block count is reached, using the Tx Underrun/EOM interrupt.

Transmit Underrun/End of Message. SDLC-like protocols do not have provisions for fill characters within a message. The SIO, therefore, automatically terminates an SDLC frame when the transmit data buffer is empty, and the output shift register has no more bits to send. It does this by first sending the two bytes of CRC and the following these with one or more flags. This technique allows very high-speed transmission under DMA or CPU control, without requiring the CPU to respond quickly to the end of message situation.

The action that the SIO takes in the underrun situation depends on the state of the Transmit Underrun/EOM status bit in status Register 0. Following a reset, the Transmit Underrun/EOM bit is set to a one and prevents the insertion of CRC characters during the time there is no data to send. Consequently, flag characters are sent. If the Transmit Underrun/EOM status bit is zero when the underrun condition occurs, the 16-bit CRC character is sent, followed by one or more flag characters. The Transmit Underrun/EOM bit is reset to zero by issuing the Reset Tx Underrun/EOM Latch command in the Command Register.

The SIO begins to send a frame when data is written into the transmit buffer. Between the time the first data byte is written and the end of the message, the Reset Tx Underrun/EOM Latch command must be issued. The Transmit Underrun/EOM status bit will then be in the reset state at the end of the message (when underrun occurs), and CRC characters will automatically be sent. The transmission of the first CRC bit set the Transmit Underrun/EOM status bit to a one and generates an External/Status interrupt. Also, while CRC is being sent, the Tx Buffer Empty bit in Status Register 0 is reset to indicate that the transmit shift register is full of CRC data. When CRC has been completely sent, the Tx Buffer Empty status bit is set, and a Transmit Interrupt is generated to indicate that another message may begin. This interrupt occurs because CRC has been sent, and a flag has been loaded into the shift register. If no more messages are to be sent, the program can terminate transmission by disabling the transmitter.

Although there is no restriction as to when the Transmit Underrun/EOM bit can be reset within a message, it is usually reset after the first data character (secondary address field) is sent to the SIO. By resetting the status bit early in the message, the CPU has additional time (16 bits of CRC) to recognize if an unintentional transmit underrun situation has occured and to respond with an Abort command. Issuing the Abort command stops the flags from going on the line prematurely and eliminates the possibility of the receiver accepting the frame as valid data. This situation can happen if, at the receiving end, the data pattern immediately preceding the automatic flag insertion matches the CRC checker, giving a false CRC check result.

CRC Generation. The CRC generator must be reset to all ones at the beginning of each frame before CRC accumulation can begin. Actual accumulation begins on the first data character (address field) loaded into the transmit buffer. The Tx CRC Enable bit in the Transmit Control Register should be set to a one before the first character is loaded into the transmit buffer. In SDLC mode, all characters between the opening and the closing flags are included in CRC accumulation. The output of te CRC generator is inverted before it is transmitted.

Transmit Termination. The normal sequence at the end of a frame is

A Transmit Interrupt occurs when the last data character written to the transmit buffer is downloaded into the transmit shift register. This interrupt may be cleared by issuing a Reset Tx Interrupt Pending command.

An External/Status Interrupt occurs when the first bit of the CRC character is transmitted. This interrupt condition should first be tested to see if the interrupt was caused by the Tx Underrun/EOM bit going High and then reset by issuing a Reset External/Status Interrupts command.

A Transmit Interrupt occurs when the first bit of the flag is transmitted. This interrupt may be cleared by issuing a Reset Tx Interrupt Pending command, by loading the first character of the next message, or by disabling the transmitter.

If the transmitter is disabled while a character is being sent, that character (data or flag) is sent in the normal fashion but is followed by a marking line rather than CRC or more flag characters. If CRC characters are being sent at the time the transmitter is disabled, all 16 bits will be transmitted, followed by a marking line ; however, flags are sent in place of CRC. A character in the buffer when the transmitter is disabled remains in the buffer.

SDLC RECEIVE

Initialization. The receiver is enabled only after all of the receive parameters are initialized. After the Receiver Enable bit in the Receiver Control Register is set to a one, the receiver will be in the Hunt phase and will remain in this phase until the first flag is received. While in the SDLC mode, the receiver never re-enters the Hunt phase, unless specifically instructed to do so by the program or when an Abort character is detected in the incoming data stream.

Receiver Characteristics. The receiver may be programmed to assemble five to eight data bits into a character. The character is right-justified in the shift register and transferred to the receive data FIFO. All data transfers to the FIFO are in 8-bit groups. When the character length programmed is less than eight bits, the most significant bit(s) transferred with a character, will be the least-significant bit(s) of the next character. The character length programmed may be changed on the fly during the reception of a frame ; however, care must be taken to assure that the change is effective, before the number of bits specified for the character length has been assembled.

The address field in the SDLC frame is defined as an 8-bit field. When the Address Search Mode is selected, the receiver will compare the 8-bit character following the flag (first non-flag character) against the address programmed in Sync Word Register 1 or the hardwired global address (11111111). When the address field of the SDLC frame matches either address, data transfer will begin with the address character being loaded into the receive data FIFO. If the frame address does not match either address, the receiver will remain idle and continue checking every frame received for an address match. The address comparison is always done on the first eight bits following a flag, regardless of the bits per character programmed.

The SIO receiver is capable of matching only one address character. Once a match occurs, all data is transferred to the receive data FIFO at the programmed bits per character rate. If SDLC extended address field recognition is used (two or more address characters), the CPU program must be capable of determining whether or not the frame has a correct address field. If the correct address field is not received, the Hunt bit can be set to suspend reception and start searching for the next frame. The control field of an SDLC frame is transparent to the SIO ; it is transferred to the data FIFO as a data character. All extra zeros, inserted in the data stream by the transmitter, are automatically deleted in the receiver.

Data Transfer and Status Monitoring. After receipt of a valid flag, the assembled characters are transferred to the receive data FIFO, and the status information for each character is transferred to the receive error FIFO. The following four modes are available to transfer the received data and its associated status to the CPU.

No Receiver Interrupts Enabled. This mode is used for polling operations or for off-line conditions. When transferring data, using a polling routine, the Rx Character Available bit in Status Register 0 should be checked to determine whether or not a receive character is available for transfer. Only when a character is available should the receive buffer and Status Register 1 be read. The Rx Character Available bit is set to a one every time a character is shifted to the top of the receive data FIFO. This bit is reset when the receive buffer is read.

Interrupt On First Character Only. This interrupt mode is normally used to start a DMA transfer routine, or in some cases, a polling loop. The SIO will generate an interrupt the first time a character is shifted to the top of the receive data FIFO after this mode is selected or reinitialized. An interrupt will be generated thereafter only if a Special Receive Condition is detected. This mode is reinitialized with the Enable Interrupt On Next Received Character command. Parity Errors do not cause interrupts in this mode, but a Receive Overrun Error or an End Of Frame condition will.

Interrupt On Every Character. This interrupt mode will generate a Receiver Interrupt every time a character is shifted to the top of the receive data FIFO. A Special Receive Condition interrupt on a Parity error is optional in this mode.

Special Receive Condition Interrupt. The special condition interrupt mode is not an interrupt mode, as such, but works in conjunction with Interrupt On Every Character or Interrupt On First Character Only modes. When the Status Affects Vector bit in either channel is set, a Special Receive Condition will modify the Receive Interrupt vector to signal the CPU of the special condition. Receive Overrun Error, Parity Error, and End Of Frame are the Special Receive Conditions in SDLC mode. The Overrun and Parity error status bits in Status Register 1 are latched when they occur ; the End Of Frame bit is not latched. The two bits that are latched will remain latched and will generate a Special Receive Condition Interrupt at every character available time until an Error Reset command is issued. Since the two status bits are latched, the error status in Status Register 1, when read, will reflect an error in the current word in the receive buffer, in addition to any Parity or Overrun errors received since the last Error Reset command.

SDLC Receive CRC Checking. Control of the receiver CRC checker is automatic. It is reset by the leading flag, and CRC is calculated up to the final flag. The byte that has the End Of Frame bit set is the byte that contains the result of the CRC check. If the CRC/Framing Error bit is not set (zero), the CRC indicates a valid received message. A special check sequence is used for the SDLC check, because the transmitted CRC character is inverted. The final check must be 0001110100001111. he 2-byte CRC check characters should be read and discarded by the CPU, because the last two bits of the 2-byte SDLC CRC check characters are not transferred to the receive data FIFO due to the internal timing associated with detecting the closing flag.

Unlike Synchronous modes, the logic path in SDLC mode does not have an 8-bit delay between the time a character is transferred to the receive data FIFO and the time a character enters the CRC checker. This delay is not needed, because in SDLC, all characters between the opening and closing flags are included in the CRC calculations. When the second CRC character (six bits only) is loaded into the receive buffer, CRC calculation is complete.

SDLC Receive Termination. An SDLC frame is terminated when the closing flag is detected. The detection of the flag sets the End Of Frame bit in Status Register 1 and generates a Special Receive Condition Interrupt. In addition to the End Of Frame bit being set and the results of the CRC check, Status Register 1 has three bits of Residue code valid at this time. The Residue bits indicate the boundary between the CRC check bits and the I-field bits in the frame. A detailed description of the Residue code bits is given in the Register Description section, under Status Register 1.

Any frame can be prematurely aborted by an Abort sequence. Aborts are detected if seven or more continuous ones occur in the received data stream. This condition will cause an External/Status Interrupt to be generated with the Break/Abort bit in Status Register 0 set. After the Reset External/Status Interrupts command has been issued, a second interrupt will occur when the continuous ones condition has been cleared. This second interrupt can be used to distinguish between the Abort and Idle line conditions.

REGISTER DESCRIPTION

The following sections describe the MK68564 SIO registers. Each register is detailed in terms of bit configuration, the active states of each bit, their definitions, their functions, and their effects upon the internal hardware and external pins.

COMMAND REGISTER (CMDREG)

This register contains command and reset functions used in the programming of the SIO. This register is reset to ”00H” by a channel or hardware reset. All bits, except Loop Mode, will be read as zeros during a read cycle.

D7	D6	D5	D4	D3	D2	D1	D0
CRC 1	CRC 0	CMD 2	CMD 1	CMD 0			LOOP MODE

D7, D6 : Reset Codes 1 and 0

CRC 1	CRC 0	
0	0	Null Code (no effect)
0	1	Reset Receiver CRC Checker
1	0	Reset Transmit CRC Generator
1	1	Reset Tx Underrun/End of Message Latch

Null Code. The null code has no effect on the MK68564 SIO. It is used when writing to the Command Register for some reason other than a CRC Reset.

Reset Receiver CRC Checker. It is necessary in Synchronous modes (except SDLC) to reset the receiver CRC circuitry between received messages. The CRC circuitry may be reset by one of the following : disabling the receiver, setting the Enter Hunt Mode bit in the Receiver Control Register, or issuing this Reset command. The CRC circuitry is reset automatically in SDLC mode when the End Of Frame flag is detected. This Reset command will initialize the CRC checker circuit to all ones in SDLC mode and all zeros in the other Synchronous modes.

Reset Transmit CRC Generator. This command resets the CRC generator to all ones in SDLC mode and all zeros in the other Synchronous modes. This command should be issued after the transmitter is enabled but before the first character of a message is loaded in the transmit buffer.

Reset Transmit Underrun/EOM Latch. This command resets the Underrun/EOM latch in Status Register 0 if the transmitter is enabled. The Underrun/EOM latch controls the transmission of CRC at the end of a message in Synchronous modes. When a transmit underrun occurs and this latch is low, CRC will be appended to the end of the transmission.

D5, D4, D3 : Command Codes

Command	CMD2	CMD1	CMD0	
0	0	0	0	Null Command (no effect)
1	0	0	1	Send Abort (SDLC mode)
2	0	1	0	Reset External/ Status Interrupts
3	0	1	1	Channel Reset
4	1	0	0	Enable Interrupt On Next Rx Character
5	1	0	1	Reset Tx Interrupt Pending
6	1	1	0	Error Reset
7	1	1	1	Null Command (no effect)

Command 0 (Null). The Null command has no effect on the MK68564 SIO.

Command 1 (Send Abort). This command is used in SDLC mode to transmit a sequence of eight to thirteen ones. This command always empties the transmit buffer ans sets the Tx Underrun/EOM Latch in Status Register 0 to a one

Command 2 (Reset External/Status Interrupts)**.** After an External/Status interrupt (a change on a modem line or a Break condition, for example), the upper five bits in Status Register 0 are latched. This command reenables these bits and allows interrupts to occur again as a result of a status change. Latching the status bits captures short pulses, until the CPU has time to read the change. This command should be issued prior to enabling External/Status Interrupts.

Command 3 (Channel Reset). This command disables both the receiver and transmitter, forces TxD to a marking state ("1"), forces the modem control signals high, resets any pending interrupts from this channel, and resets all control registers. See the Reset section in the SIO System Interface Description for a more detailed list. All control registers for the channel must be rewritten after a Channel Reset command.

Command 4 (Enable Interrupt On Next Rx Character**).** This command is used to reactivate the Receive Interrupt On First Character Only interrupt mode. This command is normally issued after the present message is completed but before the next message has started to be assembled. The next character to enter the receive data FIFO after this command is issued will cause a receiver interrupt request.

Note : If the data FIFO has more than one character stored when this command is issued, the first previously stored character will cause the receiver interrupt request.

Command 5 (Reset Tx Interrupt Pending**).** When the Transmit Interrupt Enable mode is selected, the transmitter requests an interrupt when the transmit buffer becomes empty. In those cases, where there are no more characters to be sent (at the end of message, for example), issuing this command resets the pending transmit interrupt and prevents any further transmitter interrupt requests until the next character has been loaded into the transmit buffer or until CRC has been completely sent.

Command 6 (Error Reset). This command resets the upper seven bits in Status Register 1. Anytime a Special Receive Condition exists when Receive Interrupt On First Character Only mode is selected, the data with the special condition is held in the receive data FIFO until this command is issued.

Command 7 (Null). The Null command has no effect on the MK68564 SIO.

D2, D1 : Not Used (read as zeros)

D0 : Loop Mode

When this bit is set to a 1, the transmitter output is connected to the receiver input and $\overline{TxC}$ is connected to the receiver clock. $\overline{RxC}$ and RxD pins are not used by the receiver ; they are bypassed internally. RxC may still be used as the baud rate generator output in Loop Mode.

MODE CONTROL REGISTER (MODECTL)

The Mode Control Register contains control bits that affect both the receiver and the transmitter. This register must be initialized before loading the Interrupt, Tx, and Rx Control Registers, and the Sync Word Registers. This register is reset to "00H" by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
CLOCK RATE 1	CLOCK RATE 0	SYNC MODE 1	SYNC MODE 0	STOP BITS 1	STOP BITS 0	PARITY E/O	PARITY ON/OFF

D7, D6 : Clock Rate 1 and 0

These bits specify the multiplier between the input shift clock rates (TxC x RxC) and data rate. The same multiplier is used for both the transmitter and receiver, although the input clock rates may be different. In x16, x32, and x64 clock modes, the receiver start bit detection logic is enabled ; therefore, for Synchronous modes, the x1 clock rate must be specified. Any clock rate may be specified for Asynchronous mode ; however, if the x1 clock rate is selected, synchronization between the receive data and the receive clock must be accomplished externally.

CLOCK RATE 1	CLOCK RATE 0	Multiple	
0	0	x1	Clock Rate = Data Rate
0	1	x16	Clock Rate = 16 x Data Rate
1	0	x32	Clock Rate = 32 x Data Rate
1	1	x64	Clock Rate = 64 x Data Rate

D5, D4 : Sync Modes 1 and 0

These bits select the various options for character synchronization. These bits are ignored, unless Sync modes is selected in the Stop Bits filed of this register.

SYNC MODE 1	SYNC MODE 0	
0	0	8-bit Programmed Sync
0	1	16-bit Programmed Sync
1	0	SDLC Mode (01111110 flag pattern)
1	1	External Sync Mode

D3, D2 : Stop Bits 1 and 0

These bits determine the number of stop bits added to each Asynchronous character that is transmitted. The receiver always checks for one stop bit in Asynchronous mode. A special code (00) signifies that a Synchronous mode is to be selected. 1 1/2 stop bits is not allowed if x1 clock rate is selected, because it will lock up the transmitter.

STOP BIT 1	STOP BIT 0	
0	0	Sync Modes
0	1	1 Stop Bit per Character
1	0	11/2 Stop Bits per Character
1	1	2 Stop Bits per Character

D1 : Parity Even/Odd

If the Parity Enable bit is set, this bit determines whether parity is checked as even or as odd. (1 = even, 0 = odd). This bit is ignored if the Parity Enable bit is reset.

D0 : Parity Enable

If this bit is set to a one, one additional bit position beyond those specified in the bits/character control field is added to the transmitted data and is expected in the receive data. The received parity bit is transferred to the CPU as part of the data character, unless eight bits per character is selected in the Receiver Control Register.

INTERRUPT CONTROL REGISTER (INTCTL)

This register contains the control bits for the various interrupt modes and the DMA handshaking signals. This register is reset to ”00H” by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
CRC16/ SDLC	CTX RDY ENABLE	RX RDY ENABLE	RX INT MODE 1	RX INT MODE 0	STATUS AFFECTS	TX INT ENABLE	EXT INT ENABLE

D7 : CRC-16/SDLC-CRC

This bit selects the CRC polynomial used by both the transmitter and receiver. When set to a one, the CRC-16 polynomial (x16 + x15 + x2 + 1) is used ; when reset to a zero, the SDLC-CRC polynomial (x16 + x12 + x5 + 1) is used. If the SDLC mode is selected, the CRC generator and checker are preset to all ones and a special check sequence is used.

The SDLC-CRC polynomial must be selected in SDLC mode. Failure to do so will result in receiver CRC errors. When a Synchronous mode, other than SDLC, is selected, the CRC generator and checker are preset to all zeros (for both polynomials). This bit must be programmed before CRC is enabled in the receiver and transmitter control registers, to assure valid CRC generation and checking. This bit is ignored in Asynchronous modes.

D6 : Tx Ready Enable

When this bit is set to a one, the TxRDY output pin will pulse Low for three clock cycles (CLK) when the transmit buffer becomes empty. When this bit is zero, the TxRDY pin is held High.

D5 : Rx Ready Enable

When this bit is set to a one, the TxRDY output pin will pulse Low for three clockcycles (CLK) when a character is available in the receive buffer. If a Special Receive Condition is detected when the Receive Interrupt On FIrst Character Only interrupt mode is selected, the RxRDY pin will not become active ; instead, a special Receive Condition interrupt will be generated. When this bit is zero, the RxRDY pin will be held High

D4, D3 : Receive Interrupt Modes 1 and 0

Together, these two bits specify the various character-avalaible conditions that will cause interrupt requests. When receiver interrupts are enabled, a Special Receive Condition can cause an interrupt request and modify the interrupt vector. Special Receive conditions are : Rx Overrun Error, Framing Error (in async mode), End Of Frame (in SDLC mode), and Parity Error (when selected). The Rx Overrun Error and the Parity Error conditions are latched in Status Register 1 when they occur ; they are cleared by an Error Reset command (Command 4) or by a hardware or channel rest.

Rx INT MODE 1	Rx INT MODE 0	
0	0	Receive Interrupts Disabled
0	1	Receive Interrupt On First Character Only
1	0	Interrupt On All Receive Characters-parity Error is a Special Receive Condition
1	1	Interrupt On All Receive Characters-parity Error is not a Special Receive Condition

Receive Interrupts Disabled. This mode prevents the receiver from generating an interrupt request and clears any pending receiver interrupts. If a character is avalaible in the receiver data FIFO, or if a Special Receive Condition exists before or during the time receiver interrupts are disabled, and receiver interrupts are then enabled without clearing these conditions, an interrupt request will immediately be generated.

Receive Interrupt On First Character Only. The receiver requests an interrupt in this mode on the first available character (or stored FIFO character), or on a Special Receive Condition. If a Special Receive Condition occurs, the data with the special condition is held in the receive data FIFO until an Error Reset command (Command 6) is issued.

The receive Interrupt On First Character Only mode can be re-enabled by the Enable Interrupt On Next Rx Character command (Command 4). If this interrupt mode was terminated by a Special Receive Condition, the Error Reset command must be issued, before Command 4, for proper operation to resume.

Interrupt On All Receive Characters. This mode ammows an interrupt for every character received (or character in the receive data FIFO) and provides a unique vector (if Status Affects ector is enabled) when a Special Receive Condition exists. When the interrupt request is due to a special condition, the data containing that condition, the data containing data FIFO.

D2 : Status Affects Vector

When this bit is zero, the value programmed into the Vector Register is returned during a read cycle or an interrupt acknowledge cycle. If the Vector Register has not been programmed following a hardware reset, then ”0FH” is returned.

When this bit is a one, the vector returned during a read cycle or an interrupt acknowledge cycle is variable. The variable field returned depends on the highest-priority pending interrupt at the start of the cycle.

The Status Affects Vector control bits from both channels are logical ”or” ed together ; therefore, if either is programmed to a one, its operation affects both channels. This is the only control bit that functions in this manner on the MK68564.

V2	V1	0	Interrupt Condition
0	0	0	Ch B Transmit Buffer Empty
0	0	1	Ch B External/status Change
0	1	0	Ch B Receive Character Available
0	1	1	Ch B Special Receive Condition*
1	0	0	Ch A Transmit Buffer Empty
1	0	1	Ch A External/status Change
1	1	0	Ch A Receive Character Available
1	1	1	Ch A Special Receive Condition*

* Special Receive Conditions : Parity Error, Rx Overrun Er-

D1 : Transmit Interrupt Enable

When this bit is set to a one, the transmitter will request an interrupt whenever the transmit buffer becomes empty. When this bit is zero, no transmitter interrupts will be requested.

D0 : External/Status Interrupt Enable

When this bit is set to a one, an interrupt will be requested by the external/status logic on any of the following occurrences : a transition (high-to-low or low-to-high) on the DCD, CTS, or SYNC input pins, a break/abort condition that has been detected and terminated, or at the beginning of CRC transmission when the Transmit Underrun/EOM latch in Status Register 0 becomes set. When this bit is zero, no External/Status interrupts will occur.

If this bit is set when an External/Status condition is pending, an interrupt will be requested. It is recommended that a Reset External/Status Interrupts command (Command 2 in the Command Register) be issued prior to enabling External/Status interrupts.

SYNC WORD REGISTER 1 (SYNC 1)

This register is programmed to contain the transmit sync character in the Monosync mode, the first eight bits of the 16-bit sync character in the Bysinc mode, or the transmit sync character in the External Sync mode. This register is not used in Asynchronous mode. In the SDLC mode, this register is programmed to contain the secondary address field used to compare against the address field of the SDLC frame. The SIO does not automatically transmit the station address at the beginning of a response frame. This register is reset to "00H" by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
SYNC/ SDLC7	SYNC/ SDLC6	SYNC/ SDLC5	SYNC/ SDLC4	SYNC/ SDLC3	SYNC/ SDLC2	SYNC/ SDLC1	SYNC/ SDLC0

SYNC WORD REGISTER 2 (SYNC 2)

This register is programmed to contain the receive sync character in the Monosync mode, the last eight bits of the 16-bit sync character in the Bisync mode, or a flag character (01111110) in the SDLC mode. This register is not used in the External Sync mode and the Asynchronous mode. This register is reset to "00H" by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
SYNC/ SDLC 15	SYNC/ SDLC 14	SYNC/ SDLC 13	SYNC/ SDLC 12	SYNC/ SDLC 11	SYNC/ SDLC 10	SYNC/ SDLC 9	SYNC/ SDLC 8

RECEIVER CONTROL REGISTER (RCVCTL)

This register contains the control bits and parameters for the receiver logic. This register is reset to "00H" by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
RX BITS CHAR 1	RX BITS CHAR 0	RX AUTO ENAB.	HUNT MODE	RX CRC ENAB.	ADDR. SEARCH	STRIP SYNC	RX ENABLE

D7, D6 : Receiver Bits/Character 1 and 0

The state of these two bits determines the number of bits to be assembled as a character in the received serial data stream. If Parity is enabled, one additional bit will be added to each character. The number of bits per character can be changed while a character is being assembled but only before the number of bits currently programmed is reached. All data is right-justified in the shift register and transferred to the receive data FIFO in 8-bit groups.

In Asynchronous mode, transfers are made at character boundaries, and all unused bits of character are set to a one. In Synchronous modes and SDLC mode, an 8-bit segment of the serial data stream is transferred to the data FIFO when the internal counter reaches the number of bits per character programmed. For less than eight bits per character, no parity, the MSB bit(s) of the first transfer will be the LSB bit(s) of the next transfer.

RX BITS CHAR 1	RX BITS CHAR 0	Bits/character (no parity)	Bits/character (parity)
0	0	5	6
0	1	6	7
1	0	7	8
1	1	8	9

D5 : Receiver Auto Enables

When this bit is set to a one, and the Receiver Enable bit is also set, a Low on the DCD input pin becomes the enable for the receiver. When this bit is zero, the DCD pin is simply an input to the SIO, and its status is displayed in Status Register 0.

D4 : Enter Hunt Mode

This bit, when written to a one, rearms the receiver synchronization logic and forces the comparison of the received bit stream to the ontents of Sync Word Register 1 and/or Sync Word Register 2, depending upon which Synchronous mode is selected, until bit synchronization is achieved. The SIO automatically enters the Hunt mode after a channel or hardware reset, after an Abort condition is detected, or when the receiver is disabled. When the Hunt mode is entered, the Hunt/Sync bit in Status Register 0 is set to a one. When synchronization is achieved, the Hunt/Sync bit is reset to a zero. If External/Status interrupts are enabled, an interrupt request will be generated on both transitions of the Hunt/Sync bit. Enter Hunt Mode has no affect in Asynchronous modes. This bit is not latched and will always be read as a zero.

D3 : Receiver CRC Enable

This bit, when set to a one in a Synchronous mode other than SDLC, is used to initiate CRC calculation at the beginning of the last byte transferred from the receiver shift register to the receive data FIFO. This operation occurs independently of the number of bytes in the receive data FIFO. As long as this bit is set, CRC will be calculated on all characters received (data or sync). When a particular byte is to be excluded from CRC calculation, this bit should be reset to a zero before the next byte is transferred to the receive data FIFO. If this feature is used, caremust be taken to ensure that eight bits per character are selected in the reciever because of an inherent eight-bit delay from the receiver shift register to the CRC checker.

When this bit is set to a one in SDLC mode, the SIO will calculate CRC on all bits between the opening and closing flags. There is no delay from the receiver shift register to the CRC checker in SDLC mode. This bit is ignored in Asynchronous modes.

D2 : Address Search Mode

Setting this bit to a one in SDLC mode forces the comparison of the first non-flag character of a frame with the address programmed in Sync Word Register 1 or the global address (11111111). If a match does not occur, the frame is ignored, and the receiver remains idle until the next frame is detected. No receiver interrupts can occur in this mode, unless there is an address match. This bit is ignored in all modes except SDLC.

D1 : Sync Character Load Inhibit

When this bit is set to a one in any Synchronous mode except SDLC, the SIO compares the byte in Sync Word Register 1 with the byte about to be loaded into the receiver data FIFO. If the two bytes are equal, the load is inhibited, and no receiver interrupt will be generated by this character. CRC calculation is performed on all bytes, whether they are loaded into the data FIFO or not, when the receiver CRC is enabled. Note that the register used in the comparison contains the transmit sync character in Monosync and External sync modes. This bit is ignored in SDLC mode because all flag characters are automatically striped in this mode without performing CRC calculations on them.

If this bit is set to a one in Asynchronous modes, any character received matching the contents of Sync Word Register 1 will not be loaded into the receive data FIFO, and no receiver interrupt will be generated for the character.

D0 : Receiver Enable

When this bit is set to a one, receiver operation begins if Rx Auto Enables mode is not selected. This bit should be set only after all receiver parameters are established, and the receiver is completely initialized. When this bit is zero, the receiver is disabled ; the receiver CRC checker is reset, and the receiver is in the Hunt mode.

TRANSMITTER CONTROL REGISTER (XMTCTL)

This register contains the control bits and parameters for the transmitter logic. This register is reset to ”00H” by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
TX BITS CHAR 1	TX BITS CHAR 0	TX AUTO ENABLES	SEND BREAK	TX CRC ENABLE	DTR	RTS	TX ENABLE

D7, D6 Transmit Bits/Character 1 and 0

The state of these two bits determine the number of bits in each byte transferred from the transmit buffer to the transmit shift register. All data written to the transmit buffer must be right-justified with the least-significant bits first. The Five Or Less mode allows transmission of one to five bits per character ; however, the CPU should format the data characters as shown. If Parity is enabled, one additional bit per character will be transmitted.

TX BITS/ CHAR 1	TX BITS/ CHAR 0	Bits/character (no parity)
0	0	Five or Less
0	1	6
1	0	7
1	1	8

D7	D6	D5	D4	D3	D2	D1	D0	Five or Less
1	1	1	1	0	0	0	D	Sends One Data Bit
1	1	1	0	0	0	D	D	Sends Two Data Bits
1	1	0	0	0	D	D	D	Sends Three Data Bits
1	0	0	0	D	D	D	D	Sends Four Data Bits
0	0	0	D	D	D	D	D	Sends Five Data Bits

D5 : Transmit Auto Enables

When this bit is set to a one, and the Transmit Enable bit is also set, a Low on the CTS input pin will enable the transmitter. When this bit is zero, the CTS pin is simply an input to the SIO, and its status is displayed in Status Register 0.

D4 : Send Break

When set to a one, this bit immediately forces the Transmit Data output pin (TxD) to a spacing condition (continuous 0's), regardless of any data being transmitted at the time. This bit functions, whether the transmitter is enabled or not. When this bit is reset to zero, the transmitter will continue to send the contents of the transmit shift register. The shift register may contain sync characters, data characters, or all ones.

D3 : Transmitter CRC Enable

This bit determines if CRC calculations are performed on a transmitted data character. If this bit is a one at the time a character is loaded from the transmit buffer to the transmit shift register, CRC is calculated on the character. CRC is not calculated on any automatically inserted sync characters. CRC is not automatically appended to the end of a message unless this bit is set, and the Transmit Underrun/EOM status bit in Status Register 0 is reset when a Transmit Underrun condition occurs. If this bit is a zero when a character is loaded from the transmit buffer into the transmit shift register, no CRC calculations are performed on the character. This bit is ignored in Asynchronous modes.

D2 : Data Terminal Ready (DTR)

This is the control bit for the DTR output pin. When this bit is set to a one, the DTR pin goes Low : when this bit is reset to a zero, the DTR pin goes High.

D1 : Request To Send (RTS)

This is the control bit for the RTS output pin. In Synchronous modes, when this bit is set to a one, the RTS pin goes Low ; when this bit is reset to a zero, the RTS pin goes High. In Asynchronous modes, when this bit is set, the RTS pin goes Low ; when this bit is reset, the RTS pin will go High only after all the bits of the character are transmitted, and the transmit buffer is empty.

D0 : Transmitter Enable

Data is not transmitted until this bit is set to a one, until the Send Break bit is reset and, if Tx Auto Enables mode is selected, until the CTS pin is Low. To transmit sync or flag characters in Synchronous modes, this bit has to be set when the transmit buffer is empty. Data or sync characters in the process of being transmitted are completely sent if this bit is reset to zero after transmission has started. If this bit is reset during the transmission of a CRC character, sync or flag characters are sent instead of the CRC character.

STATUS REGISTER 0 (STAT 0)
READ ONLY

This register contains the status of the receive and transmit buffers and the status bits for the five sources of External/Status interrupts.

D7	D6	D5	D4	D3	D2	D1	D0
BREAK/ ABORT	UNDERRUN /EOM	CTS	HUNT/ SYNC	DCD	TX BUFR EMPTY	INTERPT PENDING	RX CHAR AVAIL

D7 : Break/Abort

This bit is reset by a channel or hardware reset. In Asynchronous modes, this bit is set when a Break sequence (null character plus framing error) is detected in the received data stream. An External/Status interrupt, if enabled, is generated when Break is detected. The interrupt service routine must issue a Reset External/Status Interrupt command (Command 2) to the SIO, so the break detection logic can recognize the termination of the Break sequence.

The Break/Abort bit is reset to a zero when the termination of the Break sequence is detected in the incoming data stream. The termination of the Break sequence also causes the generation of an External/Status interrupt. Command 2 must be issued to enable the break detection logic to look for the next Break sequence. A single extraneous null character is present in the receiver after the termination of a break ; it should be read and discarded.

In SDLC mode, this bit is set by the detection of an Abort sequence (seven or more ones) in the received data stream. The External/Status Interrupt is handled the same way as in the case of a Break sequence. The Break/Abort bit is not used in the other Synchronous modes.

D6 : Transit Underrun/EOM

This bit is set to a one following a hardware or channel reset, when the transmitter is disabled or when a Send Abort command (Command 1) is issued. This bit can only be reset by the Reset Transmit Underrun/EOM Latch command in the Command Register. This bit is used to control the transmission of

CRC at the end of a message in Synchronous modes. When a transmit underrun condition occurs and this bit is low. CRC will be appended to the end of the transmission, and this bit will be set. Only the 0-to-1 transition of this bit causes an External/Status interrupt, when enabled. This bit is not used in Asynchronous modes.

D5 : Clear To Send (CTS)

This bit indicates the inverted state of the CTS input pin at the time of the last change of any of the five External/Status bits. Any transition of the CTS input causes the CTS bit to be latched and generates an External/Status interrupt request, if enabled. To read the current state of the CTS pin, this bit must be read immediately following a Reset External/Status Interrupts command (command 2).

D4 : Hunt/Sync

In Asynchronous modes, this bit indicates the inverted state of the SYNC input pin at the time of the last change of any of the five External/Status bits. Any transition of the SYNC input causes the Hunt/Sync bit to be latched and generates an External/Status interrupt request, if enabled. To read the current state of the SYNC pin, this bit must be read immediately following a Reset External/Status Interrupt command (command 2).

In External sync mode, the SYNC pin is used by external logic to signal character synchronization is achieved, the SYNC pin is driven Low on the second rising edge of the Receive Clock (RxC) on which the last bit of the sync character was received. Once the SYNC pin is Low, it should be held Low until the end of the message and the driven back High. Both transitions on the SYNC pin cause External/Status interrupt requests, if enabled. The inverted state of the SYNC pin is indicated by this bit.

In Monosync, Bisync, and SDLC modes, this bit indicates when the receiver is in the Hunt mode. This bit is set to a one following a hardware ir channel reset, after the Enter Hunt Mode bit is written High, when the receiver is disabled, or when an Abort sequence (SDLC mode) is detected. This bit will remain in this state until character synchronization is achieved. External/Status interrupt requests will be generated on both transitions of the Hunt/Sync bit.

D3 : Data Carrier Detect (DCD)

This bit indicates the inverted state of the DCD input pin at the time of the last change of any of the five External/Status bits. Any transition of the DCD input causes the DCD bit to be latched and generates an External/Status interrupt request, if ena-bled. To read the current state of the DCD pin, this bit must be read immediately following a Reset External/Status Interrupts command (command 2).

D2 : Transmit Buffer Empty

This bit is set to a one, when the transmit buffer becomes empty, and when the last CRC bit is transmitted in Synchronous or SDLC modes. This bit is reset when the transmit buffer is loaded or while the CRC character is being sent in Synchronous or SDLC modes. This bit is set to a one following a hardware or channel reset.

D1 : Interrupt Pending

Any interrupt condition, pending in the interrupt control logic for this channel, will set this bit to a one. This bit is reset to zero by a hardware channel reset, or when all the interrupt conditions are cleared.

D0 : Receive Character Available

This bit is set to a one when a character becomes available in the receive data FIFO. This bit is reset to zero when the receive data FIFO (receive buffer) is read, or by a hardware or channel reset.

STATUS REGISTER 1 (STAT 1) READ ONLY

This register contains the Special Receive Condition status bits and the Residue codes for the I-field in the SDLC receive mode. The All Sent bit is set High, and all other bits are reset to a Low by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
END OF FRAME	CRC/ FRAME ERROR	RX OVER-RUN ERR	PARITY ERROR	RESIDUE CODE 2	RESIDUE CODE 1	RESIDUE CODE 0	ALL SENT

D7 : End Of Frame (SDLC)

This bit is used only in SDLC mode. When set to a one, this bit indicates that a valid closing flag has been received and that the CRC/Framing Error bit and Residue codes are valid. If receiver interrupts are enabled, a Special Receive Condition interrupt will also be generated. This bit can be reset by issuing an Error Reset command (command 6). This bit is also updated by the first character of the following frame. This bit is a zero in all modes except for

SDLC.

D6 : CRC/Framing Error

In Asynchronous modes, if a Framing Error occurs, this bit is set to a one for the receive character in which the framing error occurred. When this bit is set to a one, a Special Receive Condition interrupt will be requested, if receiver interrupts are enabled.

Detection of a Framing Error adds an additional one-half bit time to the character time, so that the Framing Error is not interpreted as a new start bit.

In Synchronous and SDLC modes, this bit indicates the result of comparing the received CRC value to the appropriate check value. A zero indicates that a match has occurred. This bit is usually set since most bit combinations result in a non-zero CRC, except for a correctly completed message. Receiver interrupts are not requested by the CRC Error bit.

The CRC/Framing bit is not latched in any receiver mode. It is always updated when the next character is received. An Error Reset command (command 6) will always reset this bit to zero.

D5 : Receive Overrun Error

This bit indicates that the receive data FIFO has overflowed. Only the character that has been written over is flagged with this error. When the character is read, the error condition is latched until reset by the Error Reset command (command 6). If receiver interrupts are enabled, the overrun character and all subsequent characters received, until the Error Reset command is issued, will generate a Special Receive Condition interrupt request.

D4 : Parity Error

When parity is enabled, this bit is set to a one for those characters whose parity does not match the programmed sense (even/odd). This bit is latched so that once an error occurs, it remains set until the Error Reset command (command 6) is issued. If parity is a Special Receive Condition, a Parity is a Special Receive Condition, a Parity Error will cause a Special Receive Condition interrupt request on the character containing the error and on all subsequent characters until the Error Reset command is issued.

D3, D2, D1 : Residue Codes 2, 1, and 0

In those cases of the SDLC receive mode, where the I-field is not an integral multiple of the character length, these three bits indicate the length of the residual I-field read in the previous bytes. These codes are meaningful only for the transfer in which the End Of Frame bit is set. This field is set to 000 by a channel or hardware reset and can leave this state only if SDLC mode is selected, and a character is received.

Residue Code 2	Residue Code 1	Residue Code 0	I-Field Bits In Previous Byte	I-Field Bits In Second Previous Byte
1	0	0	0	3
0	1	0	0	4
1	1	0	0	5
0	0	1	0	6
1	0	1	0	7
0	1	1	0	8
1	1	1	1	8
0	0	0	2	8

I-Fiel Bits are Right-justified in all Cases.

FOR EIGHT BITS PER CHARACTER

If a receive character length, different from eight bits, is used for the I-field, a table similar to the previous one may be constructed for each different character

Bits Per Character	Residue Code 2	Residue Code 1	Residue Code 0
8 Bits Per Character	0	1	1
7 Bits Per Character	0	0	0
6 Bits Per Character	0	1	0
5 Bits Per Character	0	0	1

length. For no residue (that is, the last character boundary coincides with the boundary of the I-field and CRC field), the Residue codes are as follows :

D0 : All Sent

This bit is only active in Asynchronous modes ; it is always High in Synchronous or SDLC modes. This bit is Low while the transmitter is sending characters : it will go High only after all the bits of the character are transmitted, and the transmit buffer is empty.

DATA REGISTER (DATARG)

The Data Register is actually two separate registers ; a write only register that is the Transmit Buffer, and a read only register that is the Receiver Buffer. The Receiver Buffer is also the top register of a three

D7	D6	D5	D4	D3	D2	D1	D0
DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0

register stack called the receive data FIFO. The Data Register is not affected by a channel or hardware reset.

TIME CONSTANT REGISTER (TCREG)

This register contains the time constant used by the down counter in the baud rate generator. The time constant may be changed at any time, but the new value does not take effect until the next time the time constant is loaded into the down counter. It is recommended that the BRG be disabled before writing to this register, as no attempt was made to

D7	D6	D5	D4	D3	D2	D1	D0
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0

synchronize the loading of a new time constant with the clock used to drive the BRG. This register is reset to ”00H” by a channel or hardware reset.

BAUD RATE GENERATOR CONTROL REGISTER (BRGCTL)

This register contains the control bits used to pro-

D7	D6	D5	D4	D3	D2	D1	D0
				RxC INT/EXT	TxC INT/EXT	DIVIDE BY 64/4	BRG ENABLE

gram the baud rate generator and to select the BRG output mode. This register is reset to ”00H” by a channel or hardware reset.

D7, D6, D5, D4 : Not Used (read as zeros)

D3 : Receiver Clock, Internal/External

This bit determines the direction of the RxC pin. When this bit is set to a one, the RxC pin is the output of the baud rate generator. If this bit is a zero, the RxC pin is an input, and an external source must supply the receiver clock. The receiver clock is always the signal on the RxC pin, except in Loop Mode, when the transmitter clock is connected internally to the receiver clock.

D2 : Transmitter Clock, Internal/External

This bit determines the direction of the TxC pin. When this bit is set to a one, the TxC pin is the output of the baud rate generator. If this bit is a zero, the TxC pin is an input, and an external source must supply the transmitter clock. The transmit clock is always the signal on the TxC pin.

D1 : Divide By 64/4

This bit specifies the minimum BRG input clock cycles to output clock cycle. This minimum occurs when the Time Constant Register is loaded with a ”01H” value. When this bit is set to a one, 64 input clocks are required for every output clock. When this bit is a zero, four input clocks are required for every output clock.

D0 : Baud Rate Generator Enable

This bit controls the operation of the baud rate generator. When this bit is set to a one, the BRG will start counting down from the value left in the down counter when this bit was last reset to zero. If the Time Constant Register is loaded while this bit is reset, the new time constant value is loaded immediately into the down counter. The baud rate generator is disabled from counting when this bit is reset.

INTERRUPT VECTOR REGISTER (VECTRG)

This register is used to hold a vector that is passed to the CPU during an interrupt acknowledge cycle. This register can also be accessed through a read/write cycle. If the Status Affects Vector bit in the Interrupt Control Register is disabled, the value programmed into the Vector Register will be passed to the CPU during an interrupt acknowledge cycle or a read cycle. If the Status Affects Vector bit in either channel is enabled, the lower three bits of this register are modified, according to the table listed in the Interrupt Control Register description. With Status Affects Vector on, and no interrupt pending in the SIO, the lower three bits will be read as 011. Only

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2 *	V1 *	V0 *

* Variable if Status Affects Vectors is Enabled.

n

e Vector Register exists in the SIO, but it can be ac-

MK68564 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Temperature Under Bias	– 25 to 100	°C
	Storage Temperature	– 65 to 150	°C
	Voltage on Any Pin with Respect to Ground	– 3 to 7	V
	Power Dissipation	1.5	W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliabi-

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	Min.	Max.	Unit.
V_{IH}	Input High Voltage ; all Inputs	V_{SS} + 2.0	V_{CC}	V
V_{IL}	Input Low Voltage ; all Inputs	V_{SS} – 0.3	V_{SS} + 0.8	V
I_{LL}	Power Supply Current ; Outputs Open		190	mA
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25)		± 10	µA
I_{TSI}	Three-state Input Current $\overline{DTACK}$, D0-D7, $\overline{SYNC}$, $\overline{TxC}$, $\overline{RxC}$ $0 < V_{IN} < V_{CC}$, $\overline{INTR}$		20 ± 10	µA µA
V_{OH}	Output High Voltage (I_{LOAD} = – 400 µA, V_{CC} = MIN) $\overline{DTACK}$, D0-D7 (I_{LOAD} = – 150 µA, V_{CC} = MIN) All Other Outputs (except XTAL2 & $\overline{INTR}$)*	V_{SS} + 2.4		V
V_{OL}	Output Low Voltage (I_{LOAD} = 5.3mA, V_{CC} = MIN) $\overline{INTR}$, $\overline{DTACK}$, D0-D7 (I_{LOAD} = 2.4mA, V_{CC} = MIN) All Other Outputs (except XTAL2)*		0.05	V

CAPACITANCE

T_A = 25°C, F = 1MHz Unmeasured Pins Returned to Ground.

Symbol	Parameter	Test Conditions	Max.	Unit.
C_{IN}	Input Capacitance $\overline{CS}$, $\overline{IACK}$ All Others	Unmeasured Pins Returned to Ground	15 10	pF pF
C_{OUT}	Tri-state Output Capacitance		10	pF

AC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5.0 VDC ± 5%, GND = 0 VDC, T_A = 0 to 70°C)

Number	Parameter	4.0 MHz		5.0 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
1	CLK Period	250	1000	200	1000	ns	
2	CLK Width High	105		80		ns	
3	CLK Width Low	105		80		ns	
4	CLK Fall Time		30		30	ns	
5	CLK Rise Time		30		30	ns	
6	$\overline{\text{CS}}$ Low to CLK High (setup time)	0		0		ns	1
7	A1-A5 Valid to $\overline{\text{CS}}$ Low (setup time)	0		0		ns	
8	DATA Valid to $\overline{\text{CS}}$ Low (write cycle)	0		0		ns	
9	$\overline{\text{CS}}$ Width High	50		50		ns	1
10	$\overline{\text{DTACK}}$ Low to A1-A5 Invalid (hold time)	0		0		ns	
11	$\overline{\text{DTACK}}$ Low to DATA Invalid (write cycle hold time)	0		0		ns	
12	$\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High (delay)		55		50	ns	
13	CLK High to $\overline{\text{DTACK}}$ Low		320		295	ns	
14	R/$\overline{\text{W}}$ Valid to $\overline{\text{CS}}$ Low (setup time)	0		0		ns	
15	$\overline{\text{DTACK}}$ Low to R/$\overline{\text{W}}$ Invalid (hold time)	0		0		ns	
16	CLK Low to DATA Out		450		450	ns	
17	$\overline{\text{CS}}$ High to DATA Out Invalid (hold time)	0		0		ns	11
18	$\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High Impedance		105		100	ns	
19	$\overline{\text{DTACK}}$ Low to $\overline{\text{CS}}$ High	0		0		ns	
20	DATA Valid to $\overline{\text{DTACK}}$ Low	70		70		ns	
21	$\overline{\text{IACK}}$ Width High	50		50		ns	1
22	$\overline{\text{IACK}}$ Low to CLK High (setup time)	0		0		ns	1
23	CLK Low to $\overline{\text{INTR}}$ Disabled		410		410	ns	2
24	CLK Low to DATA Out		330		330	ns	2
25	$\overline{\text{DTACK}}$ Low to $\overline{\text{IACK}}$, $\overline{\text{IEI}}$, High	0		0		ns	
26	$\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High	55		50		ns	
27	$\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High Impedence		105		100	ns	
28	$\overline{\text{IACK}}$ High to DATA Out Invalid (hold time)	0		0		ns	
29	DATA Valid to $\overline{\text{DTACK}}$ Low	195		195		ns	2
30	CLK Low to $\overline{\text{IEO}}$ Low		220		220	ns	3
31	$\overline{\text{IEI}}$ Low to $\overline{\text{IEO}}$ Low		140		140	ns	3
32	$\overline{\text{IEI}}$ High to $\overline{\text{IEO}}$ High		190		190	ns	4
33	$\overline{\text{IACK}}$ High to $\overline{\text{IEO}}$ High		190		190	ns	4
34	$\overline{\text{IACK}}$ High to $\overline{\text{INTR}}$ Low		200		200	ns	5
35	$\overline{\text{IEI}}$ Low to CLK Low (setup time)	10		10		ns	
36	$\overline{\text{IEI}}$ Low to $\overline{\text{INTR}}$ Disabled		425		425	ns	6
37	$\overline{\text{IEI}}$ Low to DATA Out Valid		225		225	ns	6
38	DATA Out Valid to $\overline{\text{DTACK}}$ Low	55		55		ns	6
39	$\overline{\text{IACK}}$ High to DATA Out High Impedence		120		90	ns	

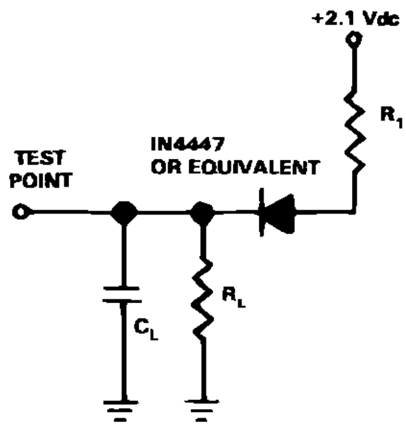
AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0 VDC ± 5%, GND = 0 VDC, T_A = 0 to 70°C)

Number	Parameter	4.0 MHz		5.0 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
40	CS HIGH TO DATA Out High Impedence		120		90	ns	
41	CS or IACK High to CLK Low	100		100		ns	7
42	TxRDY or RxRDY Width Low		3		3	CLK's	8, 10
43	CLK High TxRDY or RxRDY Low		300		300	ns	
44	CLK High to TxRDY or RxRDY High		300		300	ns	
	IACK High to CS Low or CS High to IACK Low (not shown)	50		50		ns	1
45	CTS, DCD, SYNC Pulse Width High	200		200		ns	
46	CTS, DCD, SYNC Pulse Width Low	200		200		ns	
47	TxC Period	1000	DC	800	DC	ns	9
48	TxC Width Low	180	DC	180	DC	ns	
49	TxC Width High	180	DC	180	DC	ns	
50	TxC Low to TxD Delay (X1 Mode)		300		300	ns	
51	TxC Low to INTR Low Delay	5	9	5	9	CLK's	10
52	RxC Period	1000	DC	800	DC	ns	9
53	RxC Width Low	180	DC	180	DC	ns	
54	RxC Width High	180	DC	180	DC	ns	
55	RxD to RxC High Setup Time (X1 mode)	0		0		ns	
56	RxC High to RxD Hold Time (X1 mode)	140		140		ns	
57	RxC High to INTR Low Delay	10	13	10	13	CLK's	10
58	RxC High to SYNC Low Delay (output modes)	4	7	4	7	CLK's	10
59	RESET Low	1		1		CLK	10
60	XTAL 1 Width High (TTL in)	100		80		ns	
61	XTAL 1 Width Low (TTL in)	100		80		ns	
62	XTAL 1 Period (TTL in)	250	2000	200	2000	ns	
63	XTAL 1 Period (crystal in)	250	1000	200	1000	ns	

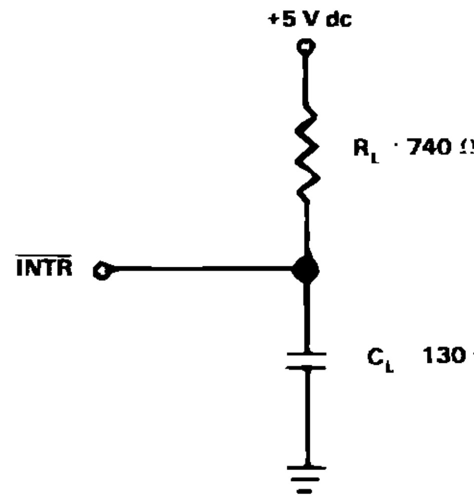
Notes :
1. This specification only applies if the SIO has completed all operations initiated by the previous bus cycle, when CS or IACK was asserted. Following a read, write, or interrupt acknoledge cycle, all operations are complete within two CLK cycles after the rising edge of CS or IACK. If CS or IACK is asserted prior to the completion of the internal operations, the new bus cycle will be postponed.
2. If IEI meets the setup time to the falling edge of CLK, 1 1/2 cycles following the clocking in of IACK.
3. No internal interrupt request pending at the start of an interrupt acknoledge cycle.
4. Time starts when first signal goes invalid (high).
5. If an internal interrupt is pending at the end of the interrupt acknoledge cycle.
6. If Note 2 timing is not met.
7. If this spec is met, the delay listed in Note 1 will be one CLK cycle instead of two.
8. Ready signals will be negated asynchronous to the CLK, if the condition causing the assertion of the signals is cleared.
9. If RxC and TxC are asynchronous to the System Clock, the maximum clock rate into RxC and TxC should be no more than one-fifth the System Clock rate. If RxC and TxC are synchronized to the falling edge of the System Clock, the maximum clock rate into RxC and TxC can be one-fourth the System Clock rate.
10. System Clock.
11. Due to the dynamic nature of the internal data bus, if CS is held low for more than a few hundred milliseconds the

Figure 13 : Output Test Load.



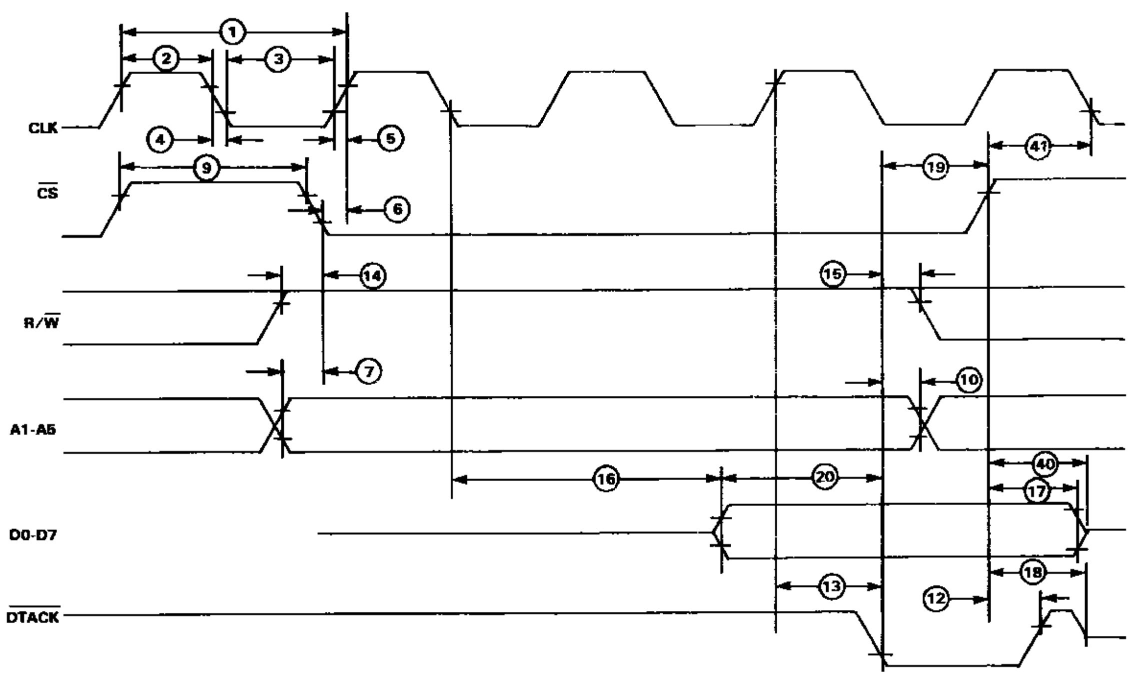
For all Outputs Except	$\overline{\text{DTACK}}$, D0-D7
	$\overline{\text{INTR}}$, XTAL2
	C_L = 130pf
	R_L = 16KΩ
	R_1 = 450Ω
for	$\overline{\text{DTACK}}$, D0-D7
	C_L = 130pf
	R_L = 6KΩ
	R_1 = 200Ω

Figure 14 : INTR Test Load.



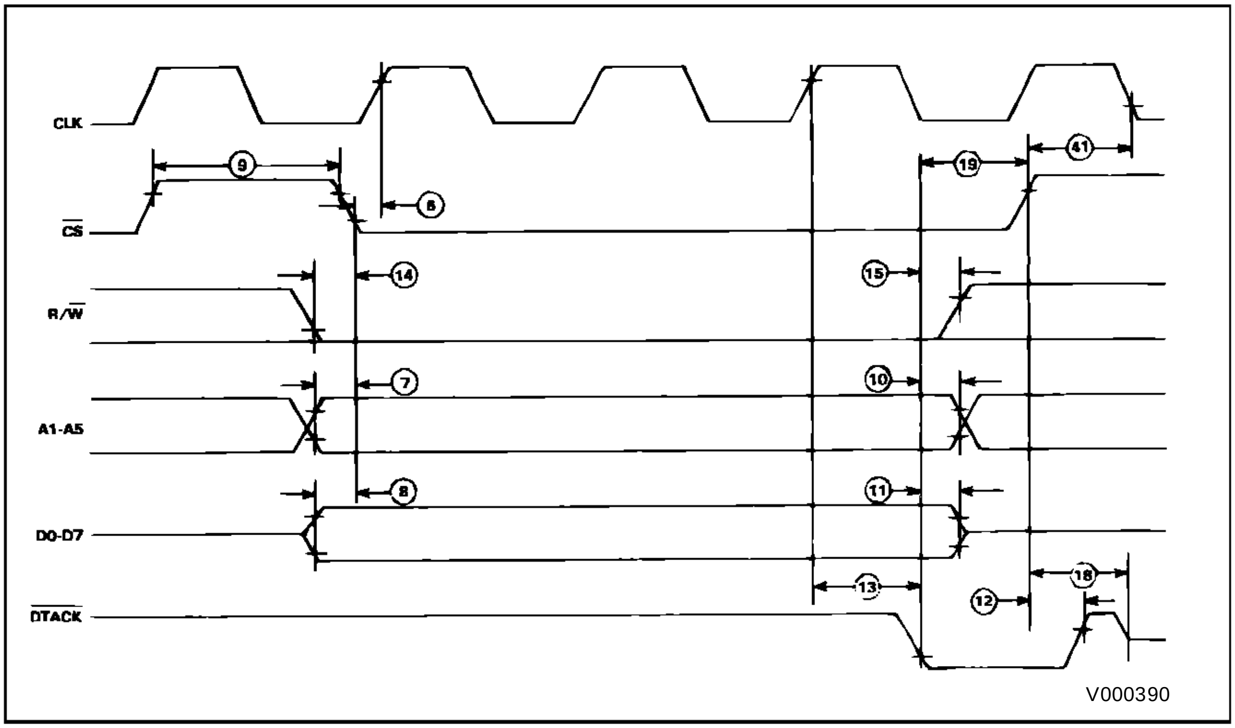
Note : XTAL2 Output Test Load is a Crystal.

Figure 15 : Read Cycle.



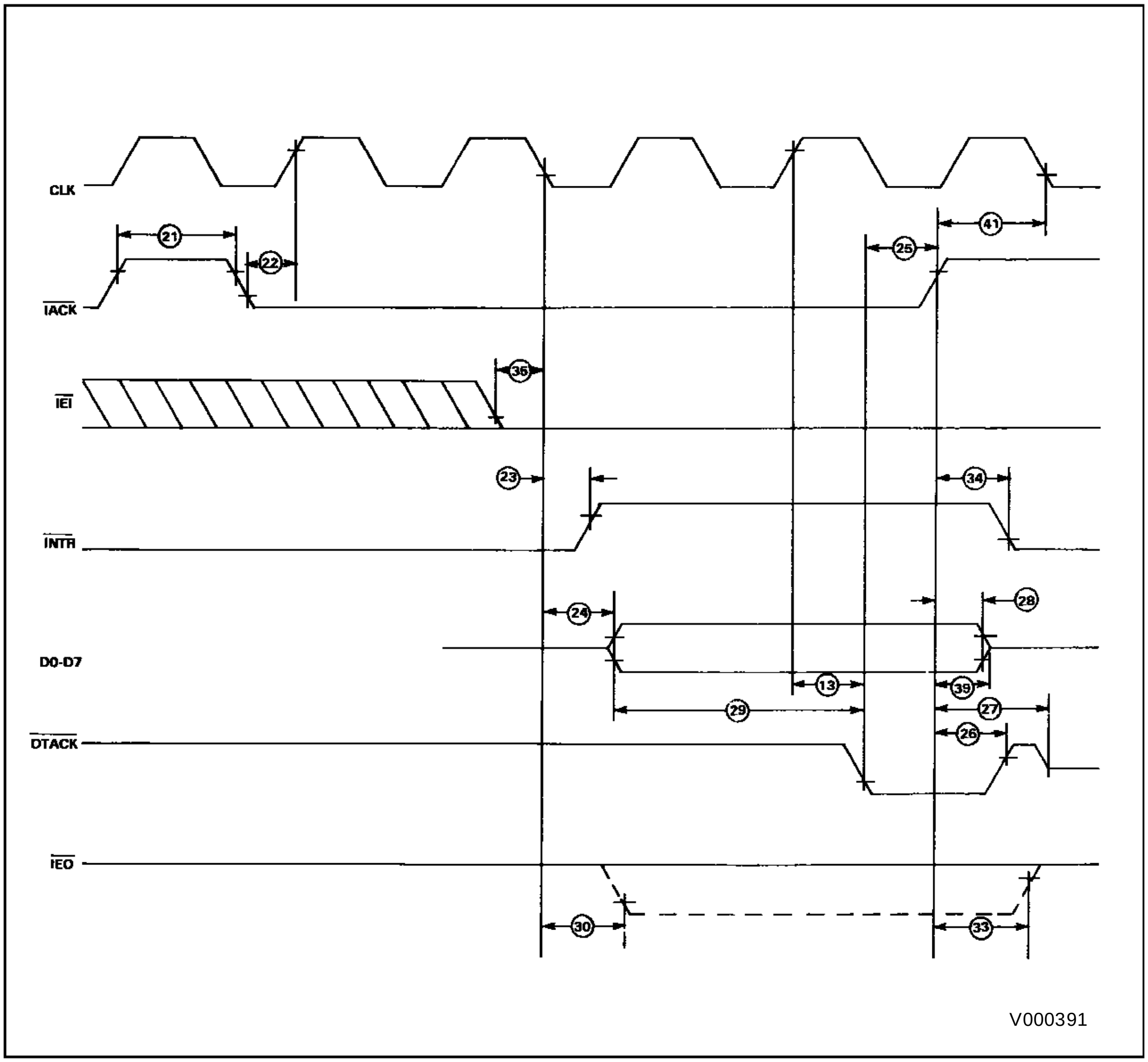
Note : Waveform Measurement for all Inputs and Outputs are Specified at Logic High = 2.0 Volts, Logic Low = 0.8 Volts.

Figure 16 : Write Cycle.



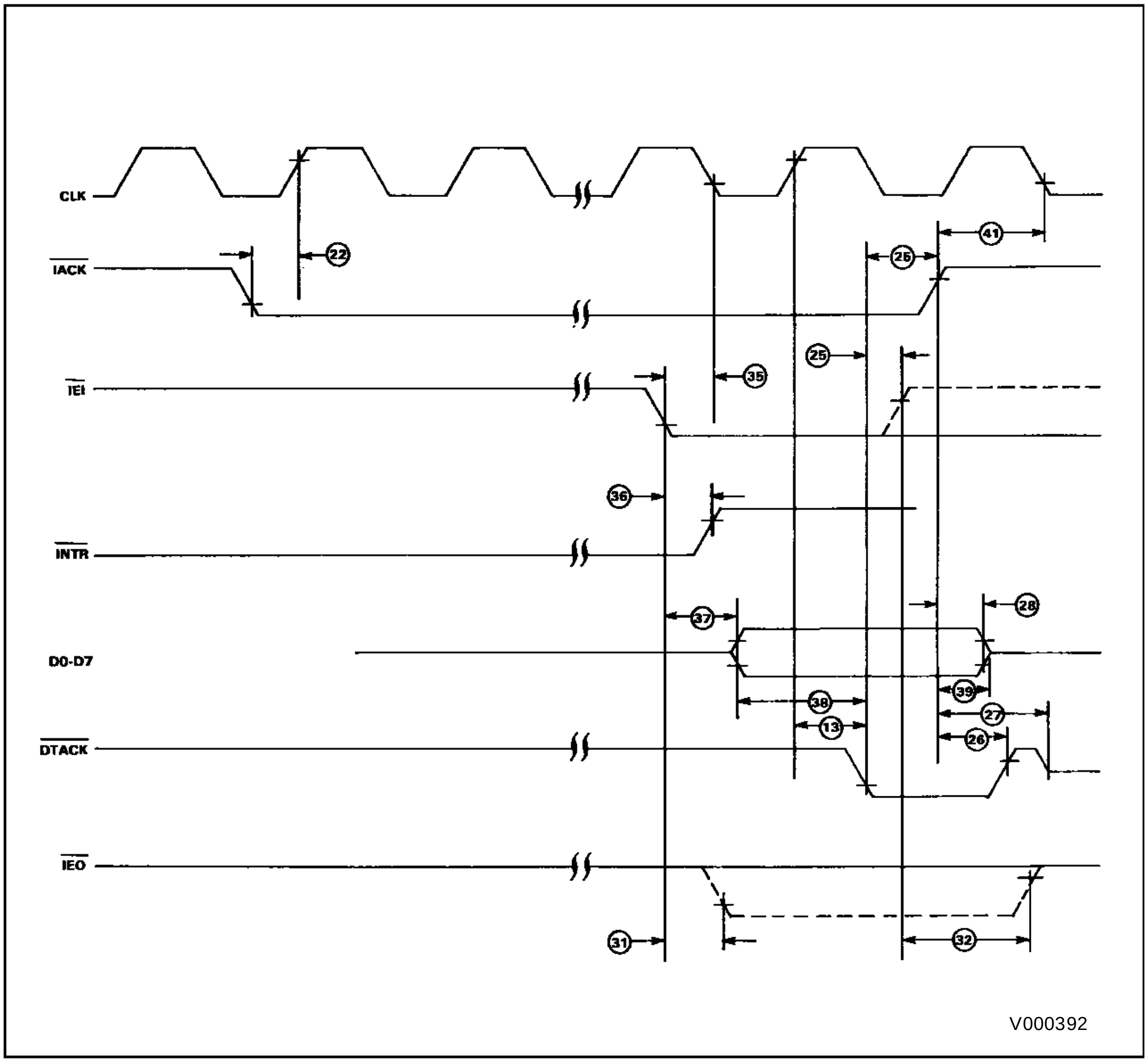
Note : Waveform Measurements for all Inputs and Outputs are Specified at Logic High = 2.0 Volts, Logic Low = 0.8 Volts.

Figure 17 : Interrupt Acknoledge Cycle ($\overline{\text{IEI low}}$).



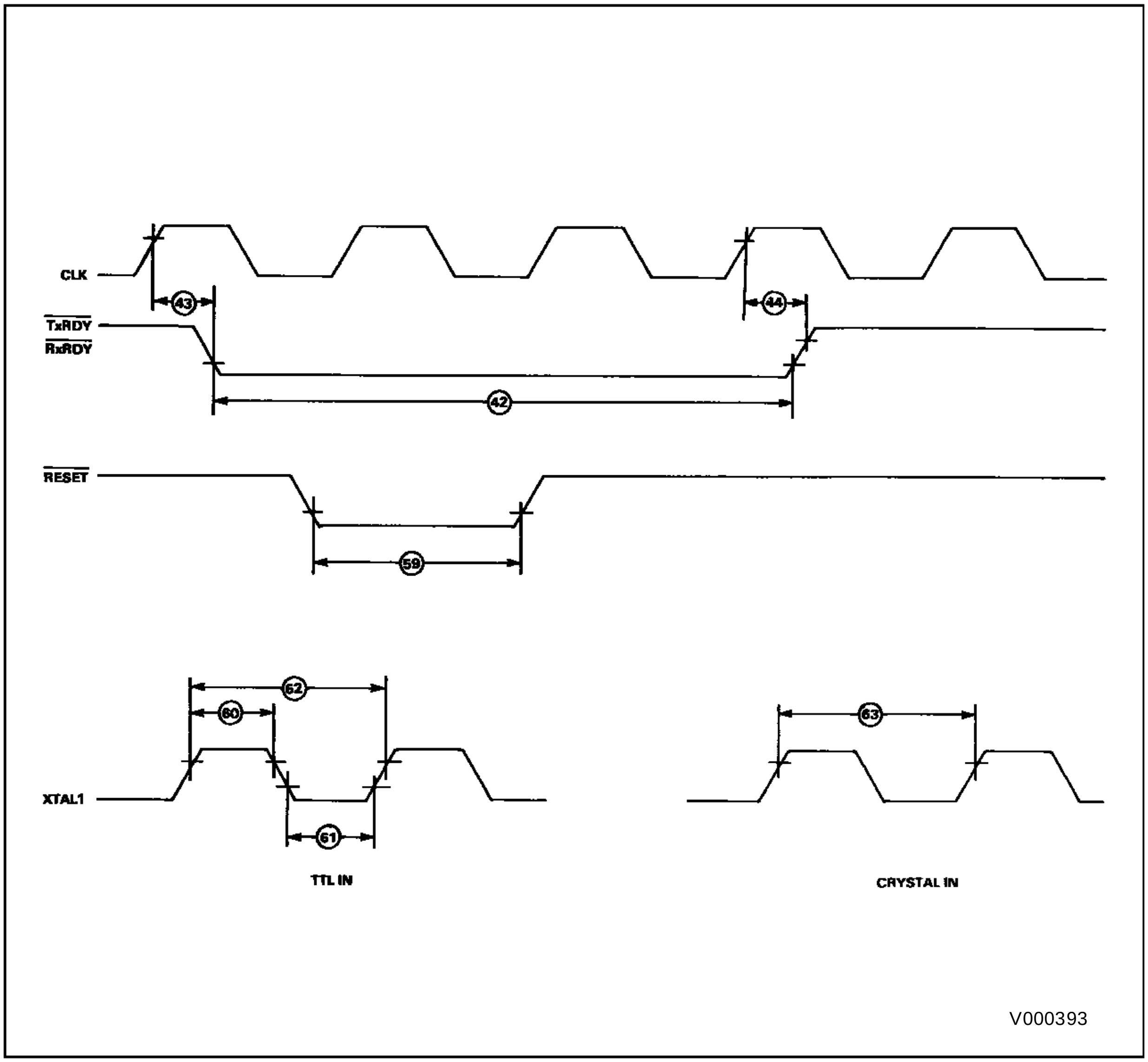
Note : Waveform Measurements for all Inputs and Outputs are Specified at Logic High = 2.0 Volts, Logic Low = 0.8 Volts.

Figure 18 : Interrupt Acknoledge Cycle ($\overline{\text{IEI}}$ high).



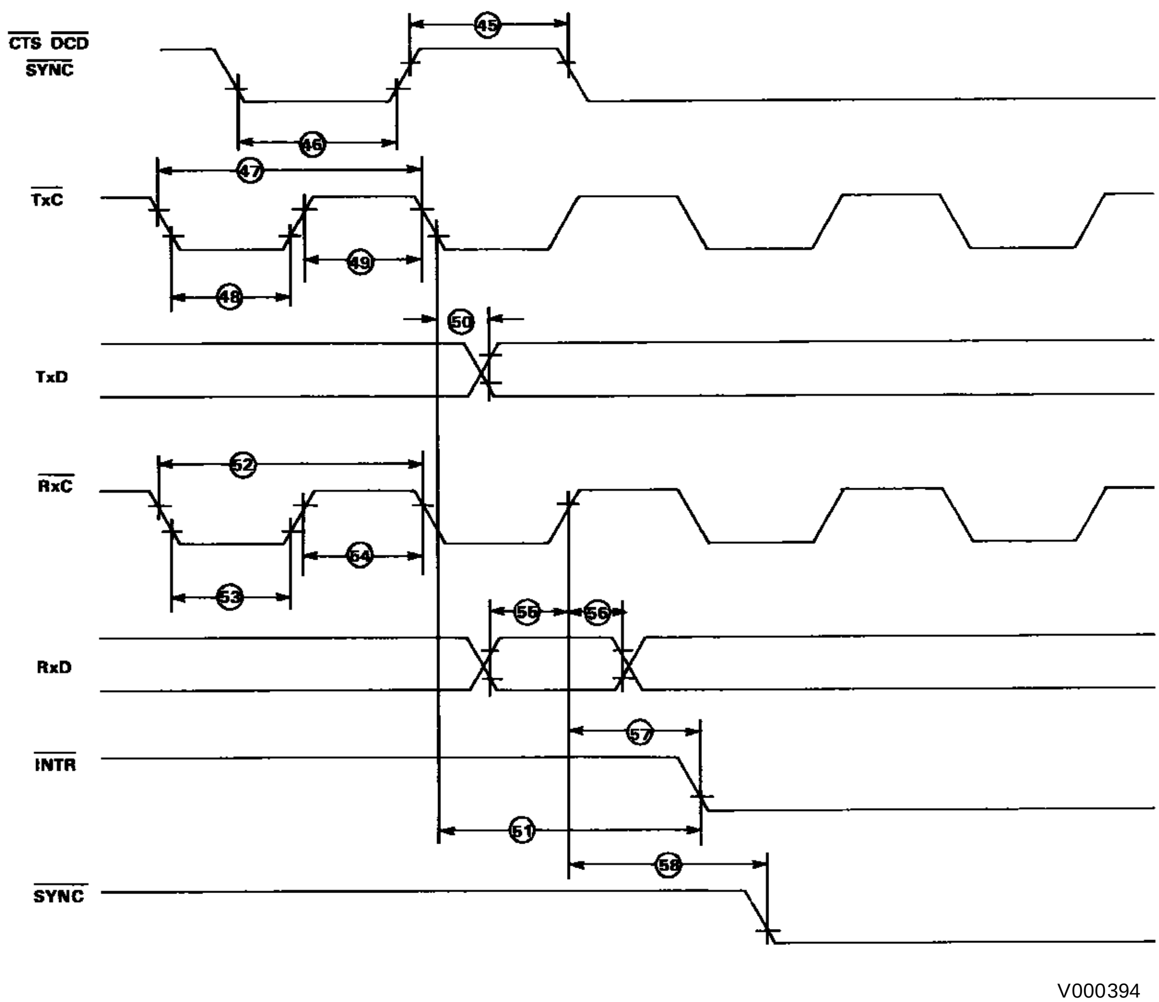
Note : Waveform Measurements for all Inputs and Outputs are Specified at Logic High = 2.0 Volts, Logic Low = 0.8 Volts.

Figure 19 : DMA Interface Timing.



Note : Waveform Measurements for all Inputs and Outputs are Specified at Logic High = 2.0 Volts, Logic Low = 0.8 Volts.

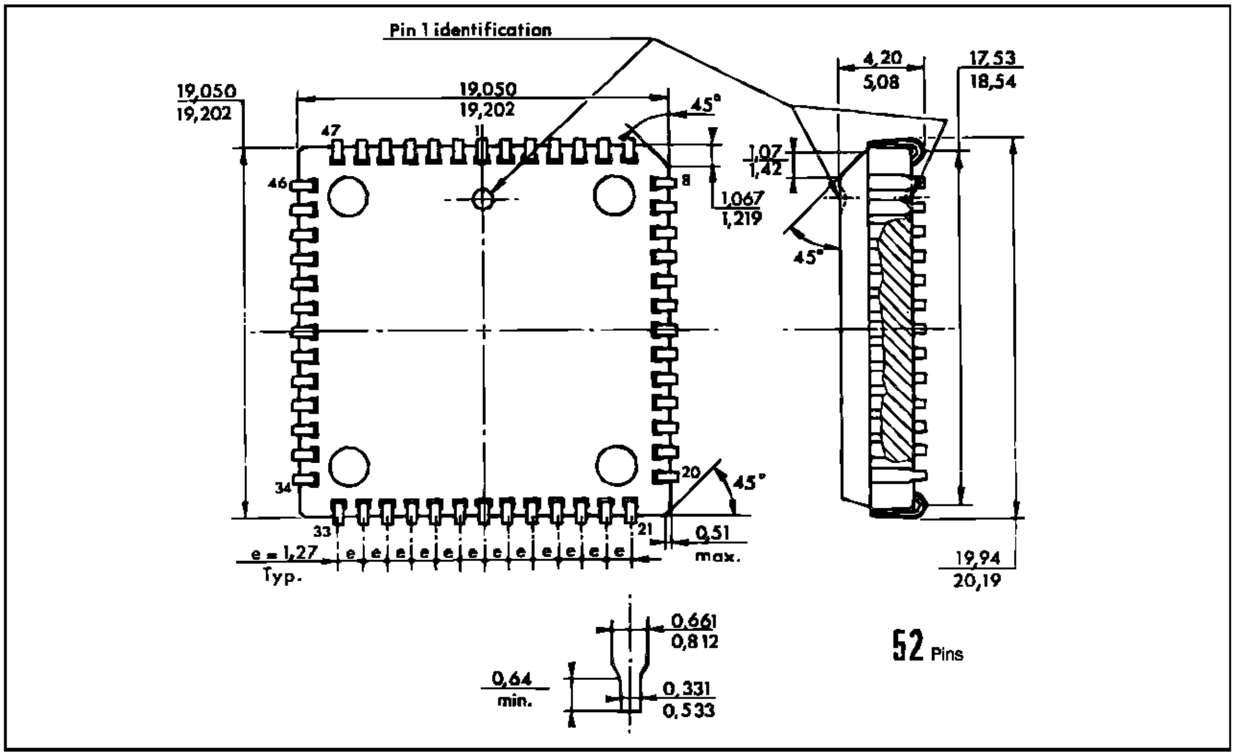
Figure 20 : Serial Interface Timing.



Note : Waveform Measurements for all Inputs and Outputs are Specified at Logic High = 2.0 Volts, Logic Low = 0.8 Volts.

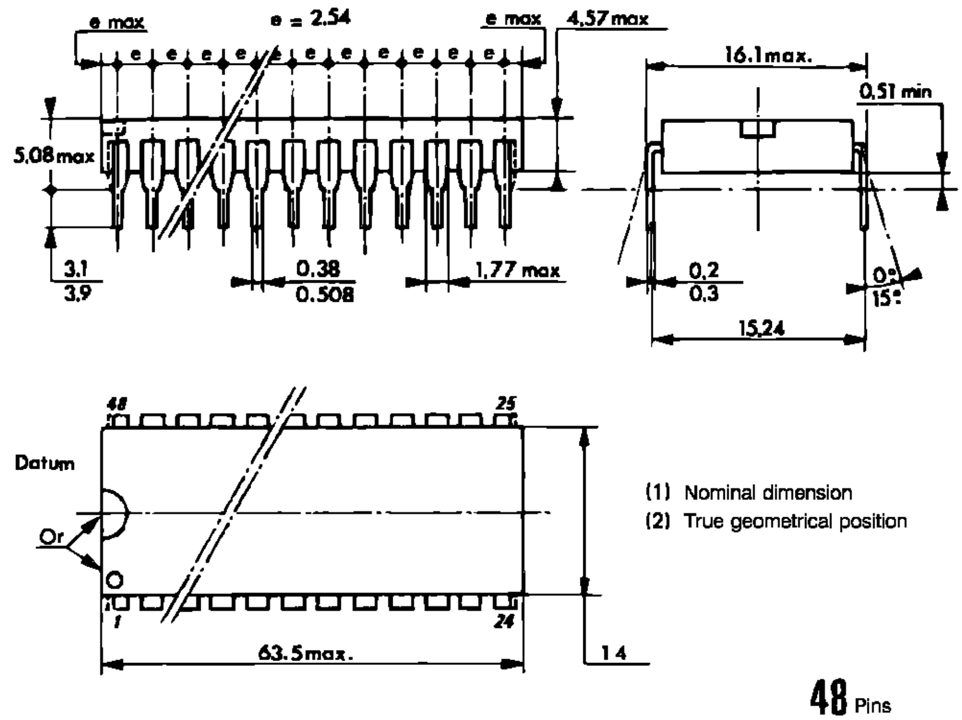
MK68564 52-PIN

Plastic Leader Chip Carrier (Q)



MK68564 48-PIN

Plastic Dual-IN-Line Package



MK68564 ORDER CODES

Part No.	Package Type	Max. Clock Frequency	Temperature Range
MK68564N-04	Plastic	4.0 MHz	0° to 70 °C
MK68564N-05	Plastic	5.0 MHz	0° to 70 °C
MK68564Q-04	PLCC	4.0 MHz	0° to 70 °C
MK68564Q-05	PLCC	5.0 MHz	0° to 70 °C