Micro Linear

ML2652/ML2653

10Base-T Physical Interface Chip

GENERAL DESCRIPTION

The ML2652, 10BASE-T Physical Interface Chip, is a complete physical interface for twisted pair and AUI Ethernet applications. It combines a 10BASE-T MAU, Manchester Encoder/Decoder, and Twisted Pair Interface filters in one monolithic IC. A complete DTE interface for twisted pair Ethernet can be implemented by combining the ML2652, an Ethernet controller, and transformers.

The ML2652 can automatically select between an AUI and twisted pair interface based on Link Pulses. Six LED outputs provide complete status at the physical link. Link pulse testing can be enabled or disabled through the LTP LED Pin.
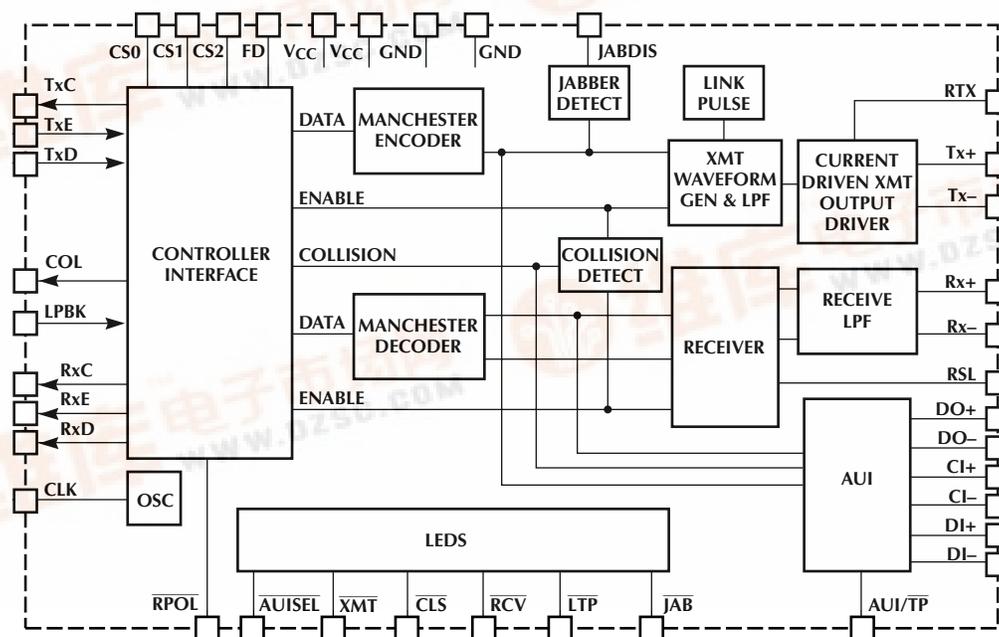
The unique transmitter design uses a waveform generator and low pass filter to meet the 10BASE-T transmitter requirements without the need for an external filter. The differential current driven output reduces common mode which in turn results in very low EMI and RFI noise.

The ML2652 and ML2653 (28 pin version) are implemented in a low power double polysilicon CMOS technology. The ML2653 does not include the AUI interface.

FEATURES

- Complete physical interface solution
- Conforms to IEEE 802.3i–1990 (10Base-T)
- On-chip transmit and receive filters
- Automatic AUI/Twisted Pair selection (ML2652 only)
- Power down mode
- Pin selectable controller interface-(CS0 – CS2)
    Intel 82586, 82596
    NSC DP8390
    Seeq 8003, 8005
    AMD 7990
- Automatic polarity correction
- Pin selectable receive squelch levels
- Status pins for: link detect, receive & transmit activity, collision, jabber, AUI selection
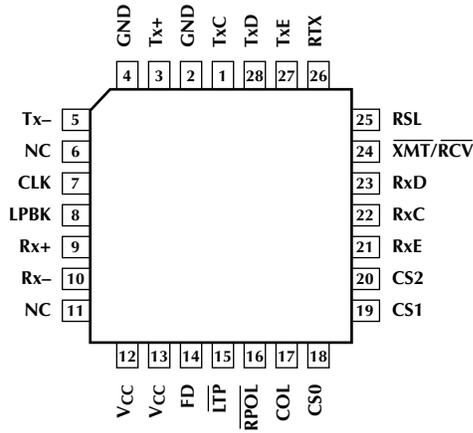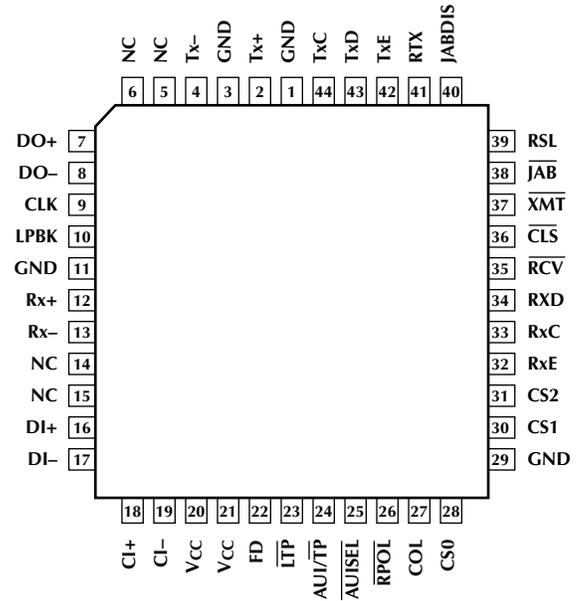- Single supply 5V ±5%

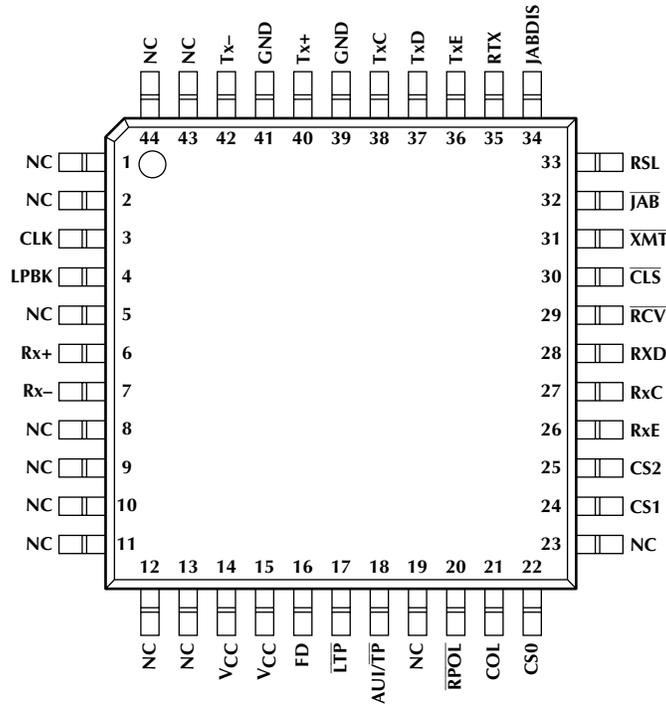## ML2652 BLOCK DIAGRAM

ML2652/ML2653

PIN CONNECTIONS

ML2653
28-Pin PLCC (Q28)

Top pins (4–26): GND, Tx+, GND, TxC, TxD, TxE, RTX
Left pins: Tx– [5], NC [6], CLK [7], LPBK [8], Rx+ [9], Rx– [10], NC [11]
Right pins: RSL [25], XMT/RCV [24], RxD [23], RxC [22], RxE [21], CS2 [20], CS1 [19]
Bottom pins (12–18): Vcc, Vcc, FD, LTP, RPOL, COL, CS0

ML2652
44-Pin PLCC (Q44)

Top pins (6–40): NC, NC, Tx–, GND, Tx+, GND, TxC, TxD, TxE, RTX, JABDIS
Left pins: DO+ [7], DO– [8], CLK [9], LPBK [10], GND [11], Rx+ [12], Rx– [13], NC [14], NC [15], DI+ [16], DI– [17]
Right pins: RSL [39], JAB [38], XMT [37], CLS [36], RCV [35], RXD [34], RxC [33], RxE [32], CS2 [31], CS1 [30], GND [29]
Bottom pins (18–28): CI+, CI–, Vcc, Vcc, FD, LTP, AUI/TP, AUISEL, RPOL, COL, CS0

ML2653
44-Pin TQFP (H44-10)

Top pins (44–34): NC, NC, Tx–, GND, Tx+, GND, TxC, TxD, TxE, RTX, JABDIS
Left pins: NC [1], NC [2], CLK [3], LPBK [4], NC [5], Rx+ [6], Rx– [7], NC [8], NC [9], NC [10], NC [11]
Right pins: RSL [33], JAB [32], XMT [31], CLS [30], RCV [29], RXD [28], RxC [27], RxE [26], CS2 [25], CS1 [24], NC [23]
Bottom pins (12–22): NC, NC, Vcc, Vcc, FD, LTP, AUI/TP, NC, RPOL, COL, CS0

ML2653 BLOCK DIAGRAM

PIN DESCRIPTION

NAME	FUNCTION
V$_{CC}$	Positive supply. +5V
GND	Ground. 0 volts. All inputs and outputs referenced to this point.
CLK	Clock input. There must be either a 20 MHz crystal or a 20 MHz clock between this pin and GND.
Tx+	Transmit positive twisted pair output. This output is a current source that drives the twisted pair cable through a pulse transformer.
Tx–	Transmit negative twisted pair output. This output is a current source that drives the twisted pair cable through a pulse transformer.
Rx+	Receive positive twisted pair input. This input receives data from the twisted pair cable through a pulse transformer.
Rx–	Receive negative twisted pair input. This input receives data from the twisted pair cable through a pulse transformer.
DO+	AUI positive transmit output. AUI transmit data output to optional external transceiver.
DO–	AUI negative transmit output. AUI transmit data output to optional external transceiver.
DI+	AUI positive receive data input from optional external transceiver.

NAME	FUNCTION
DI–	AUI negative receive data input from optional external transceiver.
CI+	AUI positive collision input from optional external transceiver.
CI–	AUI negative collision input from optional external transceiver.
RTX	Transmit current set. An external resistor between this pin and GND programs the absolute value of output current on Tx±.
TxC	Transmit clock output. Digital output which clocks the transmit data (TxD) into the device from the controller.
TxD	Transmit data input. Digital input which contains transmit data from the controller.
TxE	Transmit enable input. Digital input from the controller that indicates when the transmit data (TxD) is valid.
COL	Collision output Digital output to the controller which indicates when a collision condition is present.
RxC	Receive clock output. Digital output which clocks receive data (RxD) from the device into the controller.

PIN DESCRIPTION (Continued)

NAME	FUNCTION
RxD	Receive data output. Digital output which contains receive data sent to the controller.
RxE	Receive data valid. Digital output to the controller that indicates when the receive data (RxD) is valid.
LPBK	Local loopback. Digital input from the controller which forces the device to loopback transmit data without sending it on the media.
FD	Full Duplex Enable. When enabled the 10BASE-T MAU loopback and collision detect are disabled. LPBK must be disabled when using this function.
CS0	Controller selection input. Digital input which selects one of four standard controller timing interfaces. This pin has an internal pulldown resistor to GND.
CS1	Controller select input. Digital input which selects one of four standard controller timing interfaces. This pin has an internal pulldown resistor to GND.
CS2	Controller select input. Digital input which selects one of four standard controller timing interfaces. This pin has an internal pulldown resistor to GND.
RSL	Receive squelch level select input. Pin has internal pullup resistor to VCC. RSL = High Receive squelch level = 10Base-T RSL = Low Receive squelch level = extended distance
$\overline{\text{XMT}}$	Transmit status output. Digital output which indicates data transmission on Tx+ and Tx−. Pin is open drain output with resistor pullup and is capable of driving an LED. $\overline{\text{XMT}}$ pin and $\overline{\text{RCV}}$ pin are the same pin for the ML2653.
$\overline{\text{RCV}}$	Receive status output. Digital output which indicates unsquelched data reception on Rx+ and Rx−. Pin is an open drain output with resistor pullup and is capable of driving an LED.

NAME	FUNCTION
$\overline{\text{CLS}}$	Collision status output. Digital output which indicates that collision condition has been detected. Pin is an open drain output with resistor pullup and is capable of driving an LED.
$\overline{\text{LTP}}$	Link test pass output/input. This pin consists of an open drain output transistor with a resistor pullup that serves both as a link test pass output and a link test disable input. When used as an output, this pin is capable of driving an LED. $\overline{\text{LTP}}$ = High, link test failed $\overline{\text{LTP}}$ = Low, link test pass $\overline{\text{LTP}}$ = GND, link test disabled
AUI/$\overline{\text{TP}}$	AUI/twisted pair interface select input. AUI/$\overline{\text{TP}}$ = High, AUI selected AUI/$\overline{\text{TP}}$ = Low, TP selected
$\overline{\text{RPOL}}$	This pin must be grounded at all times.
$\overline{\text{JAB}}$	Jabber detect output. Digital output which indicates that the jabber condition has been detected. Pin is an open drain output with resister pullup and is capable of driving a LED. $\overline{\text{JAB}}$ = High, normal $\overline{\text{JAB}}$ = Low, jabber detected
$\overline{\text{AUISEL}}$	AUI/$\overline{\text{TP}}$ port output status $\overline{\text{AUISEL}}$ = High, TP port selected $\overline{\text{AUISEL}}$ = Low, AUI port selected
JABDIS	Jabber disable input JABDIS = High, jabber disabled JABDIS = Low, normal operation
NC	No connect. Leave this pin open circuit.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to GND. (Note 1)

V_{CC} supply voltage .... +6.5V
All inputs and outputs .... −0.3V to V_{CC} + 0.3V
Input current per pin .... ±25 mA
Power dissipation .... 0.75 Watt

Storage temperature range .... −65°C to 150°C
Junction Temperature .... 150°C
Lead temperature (soldering, 10 sec) .... 260°C
Thermal Resistance (θ_{JA})
    28-Lead PLCC .... 60°C/W
    44-Lead PLCC .... 54°C/W
    44-Lead TQFP .... 67°C/W

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified T_A = 0°C to 70°C, V_{CC} = 5V +5%. Note 2 & 3.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIL	Digital input low voltage	All except CLK CLK			.8 1.5	V V
VIH	Digital input high voltage	All except CLK CLK	2.0 3.5			V V
IIL	Digital input low current	VIN=GND TxD, TxE, AUI/$\overline{\text{TP}}$ VIN=GND LPBK, CS2–0, LBDIS,JABDIS VIN=GND RSL VIN=GND $\overline{\text{LTP}}$, RPOL, VIN=GND CLK	−10 −15	−25 −250	−5 −5 −50 −500 −300	µA µA µA µA µA
IIH	Digital input high current	VIN=VCC TxD, TxE, AUI/$\overline{\text{TP}}$ VIN=VCC LPBK, CS2–0, LBDIS, JABDIS VIN=VCC RSL VIN=VCC $\overline{\text{LTP}}$, RPOL VIN=VCC CLK	10	25	1 50 1 1 250	µA µA µA µA µA
CIN	Digital input capacitance	All except CLK CLK		5 10		pF pF
VOL	Digital output low voltage	IOL=−2mA TxC, COL, RxC, RxD, RxE IOL=−10mA $\overline{\text{XMT}}$, $\overline{\text{RCV}}$, $\overline{\text{CLS}}$, $\overline{\text{LTP}}$, RPOL, $\overline{\text{JAB}}$			.4 .6	V V
VOH	Digital output high voltage	IOH=2mA TxC, COL, RxC, RxD, RxE IOL=10uA $\overline{\text{XMT}}$, $\overline{\text{RCV}}$, $\overline{\text{CLS}}$, $\overline{\text{LTP}}$, RPOL, $\overline{\text{JAB}}$	4.0 2.4			V V
ICC	VCC supply current	TX transmission No transmission Powerdown mode		 2	140 105	mA mA mA
TOV	Tx± differential output voltage	RTX = 10K	2.2	2.5	2.8	Vp
THD	Tx± harmonic distortion	TxD=all ones	−27			dB
TCM	Tx± common mode output voltage				± 50	mVp
TCMR	Tx± common mode rejection	VCM=15vp, 10.1 MHz sine		± 100		mVp
TOVI	Tx± differential output voltage during idle				± 50	mVp
TOIA	Tx± output current accuracy	RTX=10K		50		mA
TRO	Tx± output resistance			1		Mohm
TCO	Tx± output capacitance			10		pF

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ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RRI	Receive input resistance		2.5K	10K		ohms
RCI	Receive input capacitance			10		pF
RSON	Receive squelch on level (Differential zero to peak voltage)	RSL=1 RSL=0	275 150		520 325	mVp mVp
RSOF	Receive squelch off level (Differental zero to peak voltage)	RSL=1 RSL=0	150 100		325 225	mVp mVp
DOV	DO± differential output voltage		± 550		± 1170	mV
DOVI	DO± differential output voltage during idle				± 40	mV
DOUS	DO±differential output voltage return to 0 undershoot				−100	mV
DOCMA	DO± common mode AC output voltage				± 40	mV
DOCMA	DO± common mode DC output voltage			VCC *.5		V
DIRI	DI/CI input resistance		2.5K	10K		ohms
DICI	DI/CI input capacitance			10		pF
DIBV	DI/CI input bias voltage	DI/CI floating		VCC *.5		V
DISON	DI/CI squelch on level		−175		−325	mVp
t1	TxC on time		45		55	ns
t2	TxC off time		45		55	ns
t3	TxC period			100		ns
t4	TxE setup time		25			ns
t5	TxE hold time		0			ns
t6	TxD setup time		25			ns
t7	TxD hold time		0			ns
t8	Transmit propagation delay	Tx± DO±		60	200 200	ns ns

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t9	Start of Idle Pulse Width	Tx± DO±	200		350	ns
t10	SOI pulse width to within 40mV of final value	Tx± DO±			4500 8000	ns ns
t11	Transmit output jitter	Tx± DO±			± 8.0 ± .5	ns ns
t12	Transmit output rise and fall time	Tx± , 10–90%		5		ns
t13	TxE to $\overline{XMT}$ assert				250	ms
t14	$\overline{XMT}$ blinker pulse period		95		115	ms
t15	$\overline{XMT}$ duty cycle		45		55	%
t20	Start of receive packet to RxE assert	Rx± DI±			600 200	ns ns
t21	Start of receive packet to RxC active	Rx+ DI+			1600 1300	ns ns
t22	RxC on time		45		900	ns
t23	RxC off time		45		55	ns
t24	RxD valid before RxC		45			ns
t25	RxD valid after RxC		35			ns
t26	RxE assert to $\overline{RCV}$ assert				250	ms
t27	$\overline{RCV}$ blinker pulse period		95		115	ms
t28	$\overline{RCV}$ duty cycle		45		55	%
t29	Receive input jitter	Preamble Data			± 12 ± 18	ns ns
t30	Receive propagation delay	Tx± DI±			160 160	ns ns
t31	RxC to RxE assert		30		60	ns
t32	RxC to RxE deassert		20		45	ns
t33	RxE deassert to RxC switchover		100		200	ns

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t34	Minimum SOI pulse width required for receive detection	Tx± DI±	180 180			ns ns
t40	Jabber activation delay- TxE assert to Tx± disable		20		150	ms
t41	Tx± disable to $\overline{JAB}$ assert			200		ms
t42	Jabber reset time – TxE deassert to $\overline{JAB}$ deassert		250		750	ms
t43	Tx± disable to COL assert			50		ns
t44	Tx± disable to $\overline{CLS}$ assert			50		ns
t45	$\overline{JAB}$ deassert to COL deassert				50	ns
t46	$\overline{JAB}$ deassert to $\overline{CLS}$ deassert				50	ns
t51	Transmit link pulse period		8		24	ms
t52	Minimum link pulse period required for receive detection		2		7	ms
t52	Maximum link pulse period required for receive detection		25		150	ms
t53	Receive link pulse no detect to $\overline{LTP}$ deassert		50		150	ms
t54	Receive link pulse detect to $\overline{LTP}$ assert		2			Link Pulse
t55	AUI/$\overline{TP}$ to $\overline{AUISEL}$ delay				200	ns
t60	TxE deassert to COL assert		.9	1.0	1.1	µs
t61	COL pulse Width		.9	1.0	1.1	µs
t70	Start of $\overline{RCV}$ packet during transmission to COL assert	Rx±			500	ns
t71	Start of $\overline{RCV}$ packet during transmission to $\overline{CLS}$ assert	Rx±			500	ns
t72	End of $\overline{RCV}$ packet during transmission to COL deassert	Rx±			300	ns
t73	$\overline{CLS}$ blinker pulse period		95		115	ms
t74	$\overline{CLS}$ duty cycle		45		55	%

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t75	Transmission start during reception to COL assert	Tx±			300	ns
t76	Transmission start during reception to $\overline{\text{CLS}}$ assert	Tx±			250	ns
t77	CI± period		80		120	ns
t78	CI± duty cycle		40		60	%
t79	First valid negative CI± data transition to COL assert				100	ns
t80	First valid negative CI± data transition to $\overline{\text{CLS}}$ assert				100	ns
t81	Last CI± positive data transition to COL deassert		160		250	ns
t82	External clock input jitter				50	ps

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Low Duty cycle pulse testing is performed at T_A.

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TIMING DIAGRAMS (Continued)
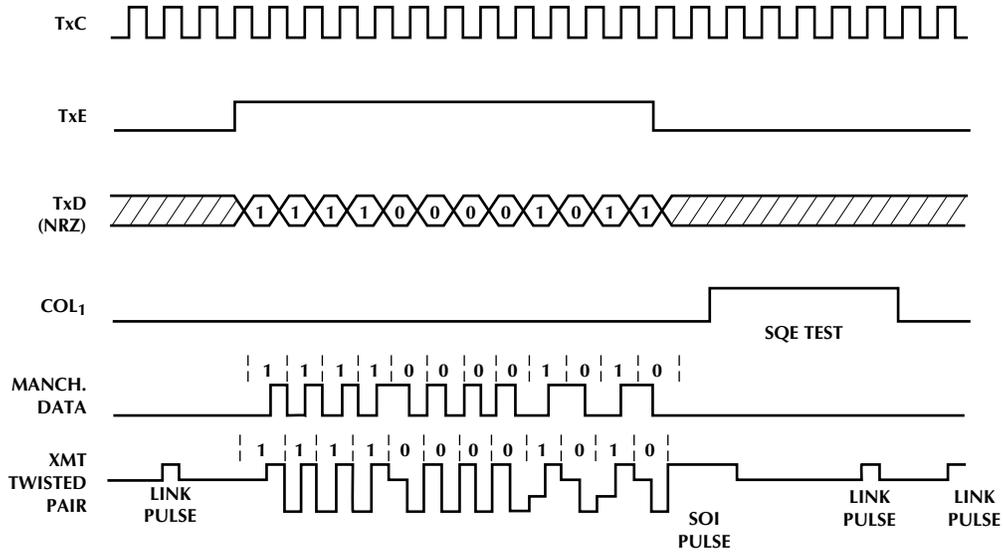
Figure 1. Transmit System Timing
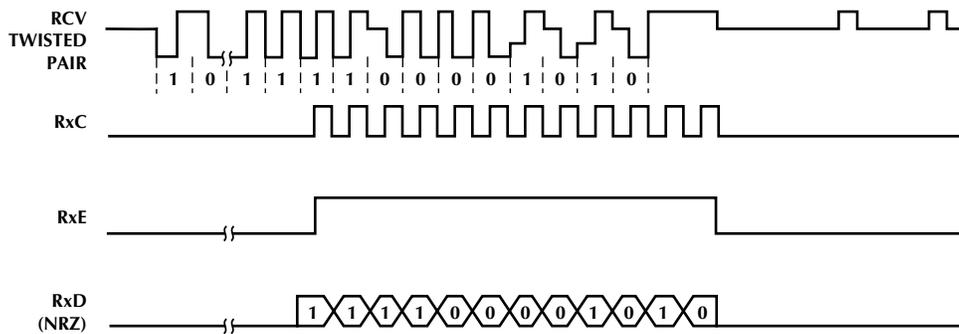
Figure 2. Receive Timing

TIMING DIAGRAMS (Continued)
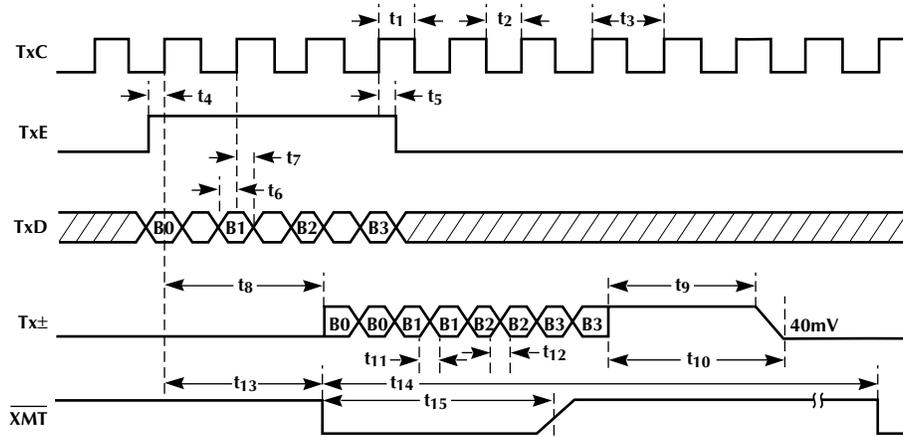
Figure 3. Transmit Timing
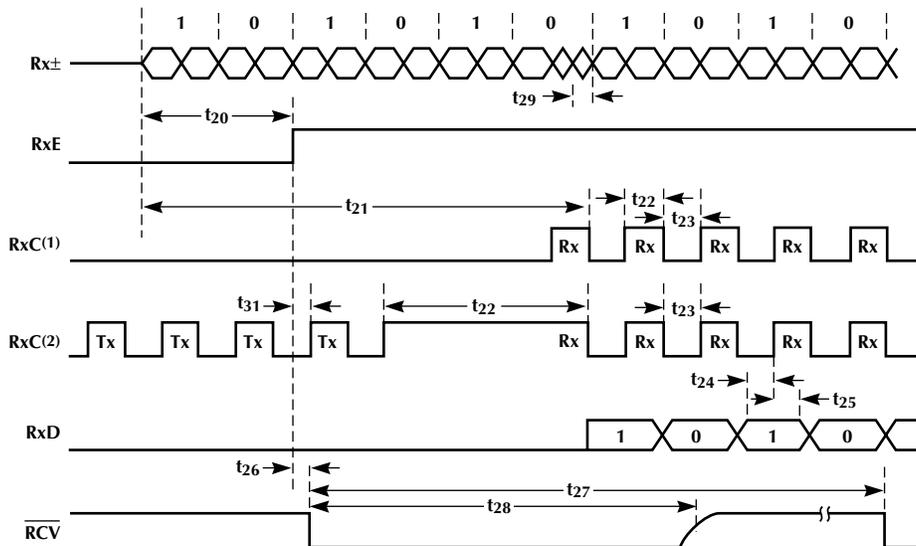
NOTE:
1. RxC IS NOT CONTINUOUS DURING IDLE
2. RxC IS CONTINUOUS DURING IDLE

Figure 4. Receive Timing – Start of Frame

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TIMING DIAGRAMS (Continued)
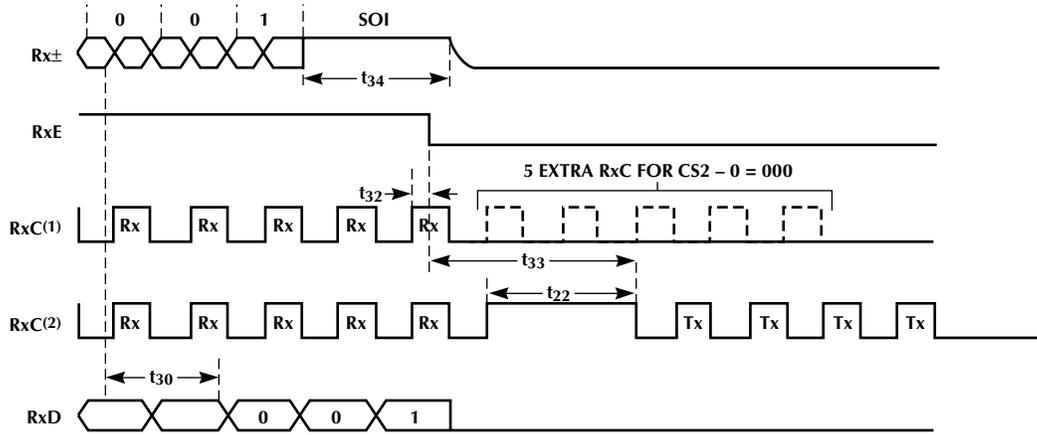
NOTE:
1. RxC IS NOT CONTINUOUS DURING IDLE — 8 EXTRA CLOCKS ADDED FOR CS2 – 0 = 000
2. RxC IS CONTINUOUS DURING IDLE

Figure 5. Receive Timing – End of Frame
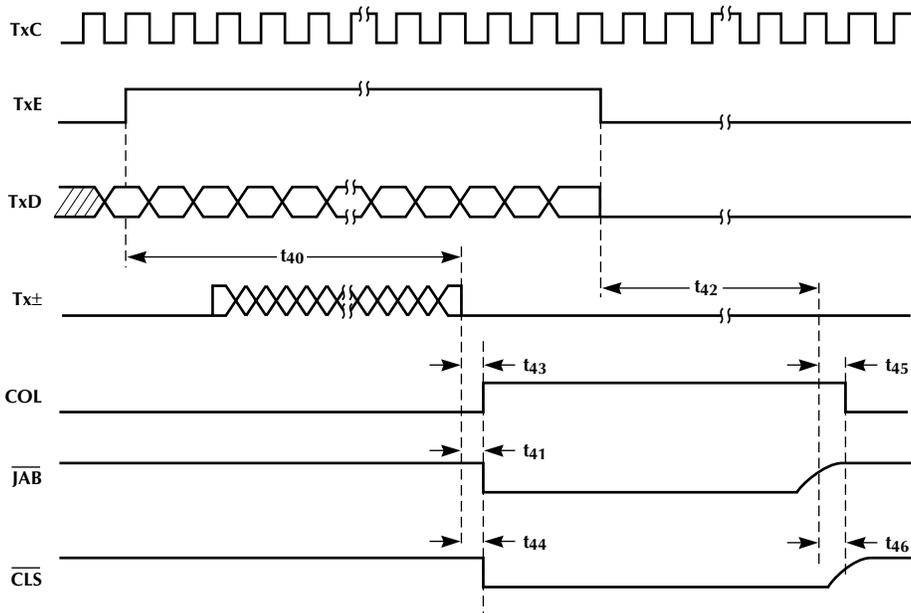
Figure 6. Jabber Timing (ML2652 only.)

TIMING DIAGRAMS (Continued)
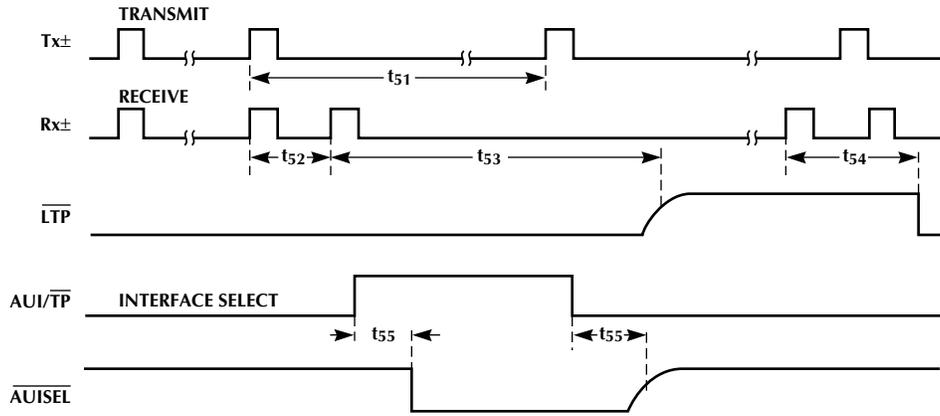
Figure 7. Link Pulse Timing
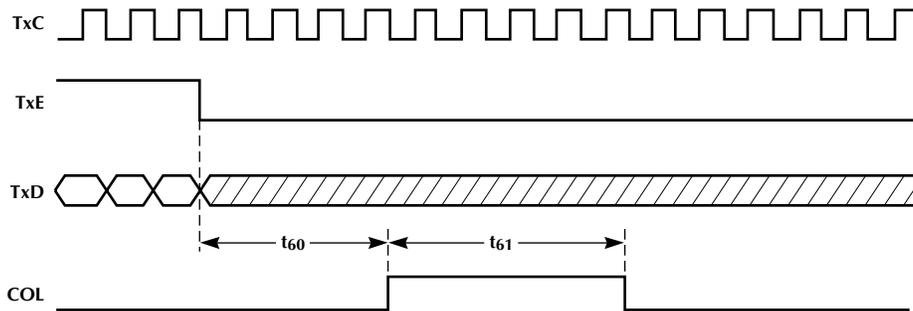
Figure 8. SQE Test Timing

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TIMING DIAGRAMS (Continued)

DATA MAY BE INVALID
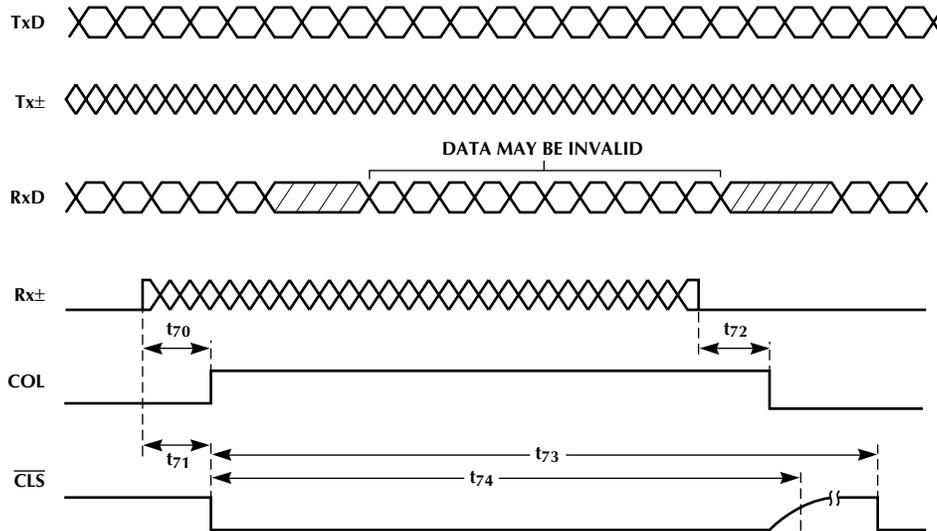
Figure 9. Collision Timing Reception During Transmission
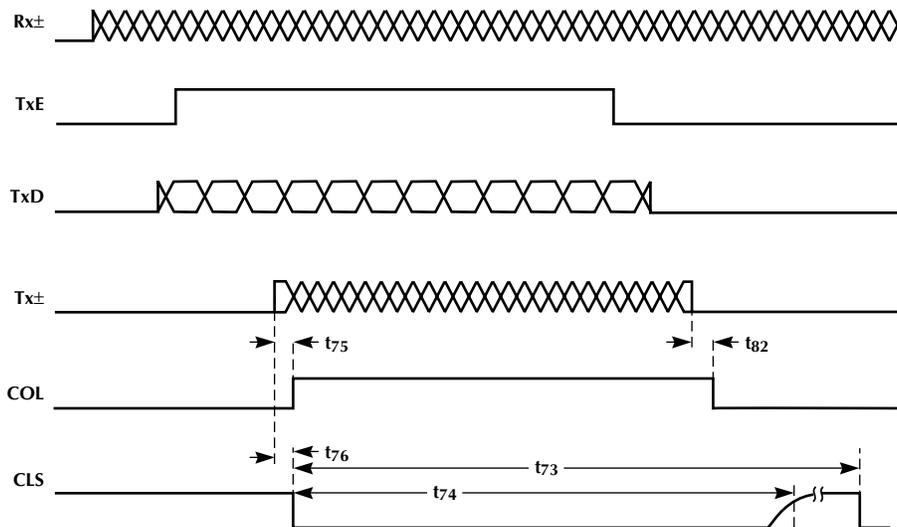
Figure 10. Collision Timing Transmission During Reception

TIMING DIAGRAMS (Continued)
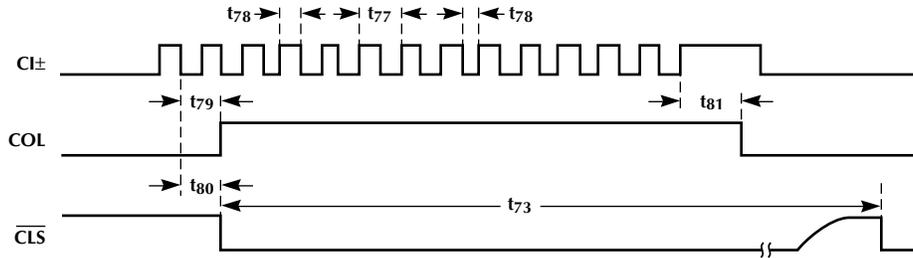
Figure 11. CI± Collision

APPLICATION CIRCUIT — ML2652
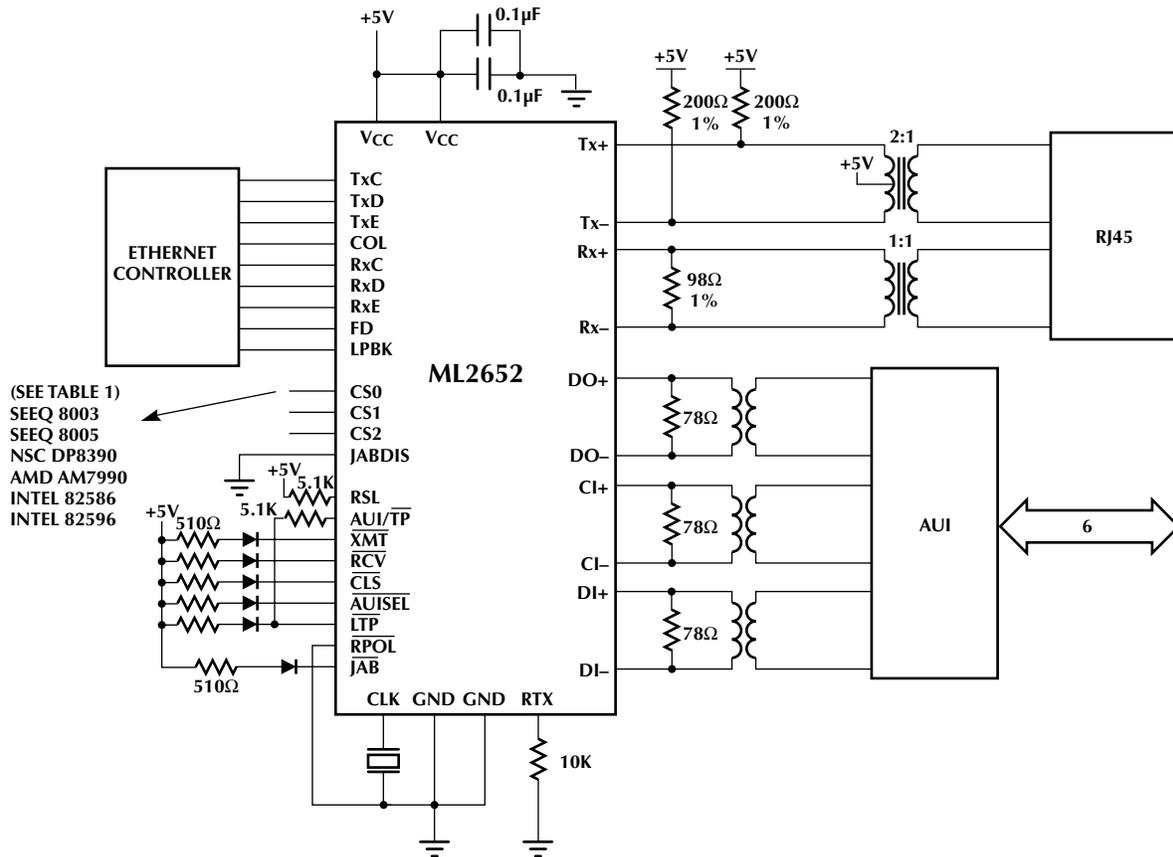
Figure 12

FUNCTIONAL DESCRIPTION

GENERAL

The ML2652 and ML2653 are composed of a transmitter section, receive section and some miscellaneous functions.

The transmit section consists of the manchester encoder, AUI, jabber detect, link pulse generator, start of idle (SOI) pulse generator, waveform generator, and line driver. The purpose of the transmit section is to take data from the controller, encode it, and transmit it over either the AUI or twisted pair interface. In addition, the transmit section generates link pulses, start of idle pulses, and checks for jabber condition. The transmitter keeps the data jitter to a maximum of ±8.0ns, and the maximum delay through the transmission section is less than 2 bits, or 200ns.

The receive section consists of the manchester decoder, collision detect, AUI, receive LPF, receive comparators, receive squelch, automatic polarity correct, start of idle (SOI) detect, and link pulse detect. The purpose of the receive section is to take data from either the twisted pair cable or AUI, decode it, then send the data to the

controller via the controller interface. In addition, the receive section detects and automatically corrects for reverse polarity, detects link pulses, detects start of idle pulses, and implements an intelligent receive squelch algorithm. The receive section can successfully lock onto an incoming data that contains ±18ns of jitter in less than 1.6µs.

The miscellaneous functions are the controller interface, single pin crystal oscillator, AUI, loopback modes, test mode, and powerdown mode. The ML2653 has no AUI interface output.

The following text describes each of these blocks and functions in more detail. Refer to the block diagram.

TRANSMISSION

The transmit data (NRZ) is first clocked into the device through the controller interface. The device can be digitally programmed to accommodate any one of four standard Ethernet controllers as described in Controller section.
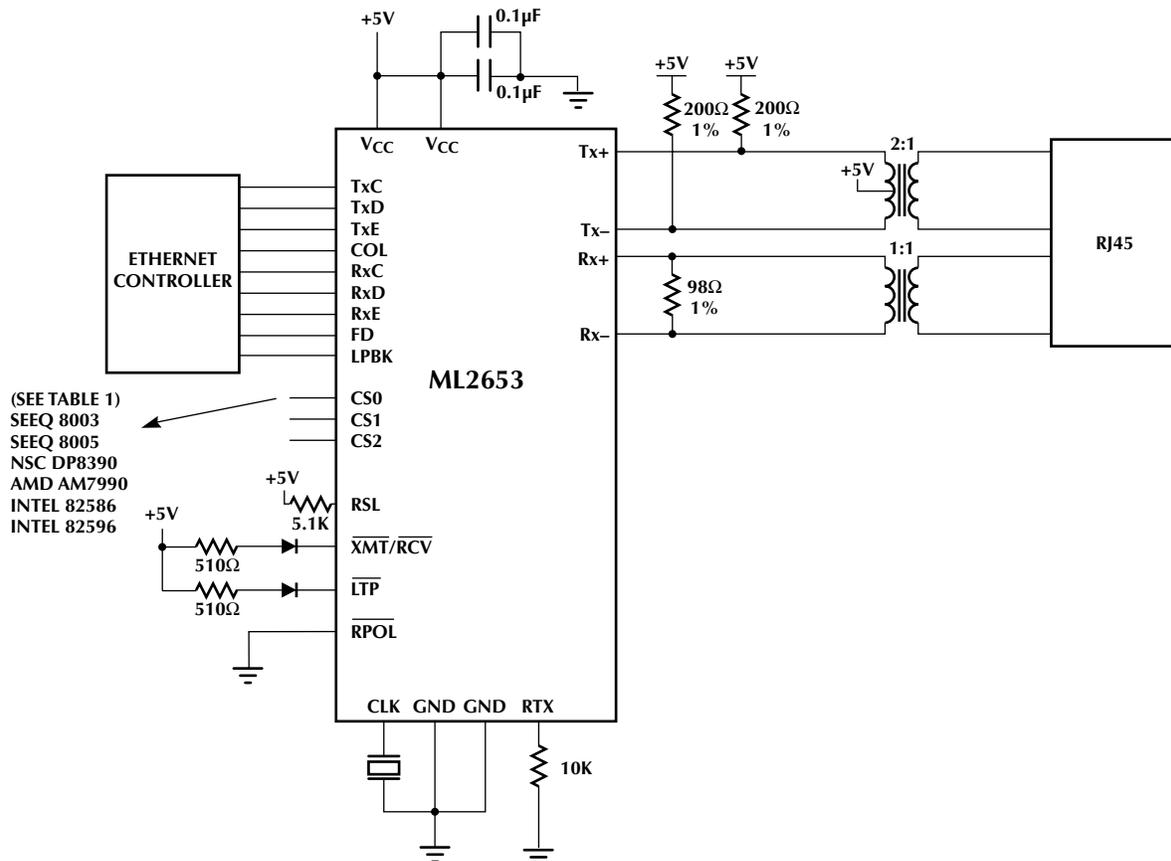
APPLICATION CIRCUIT — ML2653

Figure 13

FUNCTIONAL DESCRIPTION (Continued)

Then the NRZ data is encoded by the manchester encoder as shown in transmit timing diagram in Figure 1.

The manchester encoded data then goes to either the AUI or twisted pair interface. The selection of the appropriate interface is automatic. If the AUI is selected, the manchester encoded data is transmitted out differentially on the DO+ and DO– pins, and the twisted pair line driver is disabled. If the twisted pair interface is selected, the manchester encoded data is transmitted out differentially on Tx+ and Tx– pins, and the transmit AUI is disabled.

Refer to the AUI section for details on how the AUI and automatic interface selection is accomplished.

Assuming that the twisted pair interface is selected, the Manchester encoded data then goes to the transmit waveform generator. The transmit waveform generator takes the digital Manchester encoded data and generates a waveform. When this waveform is passed through the cable model in the 10BASE-T standard (figure 14–7 IEEE Std 802.3i–1990) it meets the voltage template (figure 14–9 IEEE Std 802.3i–1990).

The transmit waveform generator is composed of a 16 x 4 bit ROM, 4 bit DAC, 3rd order LPF, and clock generator. The DAC is used to synthesize a stair-step representation of a signal that will meet the required output template. The ROM stores the digital representation of the output signal and provides a digital input to the DAC. The ROM is addressed by a 16 phase clock generator that is locked to the transmit clock TxC. The high frequency content present in the output of the DAC is removed by a 3rd order continuous LPF which smooths the output.

The transmit line driver takes the output of the waveform generator and converts this voltage to a differential output current on Tx+ and Tx– pins. When one transmit output (either Tx+ or Tx–) is sinking current, the other output is high impedance, and vice versa. In this way, a differential output voltage is developed by sinking this output current through two external 200 ohm terminating resistor and a 2:1 transformer as shown in Figure 12.

Setting the external terminating resistors to 200 ohms as shown in Figure 12 will implement a 100 ohm terminating impedance when looking back through the transformer. If other terminating impedances are required (such as 150 ohm), the terminating resistor values can be adjusted accordingly as long as the output current stays within the minimum and maximum limits (30–70mA).

The absolute value of the output current, and subsequently the output voltage level, is set by an external resistor between RTX and GND. If RTX = 10k ohms and Tx± is terminated as shown in Figure 12, the output level is ±2.5V which meets 802.3i–1990 differential output voltage requirements. If a different output current/voltage level is desired, the level can be changed by changing the value of RTX according to the following formula:

$$RTX = K*Vb/Iout$$

$$= 125*4v/50mA$$

$$RTX = 10k\Omega$$

When data is being transmitted (and there is no collision or link pulse fail condition), the transmit data is looped back to the receive path, and the Manchester decoder will lock onto the transmit data stream.

After data transmission is completed, the transmitter sends a start of idle (SOI) pulse to signal the end of a packet. During the idle period, Tx+ and Tx– are held low. Occasionally, link pulses are transmitted during the idle period.

The $\overline{XMT}$ pin is an output that indicates transmit activity. The pin consists of an open drain output with an internal pull-up resistor and can drive an LED from VCC or another digital input. In order to make an LED visible, $\overline{XMT}$ has an internal blinker circuit that generates a 100ms blink (50ms high, 50ms low) that is triggered when a trans-mission starts. At the completion of the 100ms blink period, if a transmission is in progress, another 100ms blink is generated.

RECEPTION

The twisted pair receive data is typically transformer coupled and terminated with an external resistor as shown in Figure 12.

The output of the transformer is then applied to the device input pins Rx+ and Rx–. The input is differential, and the common mode input voltage is biased to VCC/2 by two internal 10K bias resistors from Rx+, Rx– to VCC/2.

The Rx+ and Rx– inputs then go to the receive filter. The receive filter is a continuous 3rd order LPF and has the following characteristics:

1. 3 dB cut-off frequency	15 MHz
2. Insertion Loss (5–10 MHz)	- 1.0 dB
3. 30 MHz attenuation	17.5 dB min.

The output of the filter goes to the receive comparators. There are two receive comparators inside the chip, threshold and zero crossing. The threshold comparator determines if the receive data is valid by checking the input signal level against a predetermined positive and negative squelch level. Once the threshold comparator determines that valid data is being received, the zero crossing comparator senses zero crossings to determine data transitions. Both comparators are fast enough to respond to 12ns pulse widths with minimum squelch overdrive.

FUNCTIONAL DESCRIPTION (Continued)

The receive squelch circuit determines when data on incoming Rx+, Rx– is valid. The receive squelch is considered "on" when the data is deemed to be invalid, and the receive squelch is considered "off" when data is determined to be valid.

The input signal must meet the following criteria in order to turn receive squelch off and be recognized as valid data:

1. The input signal must exceed the receive squelch on level. When this occurs, a 400ns squelch interval timer is started.

2. During the 400ns squelch interval, the input signal must go from one squelch threshold to the opposite polarity squelch threshold in less than 127ns.

3. During the 400ns squelch interval, the input signal has to make less than 9 squelch threshold to opposite polarity squelch threshold crossings.

When the receive squelch is turned off, the receive squelch off level is reduced to 2/3 of receive squelch on level.

The receive squelch will be turned back on if either the incoming data peaks go below the receive squelch off level for 400ns or the start of idle (SOI) pulse is detected.

The receive squelch on level can be digitally programmed for one of two possible levels by using the RSL pin. When RSL = 1, the squelch on level complies with the IEEE 802.3i–1990 specification. When RSL = 0, the receive squelch on level is lowered in order to accommodate greater receive attenuation and consequently longer twisted pair cable lengths. The receive squelch on level can be programmed as follows:

RECEIVE SQUELCH ON LEVEL

RSL	Application	Min	Typ	Max
1	10BASE-T	300		585mV
0	Long Distance	200		390mV

The $\overline{RCV}$ pin is an output that indicates receive activity. The pin consists of an open drain output with an internal pull-up resistor and can drive an LED from VCC or another digital input. In order to make an LED visible, $\overline{RCV}$ has an internal blinker circuit that generates a 100ms blink (50ms high, 50ms low) that is triggered when reception starts. At the completion of the 100ms blink period, if reception is in progress, another 100ms blink is generated.

The manchester decoder receives data from either the twisted pair interface (as described above) or the AUI (described in AUI section).

The manchester decoder is responsible for recovering clock and data from the incoming receive bit stream.

Clock and data recovery is accomplished by a digital PLL which can lock on the incoming bit stream in less than 1.6µs.

The clock (RxC) and NRZ data (RxD) are then output to the external world via the controller interface.

SOI

A start of idle (SOI) pulse is sent at the end of transmission in order to signal to all receivers that transmission has ended and the idle period begins. Thus, the transmit section has an SOI generator and the receive section has an SOI detector.

The transmit SOI pulse generator inserts an SOI pulse at the end of each transmission. The SOI pulse is typically a 250ns positive pulse inserted after the last positive data transition. Depending on the data pattern, the positive data transition could occur either in the middle or at the end of the last bit cell. So the actual width of the transmitted SOI pulse can vary from 250–300ns, typically.

The receive SOI detector senses the SOI pulse using the zero crossing comparator. When the SOI pulse is detected, the receiver signals to the controller that receive data is no longer valid and turns the receive squelch on.

LINK PULSE

During the idle period, link pulses are sent by the transmitter and detected by the receiver so that the integrity of the twisted pair link can be continuously monitored. Thus, the transmit section has a link pulse generator, and the receiver has a link pulse detector.

The transmit link pulse generator transmits a 100ns wide positive pulse (Tx+ high, Tx– low) every 16 ±8ms.

IEEE 802.3i–1990 Section 14 requires the link pulse to be shaped to meet a template when passed or not passed through the twisted pair line model. The transmit waveform generator takes the link pulse and generates the waveform on TX± when passed or not passed through the twisted pair line model.

The receiver monitors the receive input to determine if the link pulses are present. When the device is in the link pulse pass state, normal packet transmission and reception can occur. All link pulses less than 2–7ms apart are ignored while in the link pass state. If no link pulses or receive packets are detected for a period of 50–150ms, the device goes into the link pulse fail state.

When the device is in the link pulse fail state, reception is inhibited and the transmitter is placed in the idle state (no data transmission but link pulses are still transmitted). In order for the device to exit the link pulse fail state, one complete packet or 4 consecutive link pulses must be detected, and transmit and receive must be idle. Consecutive link pulses are defined as pulses that occur within 25–150ms of each other. If the link pulses occur

FUNCTIONAL DESCRIPTION (Continued)

2–7ms apart in the link fail state, the device ignores the link pulses and resets the number of consecutive link pulses to zero. After the link pulse fail state is exited, transmission and reception can be resumed.

Link pulse status is indicated by the $\overline{LTP}$ pin. $\overline{LTP}$ is a dual function input/output pin that acts both as an active low link test pass output and a link test disable input. The pin consists of an open drain output with an internal pull-up resistor. If the pin is tied to GND, the pin acts as an input and the link test function is disabled. If the pin is not tied to GND, the pin acts as an active low link test pass output and can drive an LED from VCC or another digital output. Thus, the LED is lit when the link test is passing.

JABBER

The transmit section contains a jabber detect circuit. Jabber is a fault condition characterized by a babbling transmitter. The ML2652 and ML2653 detect jabber when a transmission packet exceeds 20–150ms in length. If jabber detect occurs, the transmit output is disabled, the collision signal COL is sent over the controller interface, and the $\overline{JAB}$ pin is pulled low. The device remains in the jabber detect state until there is at least 250–750ms of continuous non-transmission. Note that link pulses continue to be transmitted even when the device is in the jabber condition.

The jabber detection circuitry can be disabled (only on the ML2652) with the JABDIS pin for testing and diagnostic purposes. Disabling jabber means that a jabber condition is never recognized, even when it occurs. JABDIS is an active high jabber disable input and has an internal pull-down resistor to GND.

COLLISION

Collision occurs whenever the DTE card is transmitting and receiving data simultaneously. However, the collision circuit on the ML2652 operates differently depending on whether twisted pair interface or AUI is being used.

When the twisted pair interface is used, collision occurs whenever the device is transmitting and receiving data simultaneously, that is when both RxE and TxE are active. The collision state is indicated by COL and $\overline{CLS}$ pins. COL is used to signal collision to the controller. $\overline{CLS}$ is an active low open drain output. $\overline{CLS}$ is activated during Jabber, but not during SQE test while COL is activated during both.

When the AUI is used (ML2652 only), collision is no longer detected from simultaneous transmission and reception, but the collision state is determined when a collision signal is present on the AUI collision inputs, CI+ and CI–. A 10 MHz square wave has to be applied to this input in order for the device to signal the collision state on COL and $\overline{CLS}$.

The $\overline{CLS}$ pin is an output that indicates collision activity. The pin consists of an open drain output with an internal

pull-up resistor and can drive an LED from VCC or another digital input. In order to make an LED visible, $\overline{CLS}$ has an internal blinker circuit that generates a 100ms blink (50ms high, 50ms low) that is triggered when a collision starts. At the completion of the 100ms blink period, if collision is in progress, another 100ms blink is generated.

SQE TEST

When the twisted pair interface is used, the device tests the collision circuitry at the end of each transmission by sending a 1µs collision pulse over the COL pin. This is known as SQE (signal quality error) test and is shown in the transmit timing diagram in Figure 1. The SQE test is disabled if the device is in jabber detect state or link pulse fail condition.

When AUI is used (ML2652), the SQE test pulse is generated by an external MAU and the external MAU sends the SQE test pulse to the ML2652 via the collision inputs , CI+ and CI–. The ML2652 then relays the collision signal to the controller via the COL and $\overline{CLS}$ output pins.

RECEIVE POLARITY DETECT AND AUTO CORRECTION

The ML2652 and ML2653 contain an auto-polarity circuit that detects the polarity of the receive twisted pair leads, Rx+ and RX-and internally reverses the leads if their polarity is incorrect.

When the device is powered up, it is assumed that the polarity is correct and no polarity correction occurs. Then receive polarity is continuously monitored by checking the polarity of the SOI and link pulses since they are always positive pulses. If either 2 consecutive SOI or 4 consecutive link pulses have incorrect RX± polarity, then the auto-polarity circuit internally reverses the Rx+ and Rx– connections.

AUI (APPLIES ONLY TO ML2652)

The ML2652 can be used with an external MAU via the Attachment Unit Interface (AUI). When the AUI is used, the internal MAU functions and twisted pair interface are disabled, and the device only uses the manchester encoder and decoder functions, as shown in the block diagram. The AUI consists of three differential signal pairs: DI, DO, and CI. The function of each pair is described below.

The DO+ and DO– are differential outputs to the external MAU which contain the transmit data output from the Manchester encoder. The DO+ and DO– output drivers are capable of driving 50 meters of 78 ohm cable with less than 5ns rise and fall time and less than ±0.5ns of jitter. In addition, at the end of transmission, the AUI output driver inserts a 200ns minimum pulse and meets the turnoff and idle characteristics specified in IEEE 802.3–1988. An external 78 ohm resistor across DO+ and DO– is required as shown in Figure 12 to develop the proper output levels from the internal current sources. The DO+ and DO–

FUNCTIONAL DESCRIPTION (Continued)

outputs can be coupled to an external MAU with either capacitors or a transformer. The ML2652 meets all AUI transmitter specifications outlined in IEEE 802.3–1988 Section 7.

DI+ and DI– are inputs from the external MAU which contain the receive data that goes to the manchester decoder.

The DI+ and DI– inputs contain an AUI DI squelch circuit which determines when incoming data on DI+ and DI– is valid. The DI squelch is considered "on" when the data is deemed to be invalid, and the DI squelch is considered "off" when data is determined to be valid.

The input signal on DI+ and DI– must meet the following criteria in order to turn receive squelch off and be recognized as valid data:

   1. The input signal must exceed the negative AUI DI squelch on level.

   2. The input signal must exceed the negative AUI DI squelch on level for more than 20ns.

When the DI squelch is turned off, the DI squelch off level is reduced to 2/3 of the DI squelch on level.

The DI squelch circuit will be turned back on if the idle period is detected by no DI squelch level transitions for more than 180ns.

An external 78 ohm termination resistor is needed across DI+ and DI– as shown in Figure 12. The DI+ and DI– inputs can be coupled from an external MAU into the ML2652 with either capacitors or a transformer. The ML2652 meets all AUI receiver specifications outlined in IEEE 802.3–1988 Section 7.

CI+ and CI– are inputs from the external MAU which contain the 10 MHz ± 15% collision signal as defined in IEEE 802.3–1988 Section 7. The CI+ and CI– inputs contain the same squelch circuit used on the DI inputs described in previous paragraphs in this section.

An external 78 ohm termination resistor is needed across CI+ and CI– as shown in Figure 12. The CI+ and CI– inputs can be coupled from an external MAU into the ML2652 with either capacitors (shown in Figure 12) or a transformer. The ML2652 meets all AUI receiver specifications outlined in IEEE 802.3–1988 Section 7.

The ML2652 contains an AUI/$\overline{\text{TP}}$ select input pin which controls whether the AUI or twisted pair interface is to be used for data transmission and reception. When AUI/Twisted Pair Switching = High, the AUI is used for data transmission and reception. When AUI/Twisted Pair Switching = Low, the twisted pair interface is used for data transmission and reception.

The $\overline{\text{AUISEL}}$ pin is a digital status output that indicates which interface has been selected for data transfer, either twisted pair or AUI. The pin consists of an open drain output with an internal pull-up resistor and can drive an LED from VCC or another digital input. $\overline{\text{AUISEL}}$ = High indicates that the twisted pair interface has been selected. $\overline{\text{AUISEL}}$ = Low indicates that the AUI interface has been selected.

The ML2652 has the capability to automatically select between the twisted pair interface and AUI. This automatic interface selection is accomplished by tying the $\overline{\text{LTP}}$ output pin to the AUI/$\overline{\text{TP}}$ input pin. When these two pins are connected together, if valid link pulses are detected, it is assumed that the twisted pair interface is being used. This causes $\overline{\text{LTP}}$ output to go low, thus forcing AUI/$\overline{\text{TP}}$ low, and thus enabling the twisted pair interface. If no valid link pulses are detected, it is assumed that the twisted pair interface is not being used, thus causing $\overline{\text{LTP}}$ to go high, thus forcing AUI/$\overline{\text{TP}}$ high, thus enabling the AUI interface. If valid link pulses reappear, the device will automatically disable the AUI and enable the twisted pair interface. The algorithm for determining valid link pulses is described in the Link Pulse section.

LOOPBACK

LPBK provides a loopback through the manchester encoder/decoder, but not through the on-chip 10BASE-T MAU. No data will go out on either the AUI port or the twisted pair port in this mode. This same function is found on many discrete manchester encoder/decoders.

IEEE 802.3 MAUs normally loop the transmit data (DO+) when transmitting with no collisions. When using an external transceiver through the ML2652's AUI port, the controller can first check the local loopback by setting LPBK. If it passes this test it can then check the AUI cable and external MAU by doing the normal MAU loopback.

FULL DUPLEX OPERATION

The ML2652 and ML2653 are capable of operating in the full duplex mode which transmits and receives data simultaneously. In the full duplex mode the collision circuitry is disabled just as it is in the loopback mode. To achieve full duplex operation the full duplex pin FD is enabled and the loopback pin LPBK must be disabled. Both of these conditions must be present to operate in the full duplex mode.

CONTROLLER INTERFACE

The ML2652 and ML2653 has a flexible and programmable digital interface which enables it to directly interface to Ethernet controllers manufactured by Intel, AMD, National and Seeq.

FUNCTIONAL DESCRIPTION (Continued)

The controller interface consists of seven pins. TxC, TxD, and TxE are the transmit clock output, transmit data input, and transmit data enable input, respectively. RxC, RxD, and RxE are the receive clock output, receive data output, and receive data enable output, respectively. COL is the collision detect output.

All the standard Ethernet controllers use a similar controller interface but differ in the polarity of COL, LPBK, TxE and RxE, and in what edge of TxC and RxC that clocks in the data. They also differ on whether the RxC clock needs to be continuous or not during idle, and on the polarity of RxD during idle. In order to accommodate the different controller interface definitions, the controller select pins, CS2–0, modify these signals according to Table 1.

POWERDOWN

The device can be placed in the power down mode with the controller select pins CS2–0 as described in Table 1. When in powerdown mode, the current consumption is reduced to less than ZmA and all device functions are disabled.

CRYSTAL OSCILLATOR

The ML2652 requires an accurate 20 MHz reference for internal clock generation. This can be achieved by

connecting an external crystal or an external clock between the CLK and GND pins.

If an external clock is used, it must have a frequency of 20 MHz ±0.01% and have high and low levels of 3.5 and 1.5 volts.

If a crystal is used, the crystal should be placed physically as close as possible to the CLK and GND pins, especially CLK. No other external capacitors or components are required. The crystal should have the following characteristics:

1. Parallel resonant type

2. Frequency: 20 MHz

3. Tolerance: ±0.005% @ 25°C

4. Less than 0.005% frequency drift across temperature.

5. Maximum equiv. series resistance:
   15 ohms @ 1–200µW
   30 ohms @ 0.01–1µW

6. Typical load capacitance: 20pF

7. Maximum case capacitance: 5pF

Table 1. Controller Select Pin Definitions

CS2–0	TxC	TxE	RxC	RxE	COL	LPBK	Idl RxC	Idl RxD	Controller	
0 0 0	r	h	r	h	h	h	m	l	NSC	DP8390
0 0 1	f	l	f	l	l	l	n	hi	Intel	82586/96
0 1 0	r	h	r	h	h	h	n	hi	AMD Motorola*	AM7990
0 1 1	f	h	r	h	h	l	c	lo	Seeq	8003/5
1 0 0	—	—	—	—	—	—	—	—	—	
1 0 1	—	—	—	—	—	—	—	—	—	
1 1 0	—	—	—	—	—	—	—	—	—	
1 1 1	—	—	—	—	—	—	—	—	PDN mode	

r = rising edge clocks data   h = active high   c = RxC required continuously
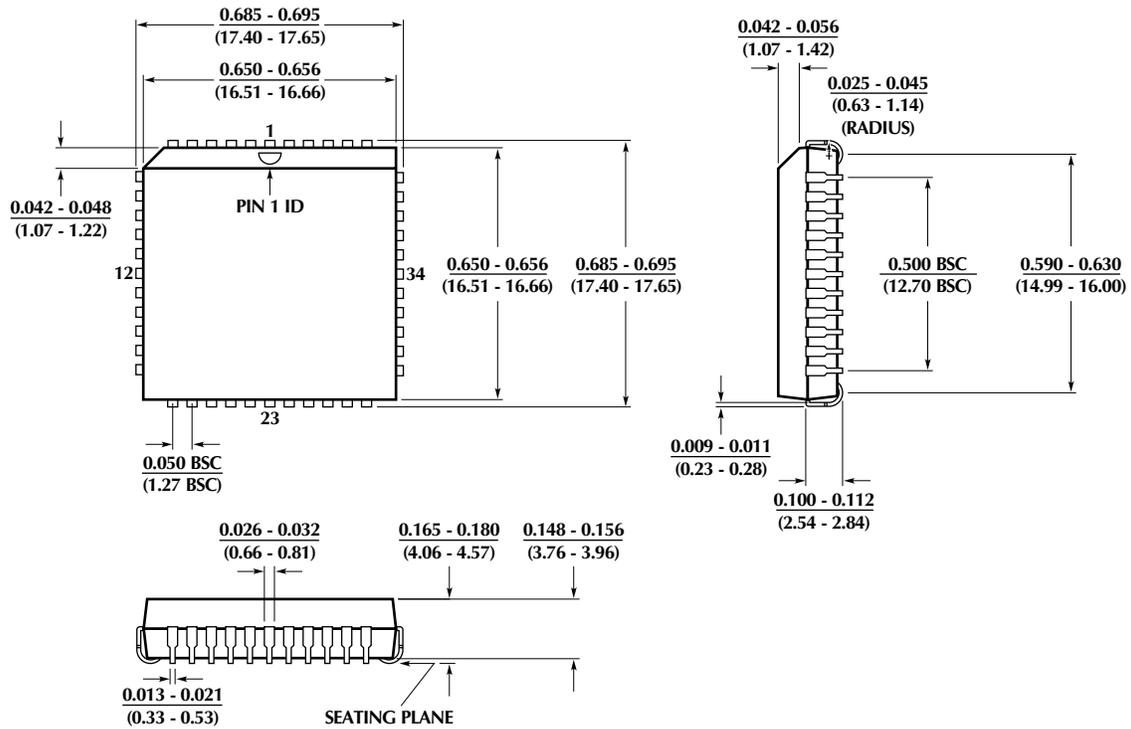f = falling edge clocks data   l = active low   n = RxC only during RxD transmission
　　　　　　　　　　　　　　　　　　　　m = RxC only during RxD transmission + 5 extra RxC cycles

* AMD mode is also recommended for all Motorola's QUICC, Power QUICC or simlar Communications Controllrs (MPC850, MPC860m ....). These controllers should be 5V or 3.3 V devices with 5V-friendly I/O pins
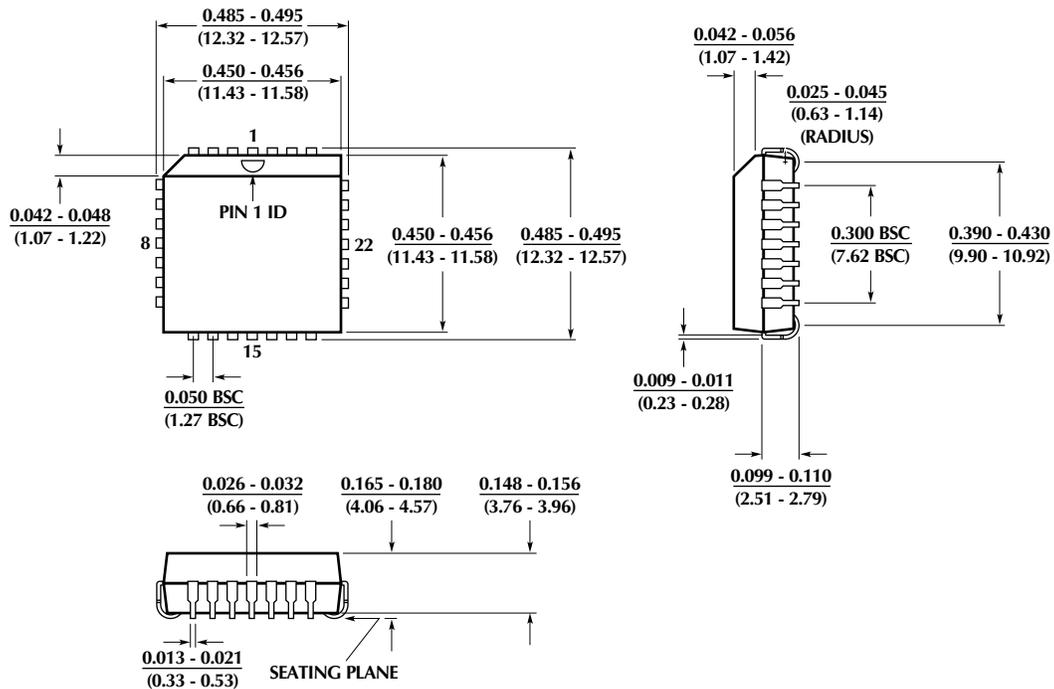
PHYSICAL DIMENSIONS inches (millimeters)

Package: Q44
44-Pin PLCC

0.685 - 0.695
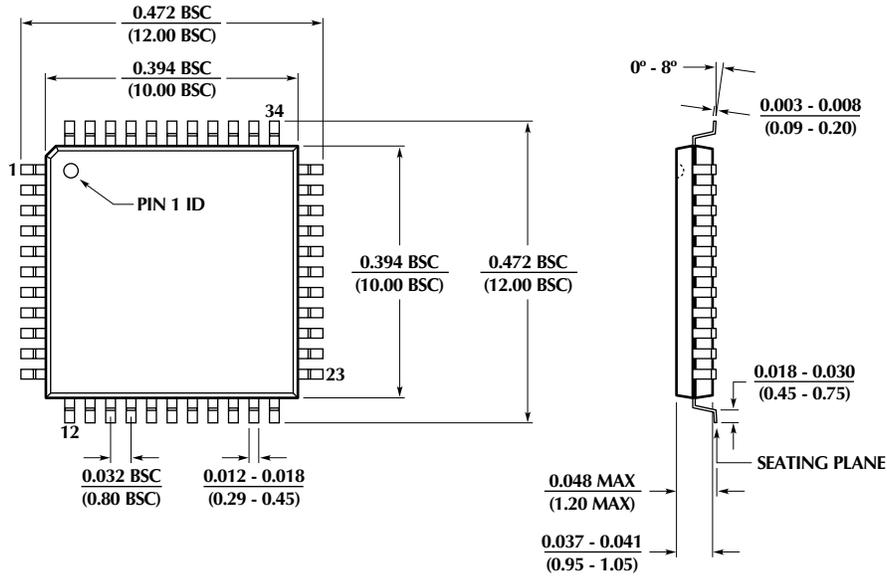(17.40 - 17.65)

0.650 - 0.656
(16.51 - 16.66)

1

PIN 1 ID

0.042 - 0.048
(1.07 - 1.22)

12

34

0.650 - 0.656
(16.51 - 16.66)

0.685 - 0.695
(17.40 - 17.65)

23

0.050 BSC
(1.27 BSC)

0.042 - 0.056
(1.07 - 1.42)

0.025 - 0.045
(0.63 - 1.14)
(RADIUS)

0.500 BSC
(12.70 BSC)

0.590 - 0.630
(14.99 - 16.00)

0.009 - 0.011
(0.23 - 0.28)

0.100 - 0.112
(2.54 - 2.84)

0.026 - 0.032
(0.66 - 0.81)

0.165 - 0.180
(4.06 - 4.57)

0.148 - 0.156
(3.76 - 3.96)

0.013 - 0.021
(0.33 - 0.53)

SEATING PLANE

Package: Q28
28-Pin PLCC

0.485 - 0.495
(12.32 - 12.57)

0.450 - 0.456
(11.43 - 11.58)

1

PIN 1 ID

0.042 - 0.048
(1.07 - 1.22)

8

22

0.450 - 0.456
(11.43 - 11.58)

0.485 - 0.495
(12.32 - 12.57)

15

0.050 BSC
(1.27 BSC)

0.042 - 0.056
(1.07 - 1.42)

0.025 - 0.045
(0.63 - 1.14)
(RADIUS)

0.300 BSC
(7.62 BSC)

0.390 - 0.430
(9.90 - 10.92)

0.009 - 0.011
(0.23 - 0.28)

0.099 - 0.110
(2.51 - 2.79)

0.026 - 0.032
(0.66 - 0.81)

0.165 - 0.180
(4.06 - 4.57)

0.148 - 0.156
(3.76 - 3.96)

0.013 - 0.021
(0.33 - 0.53)

SEATING PLANE

PHYSICAL DIMENSIONS inches (millimeters)

Package: H44-10
44-Pin (10 x 10 x 1mm) TQFP

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2652CQ	0°C to 70°C	44-Pin PLCC (Q44)
ML2653CQ	0°C to 70°C	28-Pin PLCC (Q28)
ML2653CH	0°C to 70°C	44-Pin TQFP (H44-10)

DS2652_53-01

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12/9/98 Printed in U.S.A.