查询MM1492供应商 捷多邦，专业PCB打样工厂，24小时加急出货

I²C BUS Controlled 5-Input 2-Output AV Switch
Monolithic IC MM1492AF

Outline

This IC is a 5-input 2-output AV switch controlled by the I²C BUS developed for use in television. Because there are 2 outputs, it supports 2 screens and P-IN-P, and also supports an external output (monitor) pin.

Features

(1) Serial control by I²C BUS
(2) 5 inputs, 2 outputs
(3) 1 Y/C (S pin) inputs, 2 outputs
(4) The video and audio switches can be controlled independently
(5) Built-in 6dB amp for video
(6) Built-in Y/C (S pin) mix circuit
(7) One of the two audio outputs has a built-in -6dB ON/OFF switch
(8) Slave address can be changed. 90H and 92H possible.
(9) Audio muting from external pin possible
(10) Maintains high impedance even when I²C BUS line (SDA, SCL) power supply is off.
(11) Built-in 3 value discrimination function built-in
(12) Built-in power ON reset function
(13) Supports 2 screens and P-IN-P. Also supports external output (monitor) pin.

Package

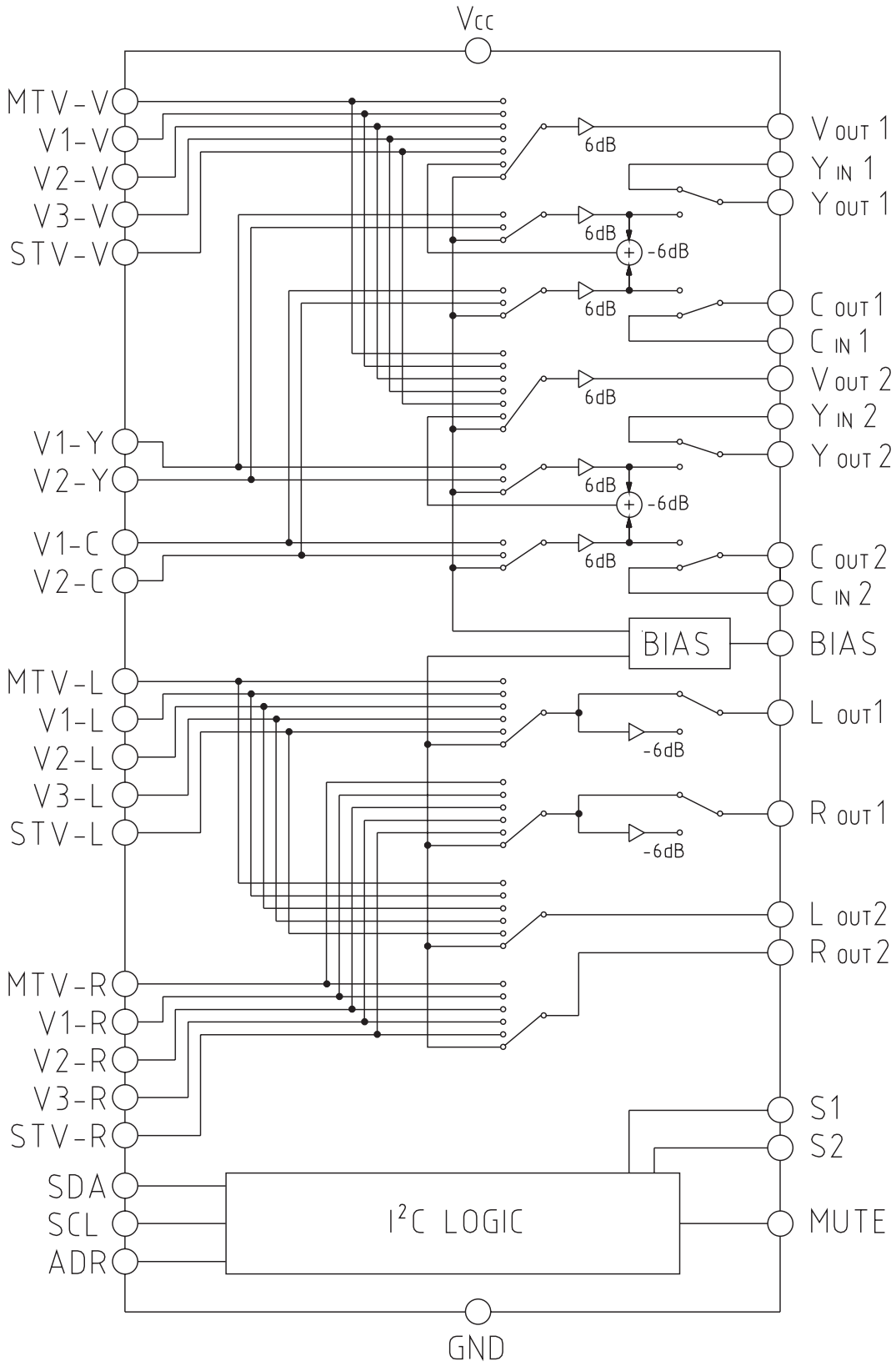
SOP-44B

Applications

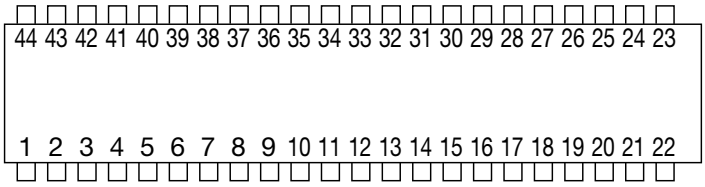
(1) TV
(2) Other video equipment

找PDF 维库一下 pdf.dzsc.com

Block Diagram



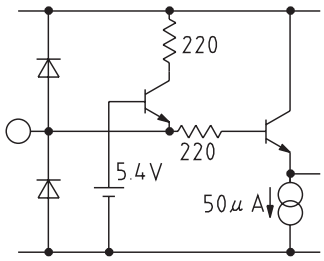
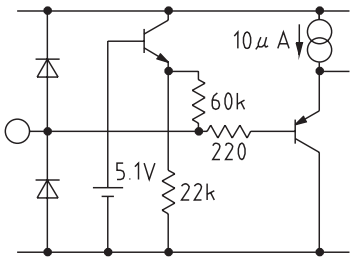
Pin Assignment

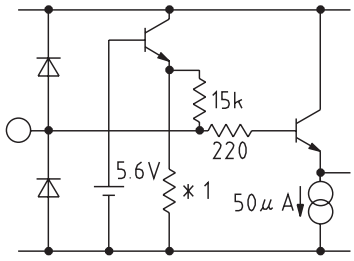
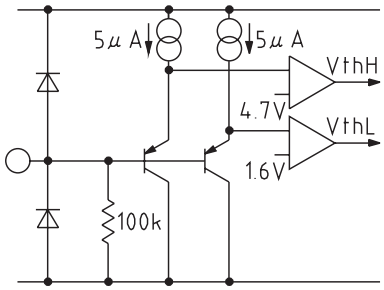
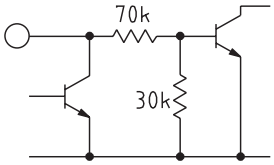
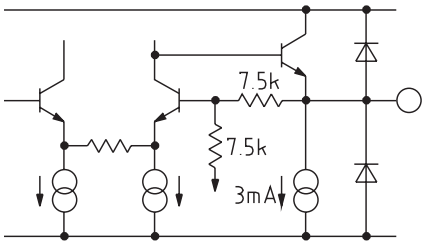
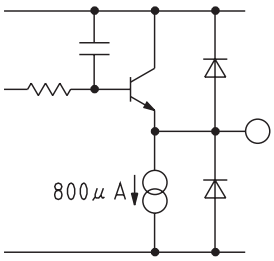
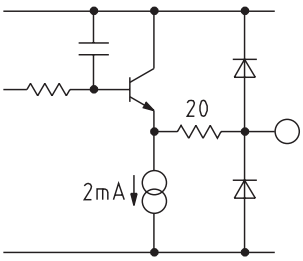


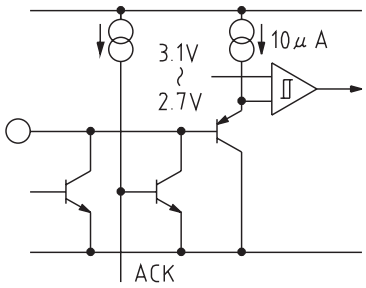
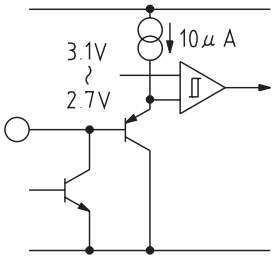
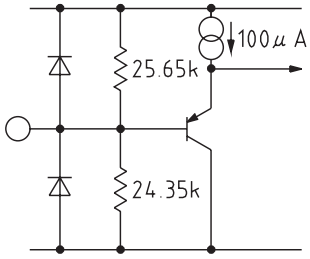
SOP-44B

1	V1–V	12	S2	23	VOUT2	34	YIN1
2	V1–L	13	V3–V	24	ROUT2	35	ROUT1
3	V1–Y	14	V3–L	25	COUT2	36	LOUT1
4	V1–R	15	V3–R	26	LOUT2	37	VOUT1
5	V1–C	16	STV–V	27	YOUT2	38	BIAS
6	S1	17	STV–L	28	GND	39	YOUT1
7	V2–V	18	STV–R	29	SDA	40	VCC
8	V2–L	19	YIN2	30	SCL	41	COUT1
9	V2–Y	20	ADR	31	MUTE	42	MTV–R
10	V2–R	21	CIN2	32	CIN1	43	MTV–V
11	V2–C	22	GND	33	GND	44	MTV–L

Pin Description

Pin No.	Pin name	Functions	Internal equivalet circuit diagram
1 3 7 9 13 16 19 34 43	V1–V V1–Y V2–V V2–Y V3–V STV–V YIN2 YIN1 MTV–V	Video input terminal (Composite or Y) *Sync chip clamp	
2 4 8 10 14 15 17 18 42 44	V1–L V1–R V2–L V2–R V3–L V3–R STV–L STV–R MTV–R MTV–L	Audio input terminal	

Pin No.	Pin name	Functions	Internal equivalet circuit diagram
5 11 21 32	V1–C V2–C CIN2 CIN1	Video input terminal (Croma)	 ＊1 5,11PIN=25kΩ、21,23PIN=12.5kΩ
6 12	S1 S2	Distinction 3-effects input terminal DC Detect	
20 31	ADR Mute	Sleve address select Audio Mute terminal	
22 28 33	GND	GND	
23 37	VOUT2 VOUT1	Composite video out	
24 26 35 36	ROUT2 LOUT2 ROUT1 LOUT1	Audio out terminal	
25 27 39 41	COUT2 YOUT2 YOUT1 COUT1	S–Video out terminal	

Pin No.	Pin name	Functions	Internal equivalet circuit diagram
29	SDA	Data input from I²C	
30	SCL	CLK input from I²C	
38	BIAS	Internal bias terminal	
40	Vcc	Vcc	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	Tstg	–40~+125	°C
Operating temperature	Topr	–20~+75	°C
Power supply voltage	Vccmax.	12	V
Allowable loss	Pd	1100	mW

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	Topr	–20~+75	°C
Operating voltage	Vop	+8~+10	V

Electrical Characteristics (Except where noted otherwise, V_{CC}=9V, Ta=25°C)

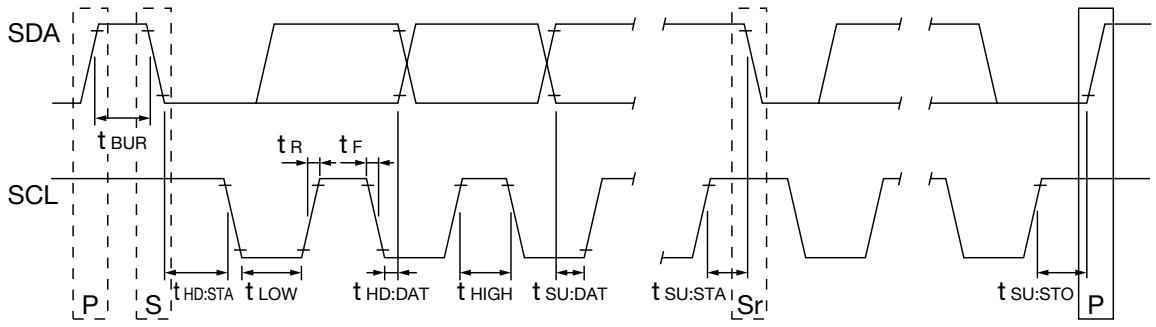
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption	I_{CC}	No signal	39	55	71	mA
V_{OUT}1						
Voltage gain	G_{V1}	SIN wave : 1V_{P-P} 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	f_{V1}	SIN wave : 1V_{P-P} 10MHz/100kHz	–1.0	0.0	1.0	dB
Differential gain	DG_{V1}	Staircase signal 1V_{P-P}	–3	0	3	%
Differential phase	DP_{V1}	Staircase signal 1V_{P-P}	–3	0	3	deg
Input dynamic ranges	D_{V1}	SIN wave : 100kHz THD=1.0%	1.4	1.5		V_{P-P}
V_{OUT}2						
Voltage gain	G_{V2}	SIN wave : 1V_{P-P} 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	f_{V2}	SIN wave : 1V_{P-P} 10MHz/100kHz	–1.0	0.0	1.0	dB
Differential gain	DG_{V2}	Staircase signal 1V_{P-P}	–3	0	3	%
Differential phase	DP_{V2}	Staircase signal 1V_{P-P}	–3	0	3	deg
Input dynamic range	D_{V2}	SIN wave : 100kHz THD=1.0%	1.4	1.5		V_{P-P}
Y_{OUT}1						
Voltage gain	G_{Y1}	Vn–Y : SIN wave 1V_{P-P} 100kHz	5.5	6.0	6.5	dB
	G_{Y2}	Y_{IN}1 : SIN wave 2V_{P-P} 100kHz	–0.5	0.0	0.5	dB
Frequency characteristics	f_{Y1}	Vn–Y : SIN wave 1V_{P-P}	–1.0	0.0	1.0	dB
	f_{Y2}	Y_{IN}1 : SIN wave 2V_{P-P}	–1.0	0.0	1.0	dB
Differential gain	DG_{Y1}	Vn–Y : Staircase signal 1V_{P-P}	–3	0	3	%
		Y_{IN}1 : Staircase signal 2V_{P-P}	–3	0	3	%
Differential phase	DP_{Y1}	Vn–Y : Staircase signal 1V_{P-P}	–3	0	3	deg
		Y_{IN}1 : Staircase signal 2V_{P-P}	–3	0	3	deg
Input dynamic range	D_{Y1}	Vn–Y : SIN wave 100kHz THD=1.0%	1.4	1.5		V_{P-P}
	D_{Y2}	Y_{IN}1 : SIN wave 100kHz THD=1.0%	3.2	3.8		V_{P-P}
Output impedance	Z_{OY1}			(50)		Ω
Y_{OUT}2						
Voltage gain	G_{Y3}	Vn–Y : SIN wave 1V_{P-P} 100kHz	5.5	6.0	6.5	dB
	G_{Y4}	Y_{IN}2 : SIN wave 2V_{P-P} 100kHz	–0.5	0.0	0.5	dB
Frequency characteristics	f_{Y3}	Vn–Y : SIN wave 1V_{P-P}	–1.0	0.0	1.0	dB
	f_{Y4}	Y_{IN}2 : SIN wave 2V_{P-P}	–1.0	0.0	1.0	dB
Differential gain	DG_{Y2}	Vn–Y : Staircase signal 1V_{P-P}	–3	0	3	%
		Y_{IN}2 : Staircase signal 2V_{P-P}	–3	0	3	%
Differential phase	DP_{Y2}	Vn–Y : Staircase signal 1V_{P-P}	–3	0	3	deg
		Y_{IN}2 : Staircase signal 2V_{P-P}	–3	0	3	deg
Input dynamic range	D_{Y3}	Vn–Y : SIN wave 100kHz THD=1.0%	1.4	1.5		V_{P-P}
	D_{Y4}	Y_{IN}2 : SIN wave 100kHz THD=1.0%	3.2	3.8		V_{P-P}
Output impedance	Z_{OY2}			(50)		Ω
C_{OUT}1						
Voltage gain	G_{C1}	Vn–C : SIN wave 1V_{P-P} 100kHz	5.5	6.0	6.5	dB
	G_{C2}	C_{IN}1 : SIN wave 2V_{P-P} 100kHz	–0.5	0.0	0.5	dB
Frequency characteristics	f_{C1}	Vn–C : SIN wave 1V_{P-P}	–1.0	0.0	1.0	dB
	f_{C2}	C_{IN}1 : SIN wave 2V_{P-P}	–1.0	0.0	1.0	dB
Differential gain	DG_{C1}	C_{IN}1 : Staircase signal 2V_{P-P}	–3	0	3	%
Differential phase	DP_{C1}	C_{IN}1 : Staircase signal 2V_{P-P}	–3	0	3	deg
Input dynamic range	D_{C1}	Vn–Y : SIN wave 100kHz THD=1.0%	2.75	3.25		V_{P-P}
	D_{C2}	Y_{IN}1 : SIN wave 100kHz THD=1.0%	5.5	6.5		V_{P-P}
Input impedance	Z_{IC1}	Vn–C and C_{IN}1	10	15	20	kΩ
Output impedance	Z_{OC1}			(50)		Ω

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
$C_{OUT}2$						
Voltage gain	G_{C3}	Vn–C : SIN wave 1V_{P-P} 100kHz	5.5	6.0	6.5	dB
	G_{C4}	$C_{IN}2$: SIN wave 2V_{P-P} 100kHz	–0.5	0.0	0.5	dB
Frequency characteristics	f_{C3}	Vn–C : SIN wave 1V_{P-P}	–1.0	0.0	1.0	dB
	f_{C4}	$C_{IN}2$: SIN wave 2V_{P-P}	–1.0	0.0	1.0	dB
Differential gain	DG_{C2}	$C_{IN}1$: Staircase signal 2V_{P-P}	–3	0	3	%
Differential phase	DP_{C2}	$C_{IN}2$: Staircase signal 2V_{P-P}	–3	0	3	deg
Input dynamic range	D_{C3}	Vn–Y : SIN wave 100kHz THD=1.0%	2.75	3.25		V_{P-P}
	D_{C4}	$Y_{IN}2$: SIN wave 100kHz THD=1.0%	5.5	6.5		V_{P-P}
Input impedance	Z_{IC2}	$C_{IN}2$	10	15	20	kΩ
Output impedance	Z_{OC2}			(50)		Ω
$L_{OUT}1$						
Voltage gain	G_{L1}	SIN wave 2.5V_{P-P} 1kHz –6dB Select	–6.5	–6.0	–5.5	dB
	G_{L2}	SIN wave 2.5V_{P-P} 1kHz 0dB Select	–0.5	0.0	0.5	dB
Frequency characteristics	f_{L1}	SIN wave 2.5V_{P-P} 1MHz/1kHz	–3.0	0.0	1.0	dB
Total harmonic distortion	THD_{L1}	SIN wave 2.5V_{P-P} 1kHz		0.03	0.1	%
Input dynamic range	D_{L1}	SIN wave 1kHz THD<0.5%	2.6	2.8		Vrms
Output offset voltage	V_{OFFL1}	DC offset at the switching time		0	±15	mV
Input impedance	Z_{IL1}		42	60	78	kΩ
Output impedance	Z_{OL1}			(120)		Ω
$L_{OUT}2$						
Voltage gain	G_{L3}	SIN wave 2.5V_{P-P} 1kHz –6dB Select	–6.5	–6.0	–5.5	dB
	G_{L4}	SIN wave 2.5V_{P-P} 1kHz 0dB Select	–0.5	0.0	0.5	dB
Frequency characteristics	f_{L2}	SIN wave 2.5V_{P-P} 1MHz/1kHz	–3.0	0.0	1.0	dB
Total harmonic distortion	THD_{L2}	SIN wave 2.5V_{P-P} 1kHz		0.03	0.1	%
Input dynamic range	D_{L2}	SIN wave 1kHz THD<0.5%	2.6	2.8		Vrms
Output offset voltage	$VOFF_{L2}$	DC offset at the switching time		0	±15	mV
Output impedance	Z_{OL2}			(120)		Ω
$R_{OUT}1$						
Voltage gain	G_{R1}	SIN wave 2.5V_{P-P} 1kHz –6dB Select	–6.5	–6.0	–5.5	dB
	G_{R2}	SIN wave 2.5V_{P-P} 1kHz 0dB Select	–0.5	0.0	0.5	dB
Frequency characteristic	f_{R1}	SIN wave 2.5V_{P-P} 1MHz/1kHz	–3.0	0.0	1.0	dB
Total harmonic distortion	THD_{R1}	SIN wave 2.5V_{P-P} 1kHz		0.03	0.1	%
Input dynamic range	D_{R1}	SIN wave 1kHz THD<0.5%	2.6	2.8		Vrms
Output offset voltage	V_{OFFR1}	DC offset at the switching time		0	±15	mV
Input impedance	Z_{IR1}		42	60	78	kΩ
Output impedance	Z_{OR1}			(120)		Ω
$R_{OUT}2$						
Voltage gain	G_{R3}	SIN wave 2.5V_{P-P} 1kHz –6dB Select	–6.5	–6.0	–5.5	dB
	G_{R4}	SIN wave 2.5V_{P-P} 1kHz 0dB Select	–0.5	0.0	0.5	dB
Frequency characteristics	f_{R2}	SIN wave 2.5V_{P-P} 1MHz/1kHz	–3.0	0.0	1.0	dB
Total harmonic distortion	THD_{R2}	SIN wave 2.5V_{P-P} 1kHz		0.03	0.1	%
Input dynamic range	D_{R2}	SIN wave 1kHz THD<0.5%	2.6	2.8		Vrms
Output offset voltage	V_{OFFR2}	DC offset at the switching time		0	±15	mV
Output impedance	Z_{OR2}			(120)		Ω

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Crosstalk (*1)						
$V_{OUT}1$	CT_{V1}	SG1 : 4.43MHz $1V_{P-P}$ (At mix, SG2/3 input)		–60	–53	dB
$V_{OUT}2$	CT_{V2}	SG1 : 4.43MHz $1V_{P-P}$(At mix, SG2/3 input)		–60	–53	dB
$Y_{OUT}1$	CT_{Y1}	SG2 : 4.43MHz $1V_{P-P}$		–60	–53	dB
$Y_{OUT}2$	CT_{Y2}	SG2 : 4.43MHz $1V_{P-P}$		–60	–53	dB
$C_{OUT}1$	CT_{C1}	SG3 : 4.43MHz $1V_{P-P}$		–60	–53	dB
$C_{OUT}2$	CT_{C2}	SG3 : 4.43MHz $1V_{P-P}$		–60	–53	dB
$L_{OUT}1$	CT_{L1}	1kHz $2.5V_{P-P}$		–90	–80	dB
$L_{OUT}2$	CT_{L2}	1kHz $2.5V_{P-P}$		–90	–80	dB
$R_{OUT}1$	CT_{R1}	1kHz $2.5V_{P-P}$		–90	–80	dB
$R_{OUT}2$	CT_{R2}	1kHz $2.5V_{P-P}$		–90	–80	dB
Terminal voltage						
Video input terminal	V_{VIP}	No signal, No load	4.6	4.9	5.2	V
$V_{OUT}1/2$ terminal	V_{VOP}	No signal, No load	3.9	4.2	4.5	V
$Y_{OUT}1/2$ terminal	V_{YOP}	No signal, No load	3.2	3.5	3.8	V
$C_{OUT}1/2$ terminal	V_{COP}	No signal, No load	3.2	3.5	3.8	V
Audio input terminal	V_{AIP}	No signal, No load	4.0	4.3	4.6	V
Audio output terminal	V_{AOP}	No signal, No load	3.9	4.2	4.5	V
I²C condition (Refer to figure below)						
Input voltage L	V_{IL}		0.0		1.5	V
Input voltage H	V_{IH}		3.0		5.0	V
Low level output voltage	V_{OL}	SDA sink 3mA	0.0		0.4	V
High level input current	I_{IH}	SDA, SCL=4.5V	–10		10	V
Low level input current	I_{IL}	SDA, SCL=0.4V	–10		10	V
Clock frequency	f_{SCL}				100	kHz
Data transfer wait time	t_{BUF}		4.7			µS
SCL start hold time	$t_{HD:STA}$		4.0			µS
SCL low level hold time	t_{LOW}		4.7			µS
SCL high level hold time	t_{HIGH}		4.0			µS
SCL start setup time	$t_{SU:STA}$		4.7			µS
SDA data hold time	$t_{HD:DAT}$		200			nS
SDA data setup time	$t_{SU:DAT}$		250			nS
SCL rise–time	t_R				1000	nS
SCL fall–time	t_F				300	nS
SCL stop setup time	$t_{SU:STO}$		4.0			µS

(The inside of parentheses is design guarantee value.)

I²C condition



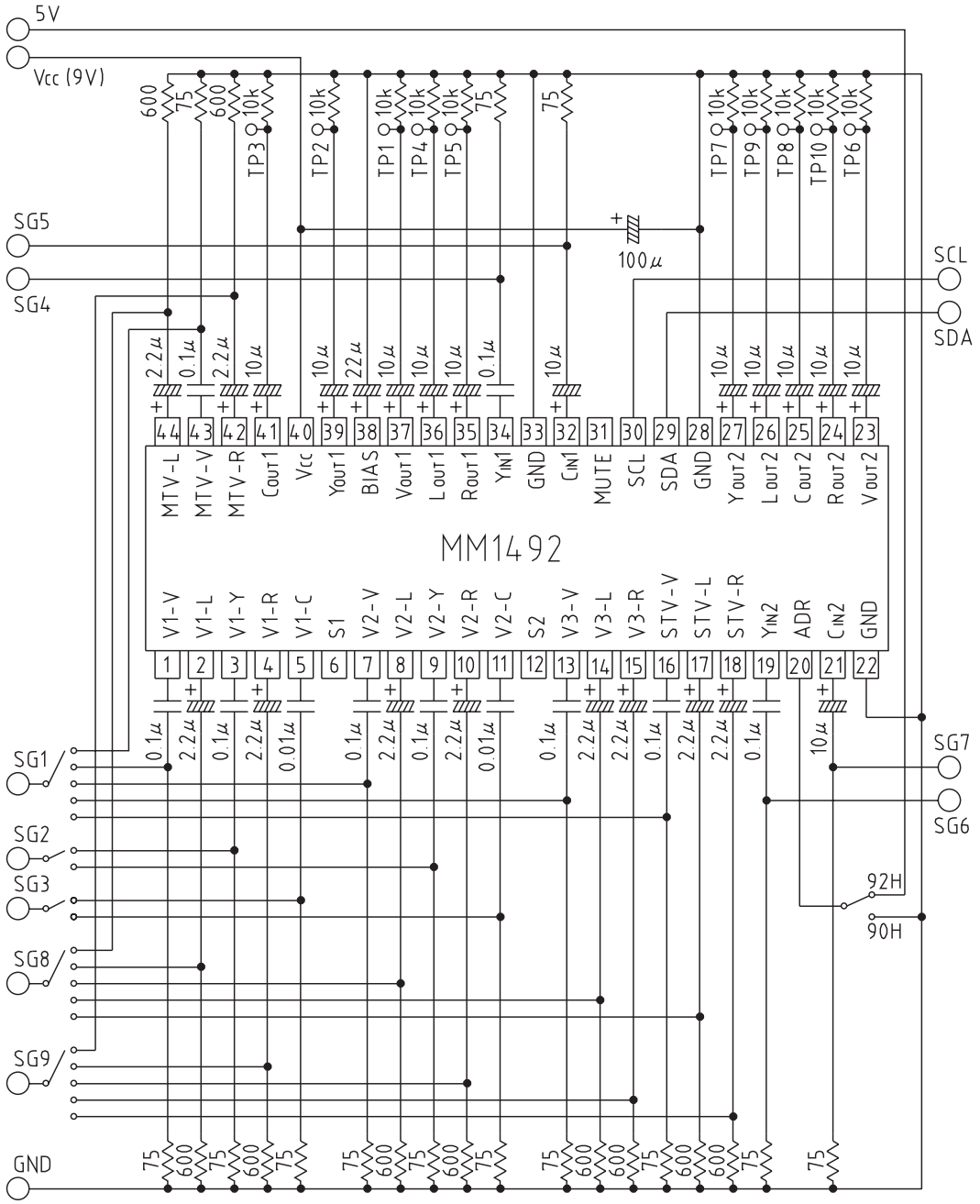
(Note.1) : Input signal symbol
Vn−V=MTV−V, V1−V, V2−V,V3−V, STV−V
Vn−Y=V1−Y, V2−Y
Vn−C=V1−C, V2−C

(Note.2) :*1 Test Circuit of Crosstalk
See Test Circuit 2

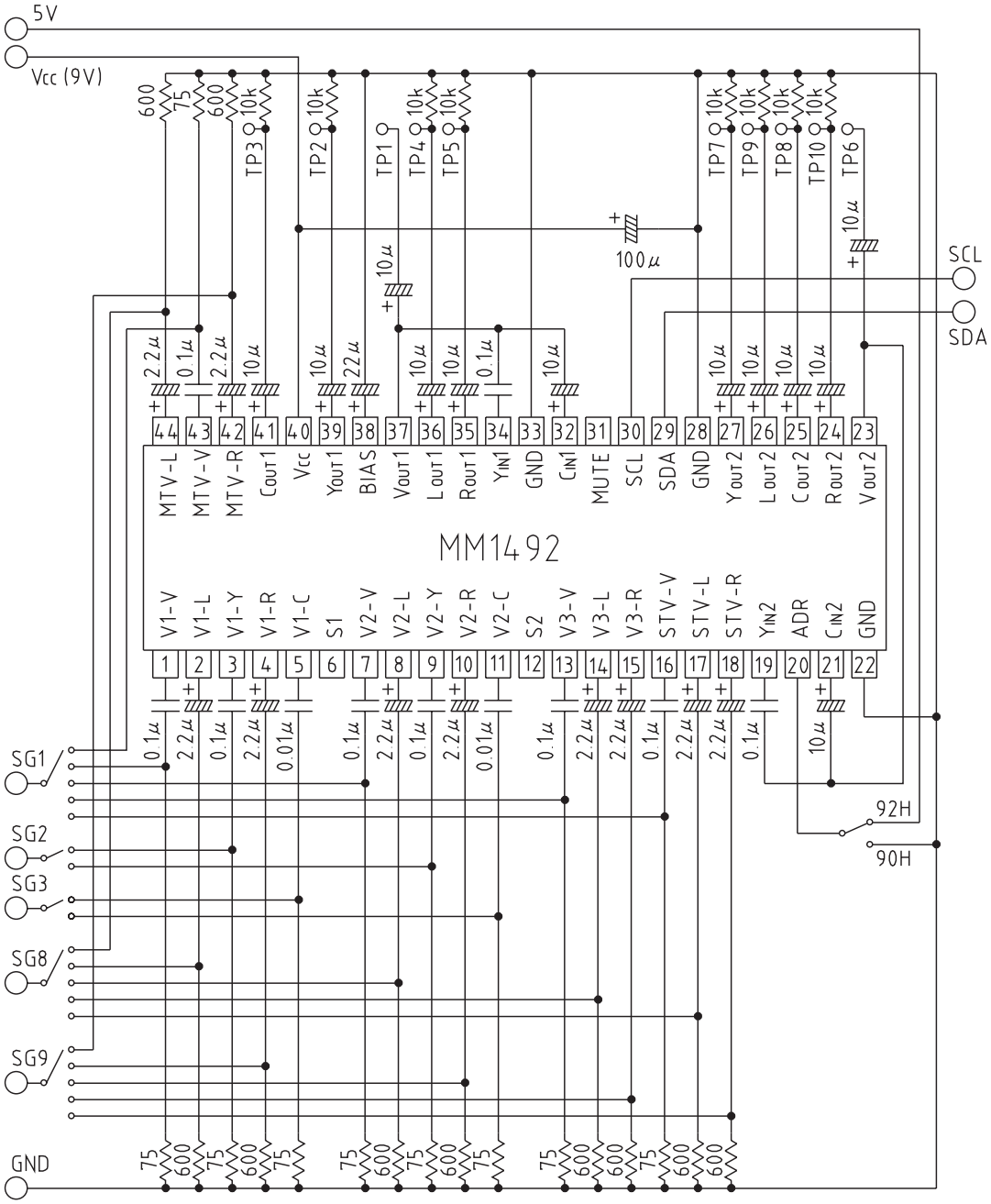
(Note.3) : Video inputs
Vn-V, Vn-Y, and YINn inputs are sync chip clamped, while Vn-C and CINn inputs are non-clamped.

Measuring Circuit

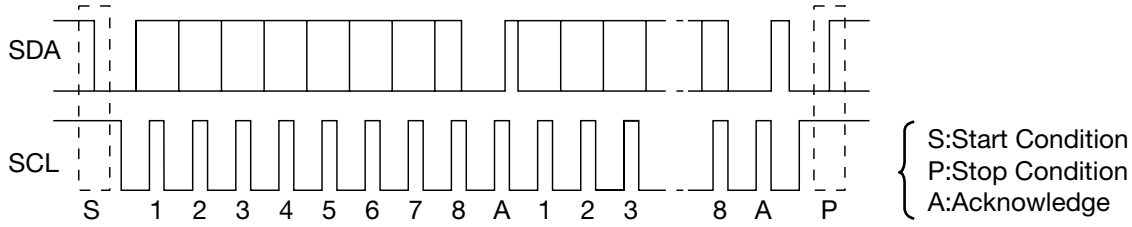
Measuring Circuit 1



Measuring Circuit 2 (Crosstalk measurement)



I²C BUS



I²C BUS is inter bus system controled by 2 lines (SDA, SCL).
Data are transmitted and received in the units of byte and Acknowledge.
It is transmitted by MSB first from the Start conditions.

[Control registers]

Control registers are data sent from the master for determining the switch conditions.
The data format is set as shown in the following figure.

S	Slave address							R/W	A	Control register 1								A	Control register 2								A	P
	1	0	0	1	0	0	0/1	0		b7	b6	b5	b4	b3	b2	b1	b0		b7	b6	b5	b4	b3	b2	b1	b0		
	Address byte																		Control data									

Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.
Set the R/W bit to 0 when data are used control registers.
As MM1492 slave address, either 90H or 92H can be selected according to the ADR terminal conditions.
When ADR terminal is L, 90H is selected.
The following figure indicates the control contents of control registers and switches.
Each bit of control registers is reset to 0, when power−on.

Register	b7	b6	b5	b4	b3	b2	b1	b0
1	Audio Gain 1	S/Comp select 1	Video out1 select			Audio out1 select		
2	Audio Gain 2	S/Comp select 2	Video out2 select			Audio out2 select		

MM1492 consists of one address byte and two control data bytes (3bytes in total).
All data over the limited length (4th and subsequent bytes) are fully neglected.
For details of the control contents of switches, refer to the separate table.

[Status registers]

Status registers are data to inform the device status.
The data format is set as shown in the following figure.

S	Slave address							R/W	A	Status register								NA	P
	1	0	0	1	0	0	0/1	1		b7	b6	b5	b4	b3	b2	b1	b0		
	Address byte									device status									

Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.
Set the R/W bit to 1 when data are used status registers.
As MM1492 slave address, either 91H or 93H can be selected according to the ADR terminal conditions.
When ADR terminal is L, 91H is selected.
Set the confirmation acknowledgement after the end of status register to non−acknowledgement.
The following figure shows the correspondence of the output data of status registers.

b7	b6	b5	b4	b3	b2	b1	b0
P-ON RESET	×	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL	×	×

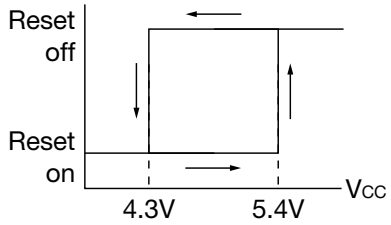
P-on RESET : 1 returns when the power on reset is done, 0 returns after reading data once.

S1/S2 OPEN : S1/S2 OPEN and SEL are identified by 3 values, and output according to the
S1/S2 SEL combinations in the following table.

DC voltage of S1/S2	S1/S2 OPEN	S1/S2 SEL
0.8V≦DC	0	1
1.3V≦DC≦3.5V	0	0
DC≦4.5V	1	0

[about power on reset]

MM1492 is provided with a power on reset function to reset each control register to 0 when power supply is turned on.
The power on reset threshold has the hysteresis as shown in following figure.



Switch Control Table

(1) Video output 1

b6	b5	b4	b3	VOUT1	YOUT1	COUT1
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV–V	YIN1	CIN1
0	0	1	0	V1–V	YIN1	CIN1
0	0	1	1	V2–V	YIN1	CIN1
0	1	0	0	V3–V	YIN1	CIN1
0	1	0	1	STV–V	YIN1	CIN1
0	1	1	0	Mute	Mute	Mute
0	1	1	1			
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV–V	YIN1	CIN1
1	0	1	0	V1–(Y+C)	V1–Y	V1–C
1	0	1	1	V2–(Y+C)	V2–Y	V2–C
1	1	0	0	V3–V	YIN1	CIN1
1	1	0	1	STV–V	YIN1	CIN1
1	1	1	0	Mute	Mute	Mute
1	1	1	1			

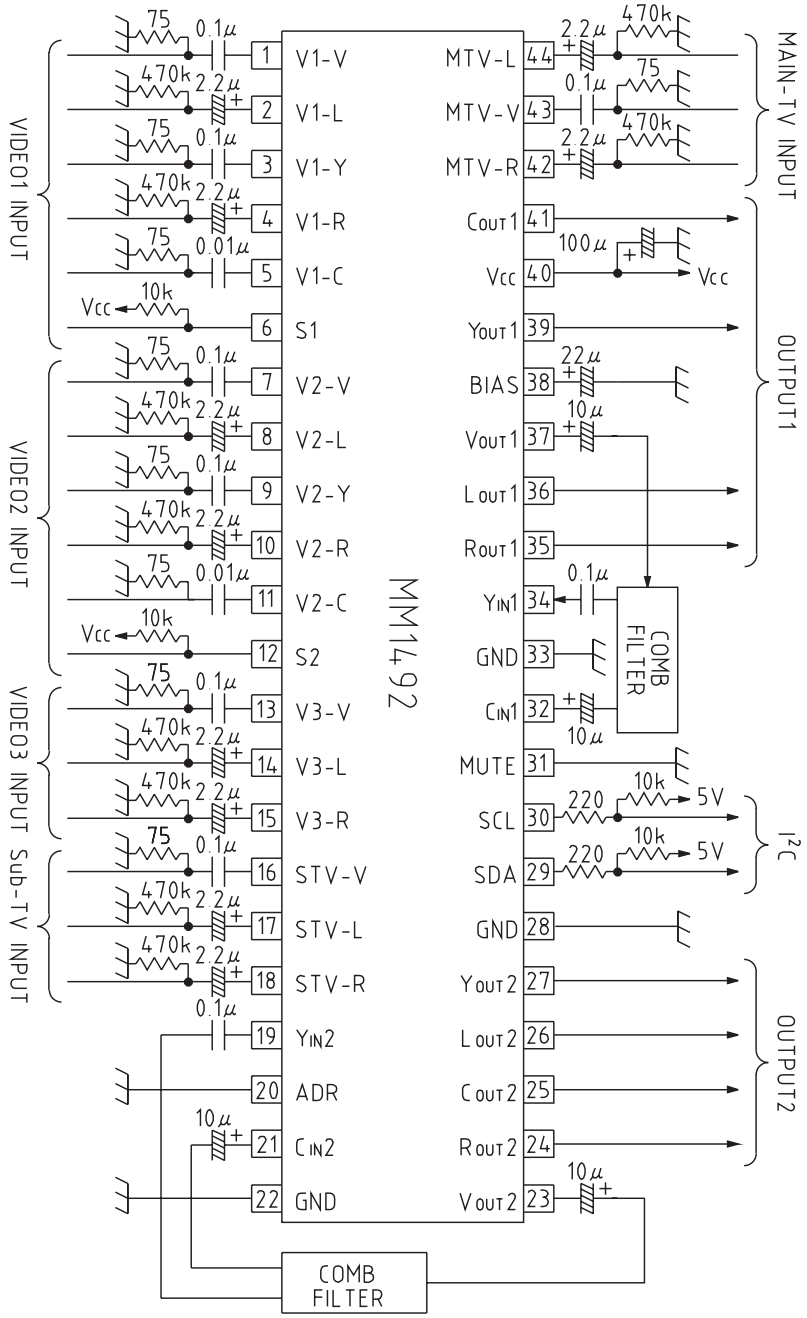
(2) Audio output 1

Mute terminal	b2	b1	b0	LOUT1	ROUT1
≦1.5V (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV–L	MTV–R
	0	1	0	V1–L	V1–R
	0	1	1	V2–L	V2–R
	1	0	0	V3–L	V3–R
	1	0	1	STV–L	STV–R
	1	1	0	Mute	Mute
	1	1	1		
≧3.0V				Mute	Mute

(3) Audio gain

b7	LOUT1	ROUT1
0	–6dB	–6dB
1	0dB	0dB

Application Circuit



Note.

(1) V_{OUT} is set to 4.2V, While C_{IN} is set to 4.9V.
Be careful since the capacity polarity may differ according to the comb filter bias.

(2) Each audio output can be set to myte by setting pin 31 to high. The mute is turned off in when pin 19 is open or low.