N *National Semiconductor*

MM58242 High Voltage Display Driver

General Description

The MM58242 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58242 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
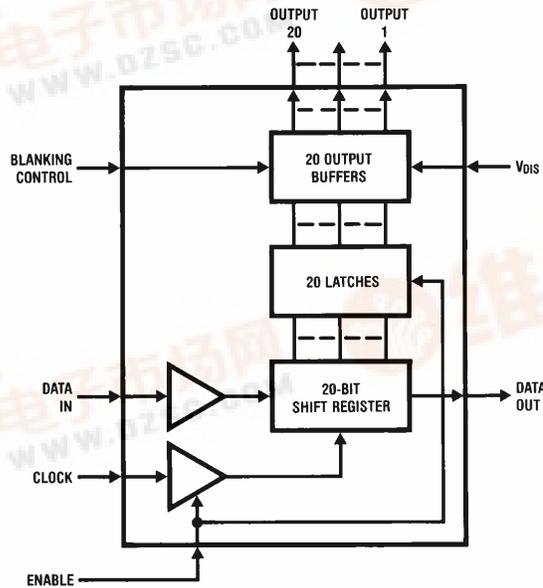- Simple to cascade

Block Diagram

FIGURE 1

TL/F/7924–1

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD} - 62.5V$
$V_{DD} + |V_{DIS}|$	62.5V
Storage Temperature	$-65°C$ to $+150°C$
Power Dissipation at $+25°C$	
Molded DIP Package, Board Mount	2.03W*
Molded DIP Package, Socket Mount	1.83W**
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

*Molded DIP Package, Board Mount, $\theta_{JA} = 52°C/W$, Derate 19.2 mW/°C above $+25°C$.

**Molded DIP Package, Socket Mount, $\theta_{JA} = 58°C/W$, Derate 17.2 mW/°C above $+25°C$.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD})			
$V_{SS} = 0V$	4.5	5.5	V
Display Voltage (V_{DIS})	-55	-25	V
Temperature Range	-40	$+85$	°C

DC Electrical Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD} I_{DIS}	Power Supply Currents	$V_{IN} = V_{SS}$ or V_{DD}, $V_{SS} = 0V$, V_{DIS} Disconnected $V_{DD} = 5.5V$, $V_{SS} = 0V$, $V_{DIS} = 55V$ All Outputs Low			150 10	μA mA
V_{IL} V_{IH}	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK Logic '0' Logic '1'	(Note 1)	2.4		0.8	V V
V_{OL} V_{OH} V_{OH}	Data Output Logic Levels Logic '0' Logic '1' Logic '1'	$I_{OUT} = 400\ \mu A$ $I_{OUT} = -10\ \mu A$ $I_{OUT} = -500\ \mu A$	$V_{DD} - 0.5$ 2.8		0.4	V V V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN} = 0V$ or V_{DD}	-10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
R_{OFF} R_{ON}	Display Output Impedances Output Off (Figure 3a) Output On (Figure 3b)	$V_{DD} = 5.5V$, $V_{SS} = 0V$ $V_{DIS} = -25V$ $V_{DIS} = -40V$ $V_{DIS} = -55V$ $V_{DIS} = -25V$ $V_{DIS} = 40V$ $V_{DIS} = -55V$	60 70 80 	 3.0 2.6 2.3	400 550 650 4.0 3.7 3.4	$k\Omega$ $k\Omega$ $k\Omega$ $k\Omega$ $k\Omega$ $k\Omega$
V_{DOL}	Display Output Low Voltage	$V_{DD} = 5.5V$, $I_{OUT} = $ Open Circuit, $-55V \leq V_{DIS} \leq -25V$	V_{DIS}		$V_{DIS} + 4$	V

Note 1: 74LSTTL $V_{OH} = 2.7V$ @ $I_{OUT} = -400\ \mu A$, TTL $V_{OH} = 2.4V$ @ $I_{OUT} = -400\ \mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

| Parameter	Conditions	Min	Typ	Max	Units

Clock Input
    Frequency, f_C
    High Time, t_H
    Low Time, t_L
	(Notes 3 and 4)	
		
		300
		300
				
				800
					
					kHz
					ns
					ns

Data Input
    Set-Up Time, t_{DS}
    Hold Time, t_{DH}
		100
		100
					ns
					ns

Enable Input
    Set-Up Time, t_{ES}
    Hold Time, t_{EH}
	(Note 2)	100
		100
					ns
					ns

Data Output
    CLOCK Low to Data Out
    Time, t_{CDO}
	$C_L = 50$ pF			500	ns

Note 2: For timimg purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 800 kHz, 50% $\pm 10\%$ duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package
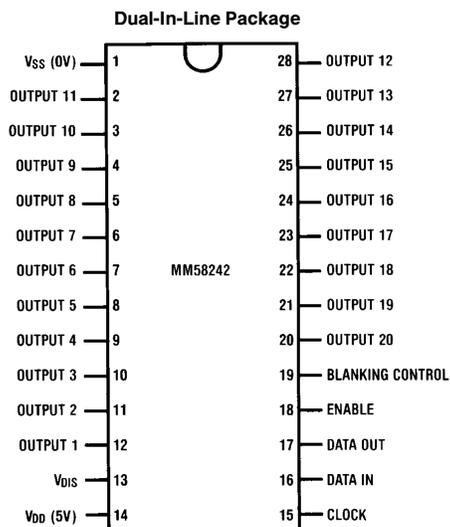
TL/F/7924–2

Top View
FIGURE 2

Order Number MM58242N
See NS Package Number N28B

Plastic Chip Carrier
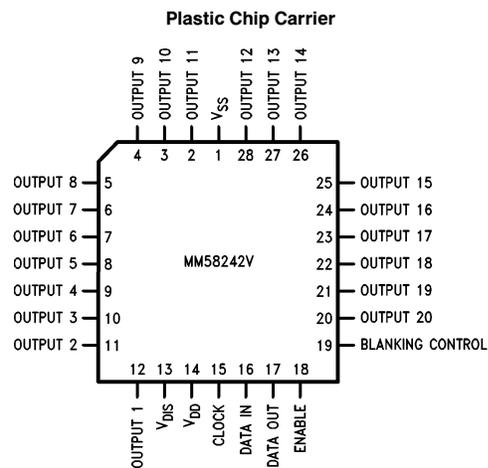
TL/F/7924–8

Top View
Order Number MM58242V
See NS Package Number V28A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58242 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58242 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58242 device, where output 1 (pin 12) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58242, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied, However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58242.

To clear (reset) the display driver at "power on" or any time, the following flushing routine may be used. With the enable signal high, clock in 20 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

In *Figure 5*, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58242 being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58242 is used to provide the grid drive for a 40-digit 2 line 5 × 7 multiplexed vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58248, which does not require an externally generated load signal.
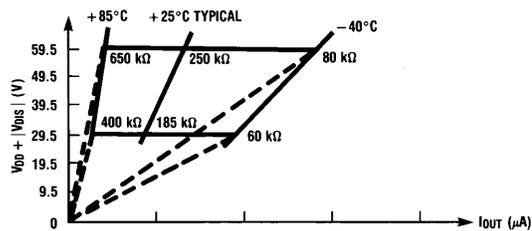

TL/F/7924–3
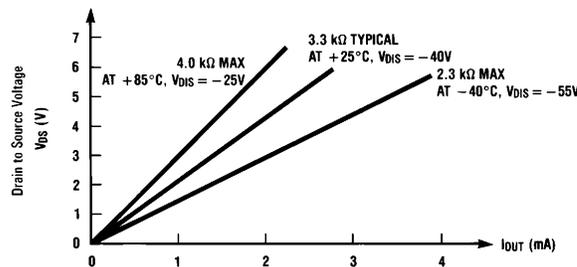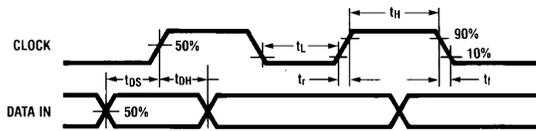
FIGURE 3a. Output Impedance Off

TL/F/7924–4

FIGURE 3b. Output Impedance On

4

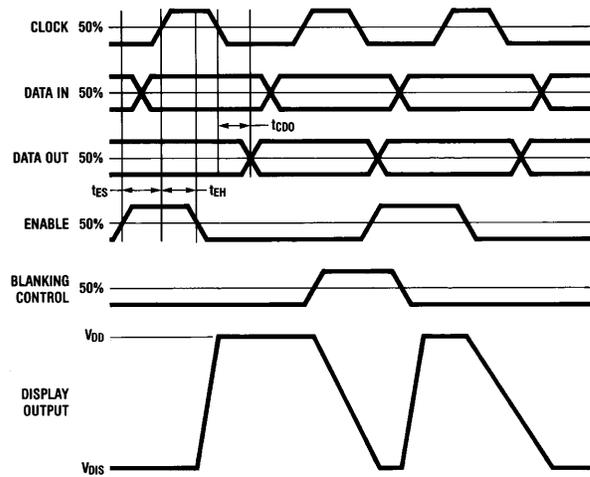# Timing Diagrams

TL/F/7924–5

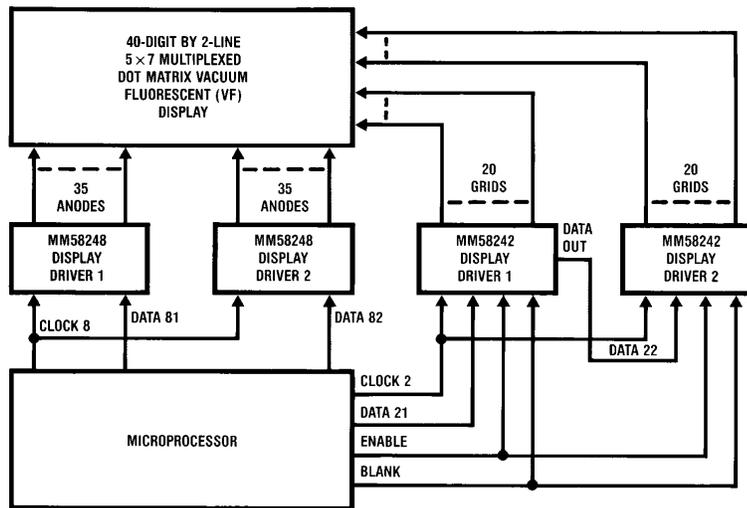For the purposes of AC measurement, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

FIGURE 4. Clock and Data Timings

TL/F/7924–6
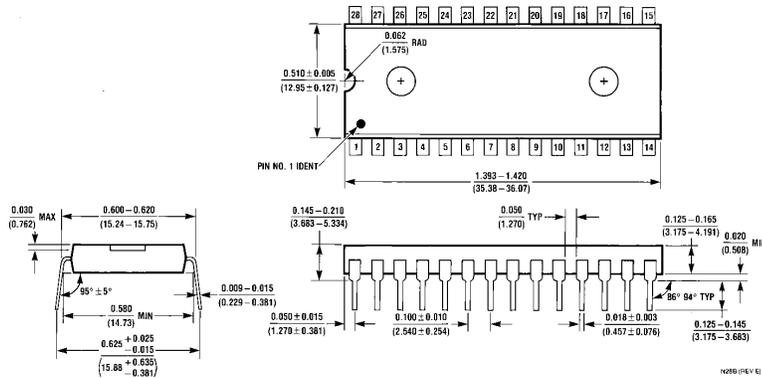
FIGURE 5. MM58242 Timings (Data Format)
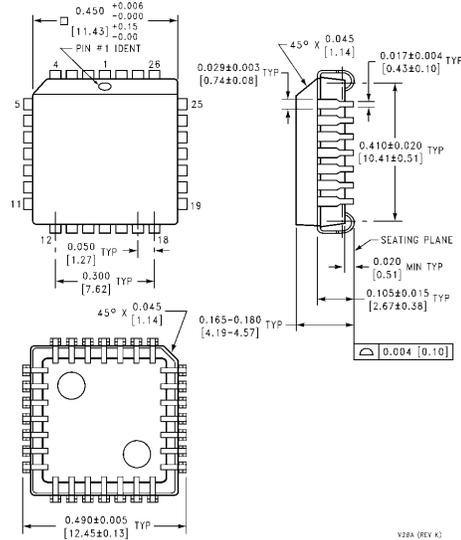
Typical Application

TL/F/7924–7

FIGURE 6. Microprocessor-Controlled Word Processor

Physical Dimensions inches (millimeters)

0.062 RAD
(1.575)

0.510±0.005
(12.95±0.127)

PIN NO. 1 IDENT

1.393−1.420
(35.38−36.07)

0.030 MAX
(0.762)

0.600−0.620
(15.24−15.75)

0.145−0.210
(3.683−5.334)

0.050 TYP
(1.270)

0.125−0.165
(3.175−4.191)

0.020 MIN
(0.508)

95°±5°

0.009−0.015
(0.229−0.381)

0.580 MIN
(14.73)

86° 94° TYP

0.625 +0.025 −0.015
(15.88 +0.635 −0.381)

0.050±0.015
(1.270±0.381)

0.100±0.010
(2.540±0.254)

0.018±0.003
(0.457±0.076)

0.125−0.145
(3.175−3.683)

N28B (REV E)

Molded Dual-In-Line Package (N)
Order Number MM58242N
NS Package Number N28B

0.450 +0.006 −0.000
[11.43] +0.15 −0.00

PIN #1 IDENT

45° X 0.045
[1.14]

0.029±0.003 TYP
[0.74±0.08]

0.017±0.004 TYP
[0.43±0.10]

0.410±0.020 TYP
[10.41±0.51]

SEATING PLANE

0.020 MIN TYP
[0.51]

0.050 TYP
[1.27]

0.300 TYP
[7.62]

0.105±0.015 TYP
[2.67±0.38]

45° X 0.045
[1.14]

0.165−0.180 TYP
[4.19−4.57]

0.004 [0.10]

0.490±0.005 TYP
[12.45±0.13]

V28A (REV K)

Plastic Chip Carrier (V)
Order Number MM58242V
NS Package Number V28A

LIFE SUPPORT POLICY