



October 1987
Revised January 1999

MM74C164 8-Bit Parallel-Out Serial Shift Register

General Description

The MM74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. A high-level input enables the other input which will then determine the state of the flip-flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

Features

- Supply voltage range: 3V to 15V
- Tenth power TTL compatible: drive 2 LPTTL loads
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power: 50 nW (typ.)
- Medium speed operation: 0.8 MHz (typ.) with 10V supply

Applications

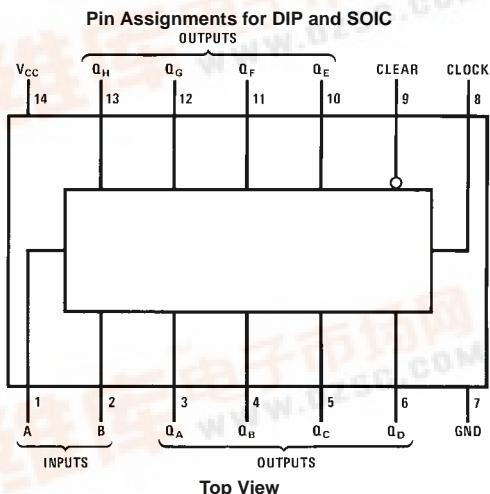
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Ordering Code:

Order Number	Package Number	Package Description
MM74C164M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74C164N	N14A	14-Lead Plastic Dual-In-Line (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

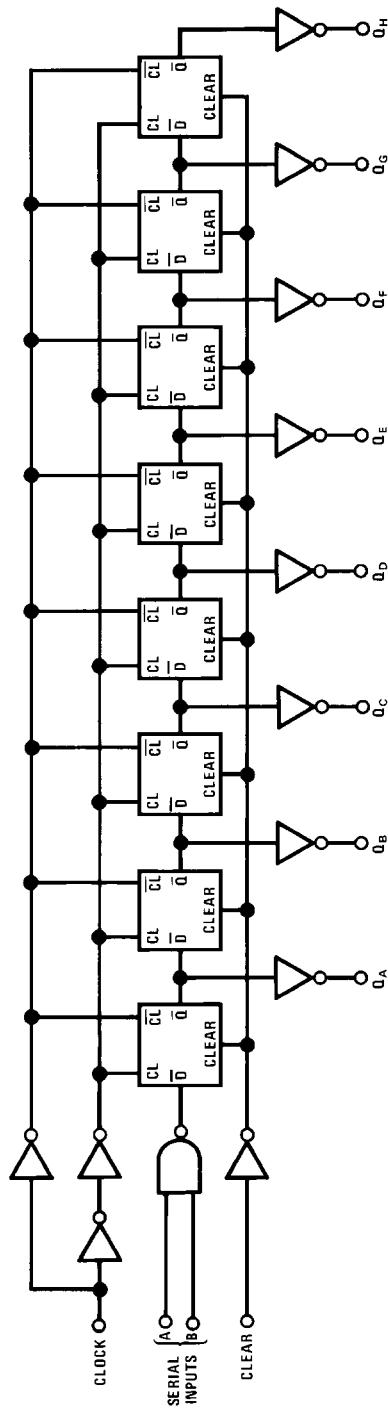


Truth Table

Serial Inputs A and B

Inputs t_n		Output t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

Block Diagram



Absolute Maximum Ratings (Note 1)		Operating V_{CC} Range	3V to 15V
Voltage at Any Pin	-0.3V to V_{CC} + 0.3V	Lead Temperature	
Operating Temperature Range	-40°C to +85°C	(soldering, 10 seconds)	260°C
Storage Temperature Range	-65°C to +150°C		
Absolute Maximum V_{CC}	18V		
Power Dissipation (P_D)			
Dual-In-Line	700 mW		
Small Outline	500 mW		

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

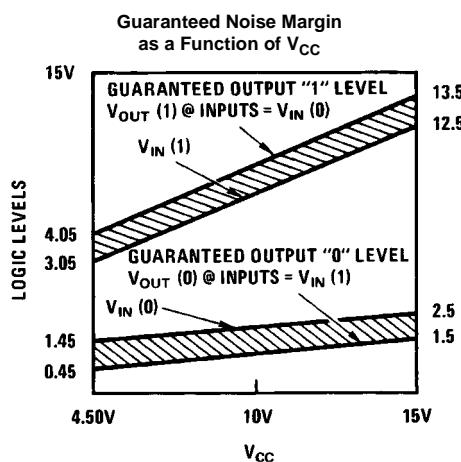
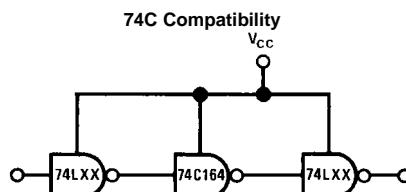
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = +10 \mu A$ $V_{CC} = 10V, I_O = +10 \mu A$			0.5 1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC} = 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_O = -360 \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	8.0			mA

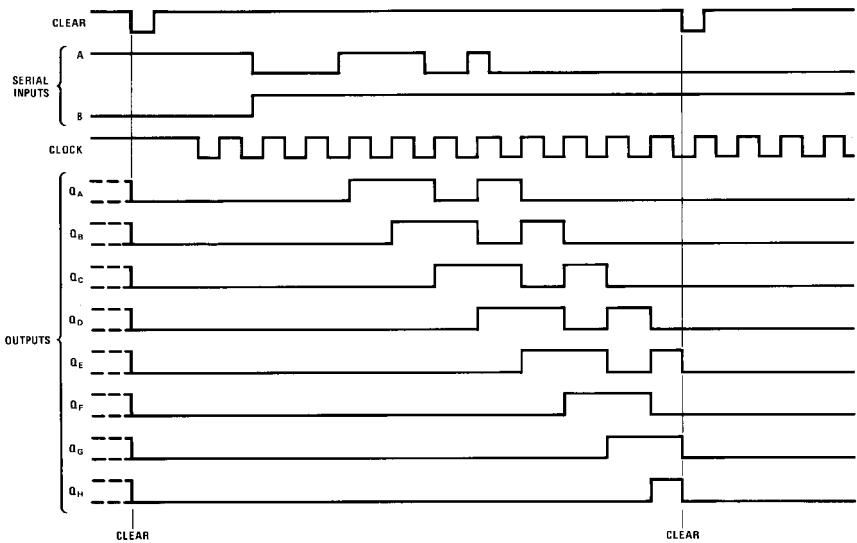
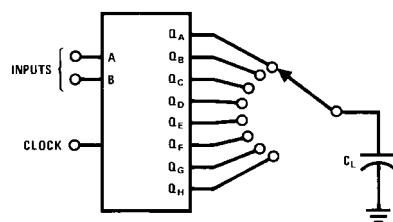
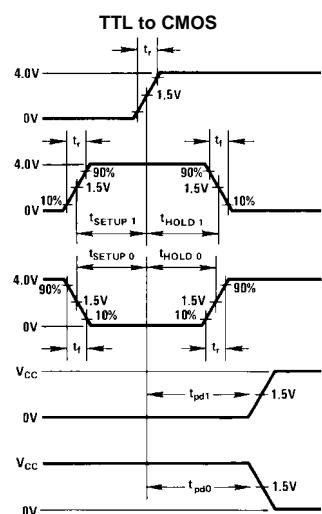
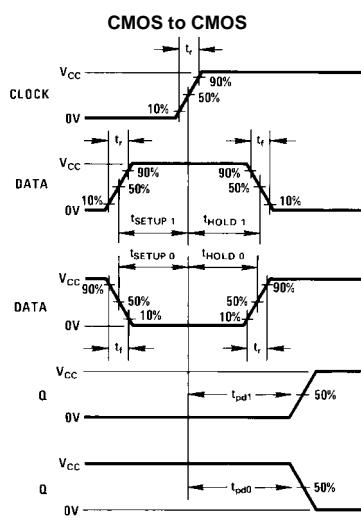
AC Electrical Characteristics (Note 2) $T_A = 25^\circ\text{C}$, $C_L = 50 \text{ pF}$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay Time to a Logical "0" or a Logical "1" from Clock to Q	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		230 90	310 120	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		280 110	380 150	ns ns
t_S	Time Prior to Clock Pulse that Data Must be Present	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	200 80	110 30		ns ns
t_H	Time After Clock Pulse that Data Must be Held	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	0 0	0 0		ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	2.0 5.5	3 8		MHz MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		150 55	250 90	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	15 5			μs μs
C_{IN}	Input Capacitance	Any Input (Note 3)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		140		pF

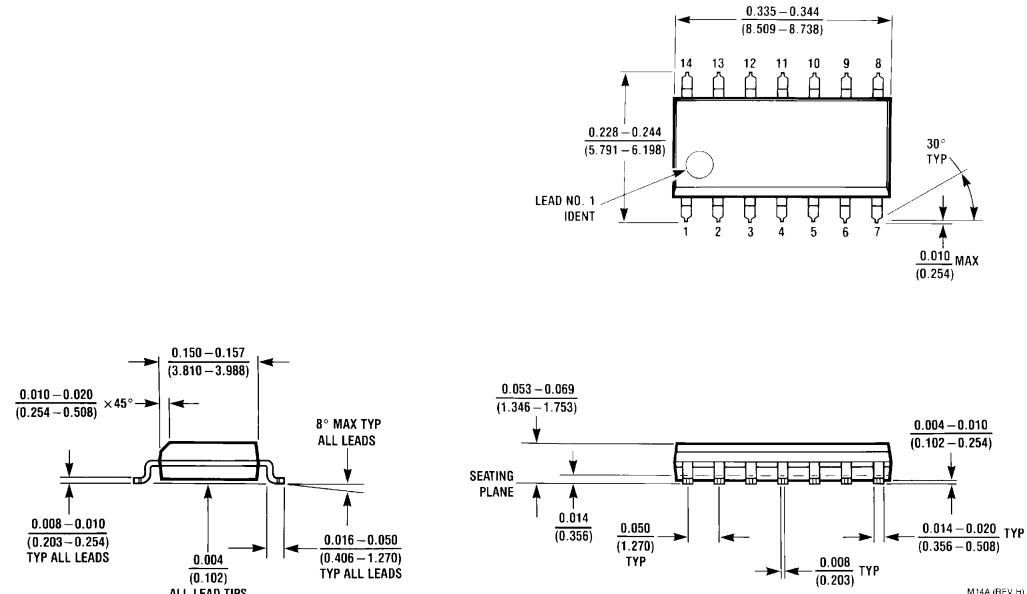
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note AN-90.**Typical Applications**

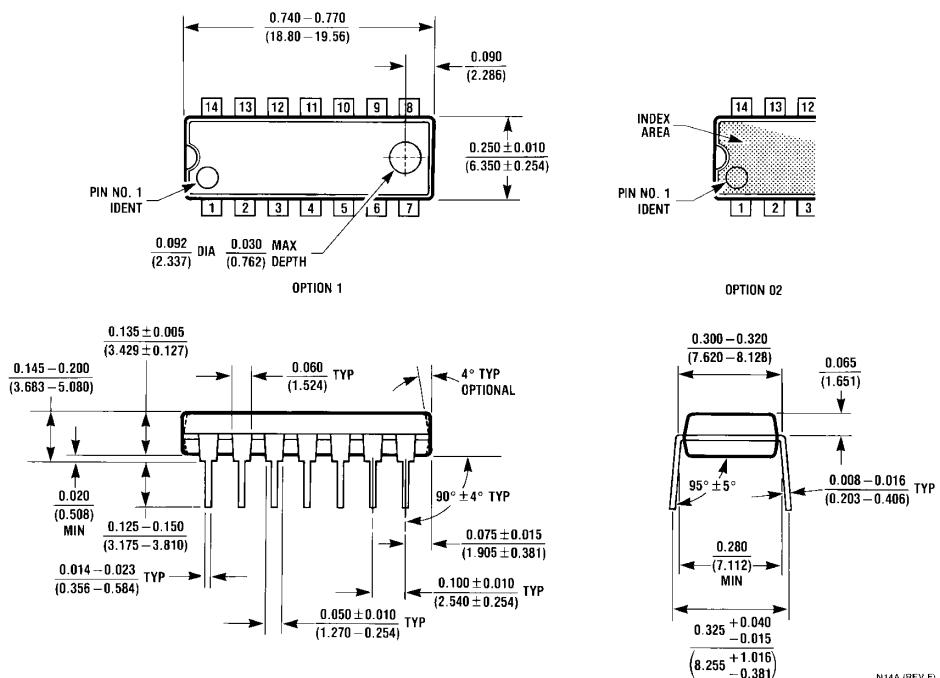
Logic Waveform**AC Test Circuit****Switching Time Waveforms**

$t_r = t_f = 20$ ns

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A**

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