

February 1988

MM54C32/MM74C32 Quad 2-Input OR Gate

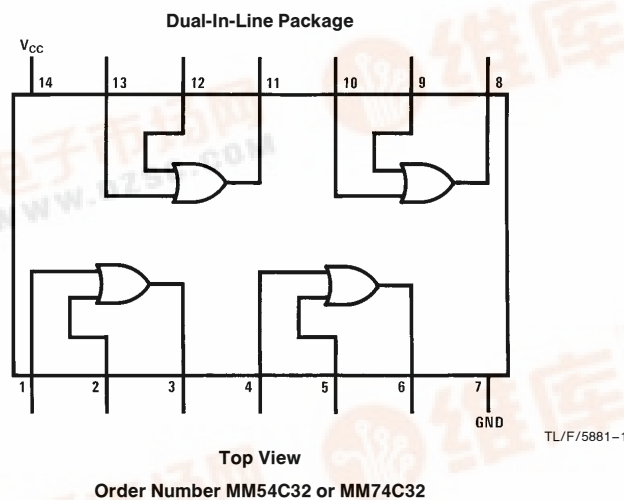
General Description

Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45V V_{CC} (typ.)
- Low power fan out of 2
- TTL compatibility driving 74L

Connection Diagram



MM54C32/MM74C32 Quad 2-Input OR Gate



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C32	−55°C to +125°C
MM74C32	−40°C to +85°C

Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical “1” Input Voltage	$V_{CC} = 5.0V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical “0” Input Voltage	$V_{CC} = 5.0V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_{CC} = 5.0V, I_O = -10 \mu A$	4.5			V
		$V_{CC} = 10V, I_O = -10 \mu A$	9.0			V
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_{CC} = 5.0V, I_O = 10 \mu A$			0.5	V
		$V_{CC} = 10V, I_O = 10 \mu A$			1.0	V
$I_{IN(1)}$	Logical “1” Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical “0” Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	15	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical “1” Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical “0” Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical “1” Output Voltage	54C, $V_{CC} = 4.5V, I_O = -360 \mu A$	2.4			V
		74C, $V_{CC} = 4.75V, I_O = -360 \mu A$	2.4			V
$V_{OUT(0)}$	Logical “0” Output Voltage	54C, $V_{CC} = 4.5V, I_O = 360 \mu A$			0.4	V
		74C, $V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V
OUTPUT DRIVE (see 54C/74C Family Characteristics Data Sheet) $T_A = 25^{\circ}C$ (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$	8.0	16		mA

Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified

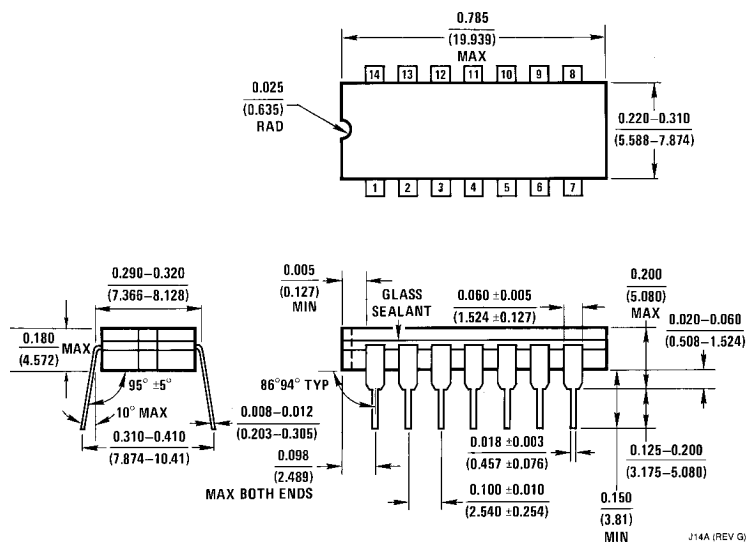
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0\text{V}$		80	150	ns
		$V_{CC} = 10\text{V}$		35	70	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Gate (Note 3)		15		pF

*AC Parameters are guaranteed by DC correlated testing.

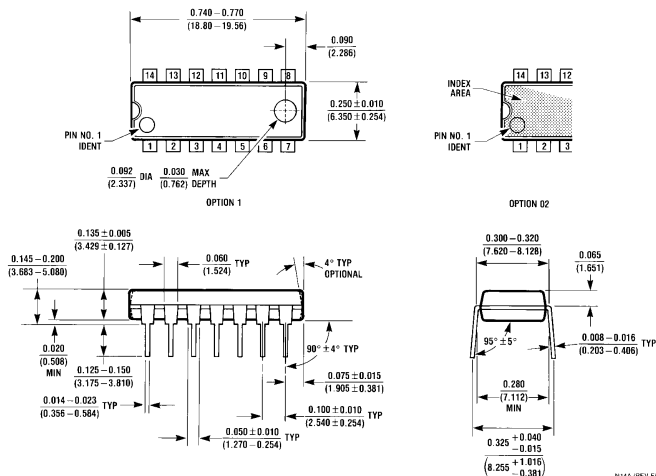
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C32J or MM74C32J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 13th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408