National Semiconductor

November 1990

MM74C908/MM74C918 Dual CMOS 30V Relay Driver

General Description

The MM74C908 and MM74C918 are general purpose dual high voltage drivers, each capable of sourcing a minimum of 250 mA at $V_{OUT} = V_{CC} - 3V$, and $T_J = 65°C$.

The MM74C908 and MM74C918 consist of two CMOS NAND gates driving an emitter follower Darlington output to achieve high current drive and high voltage capabilities. In the "OFF" state the outputs can withstand a maximum of −30V across the device. These CMOS drivers are useful in interfacing normal CMOS voltage levels to driving relays, regulators, lamps, etc.

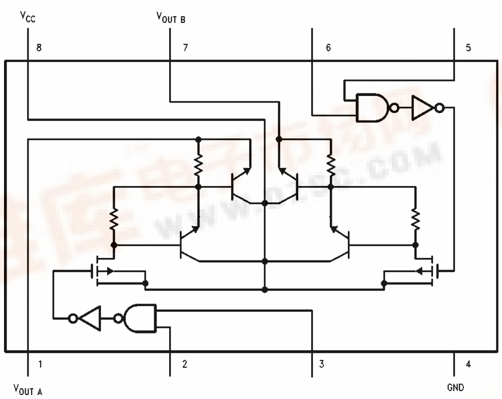
Features

- Wide supply voltage range 3V to 18V
- High noise immunity 0.45 V_{CC} (typ.)
- Low output "ON" resistance 8Ω (typ.)
- High voltage −30V
- High current 250 mA

Connection Diagrams

Dual-In-Line Package

MM74C908



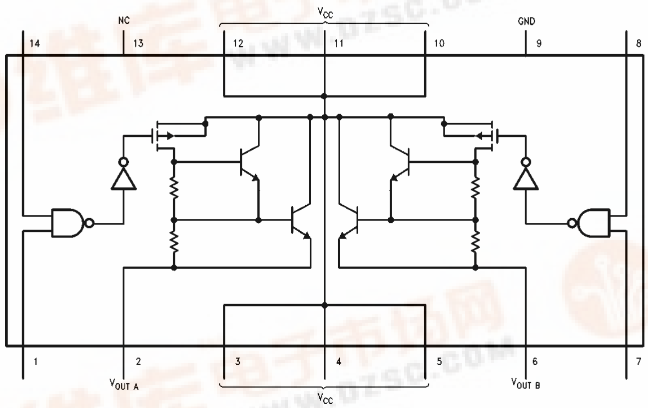
TL/F/5912–1

Top View

Order Number MM74C908

Dual-In-Line Package

MM74C918



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Top View

Order Number MM74C918

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MM74C908/MM74C918 Dual CMOS 30V Relay Driver

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Input Pin	$-0.3V$ to $V_{CC} +0.3V$
Voltage at any Output Pin	32V
Operating Temperature Range MM74C908/MM74C918	$-40°C$ to $+85°C$
Operating V_{CC} Range	4V to 18V
Absolute Maximum V_{CC}	19V
I_{SOURCE}	500 mA
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
Power Dissipation (P_D)	Refer to Maximum Power Dissipation vs Ambient Temperature Graph

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$, Outputs Open Circuit		0.05	15	μA
	Output "OFF" Voltage	$V_{IN} = V_{CC}$, $I_{OUT} = -200\ \mu A$		-30		V
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage MM74C908/MM74C918	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage MM74C908/MM74C918	$V_{CC} = 4.75V$			0.8	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage	$I_{OUT} = -300$ mA, $V_{CC} \geq 5V$, $T_J = 25°C$ $I_{OUT} = -250$ mA, $V_{CC} \geq 5V$, $T_J = 65°C$ $I_{OUT} = -175$ mA, $V_{CC} \geq 5V$, $T_J = 150°C$	$V_{CC}-2.7$ $V_{CC}-3.0$ $V_{CC}-3.15$	$V_{CC}-1.8$ $V_{CC}-1.9$ $V_{CC}-2.0$		V V V
R_{ON}	Output Resistance	$I_{OUT} = -300$ mA, $V_{CC} \geq 5V$, $T_J = 25°C$ $I_{OUT} = -250$ mA, $V_{CC} \geq 5V$, $T_J = 65°C$ $I_{OUT} = -175$ mA, $V_{CC} \geq 5V$, $T_J = 150°C$		6.0 7.5 10	9.0 12 18	Ω Ω Ω
	Output Resistance Coefficient			0.55	0.80	%/°C
θ_{JA}	Thermal Resistance MM74C908/MM74C918	(Note 3) (Note 3)		100 45	110 55	°C/W °C/W

AC Electrical Characteristics*

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logical "1"	$V_{CC} = 5V$, $R_L = 50\Omega$, $C_L = 50$ pF, $T_A = 25°C$ $V_{CC} = 10V$, $R_L = 50\Omega$, $C_L = 50$ pF, $T_A = 25°C$		150 65	300 120	ns ns
t_{pd0}	Propagation Delay to a Logic "0"	$V_{CC} = 5V$, $R_L = 50\Omega$, $C_L = 50$ pF, $T_A = 25°C$ $V_{CC} = 10V$, $R_L = 50\Omega$, $C_L = 50$ pF, $T_A = 25°C$		2.0 4.0	10 20	μs μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

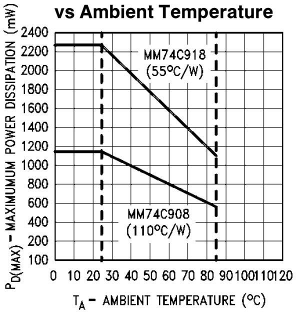
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

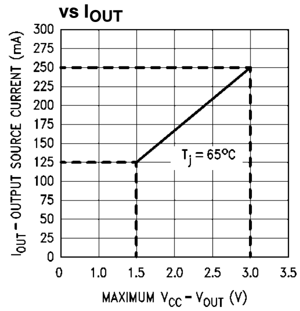
Note 3: θ_{JA} measured in free air with device soldered into printed circuit board.

Typical Performance Characteristics

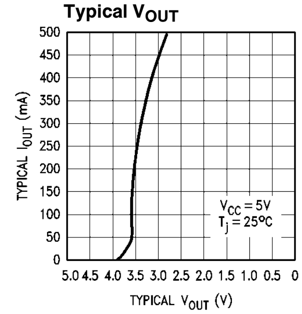
Maximum Power Dissipation vs Ambient Temperature



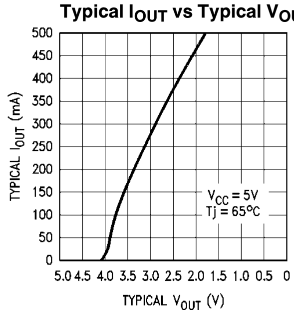
Maximum $V_{CC} - V_{OUT}$ vs I_{OUT}



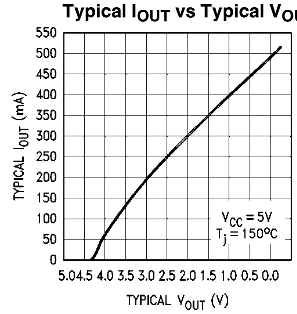
Typical I_{OUT} vs Typical V_{OUT}



Typical I_{OUT} vs Typical V_{OUT}

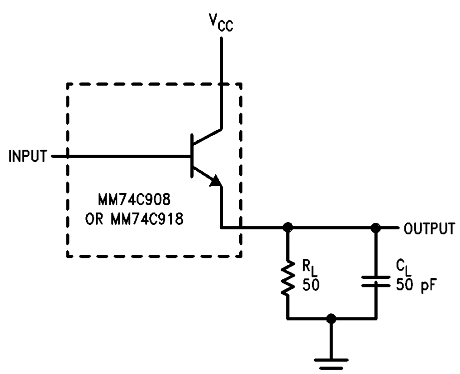


Typical I_{OUT} vs Typical V_{OUT}



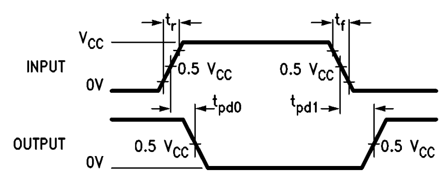
TL/F/5912–3

AC Test Circuit



TL/F/5912–4

Switching Time Waveforms



TL/F/5912–5

$t_r = t_f = 20$ ns

Power Considerations

Calculating Output "ON" Resistance ($R_L > 18\Omega$)

The output "ON" resistance, R_{ON}, is a function of the junction temperature, T_J, and is given by:

$$R_{ON} = 9\,(T_J - 25)\,(0.008) + 9 \tag{1}$$

and T_J is given by:

$$T_J = T_A + P_{DAV}\,\theta_{JA}, \tag{2}$$

where T_A = ambient temperature, θ_{JA} = thermal resistance, and P_{DAV} is the average power dissipated within the device. P_{DAV} consists of normal CMOS power terms (due to leakage currents, internal capacitance, switching, etc.) which are insignificant when compared to the power dissipated in the outputs. Thus, the output power term defines the allowable limits of operation and includes both outputs, A and B. P_D is given by:

$$P_D = I_{OA}{}^2\,R_{ON} + I_{OB}{}^2\,R_{ON}, \tag{3}$$

where I_O is the output current, given by:

$$I_O = \frac{V_{CC} - V_L}{R_{ON} + R_L} \tag{4}$$

V_L is the load voltage.

The average power dissipation, P_{DAV}, is a function of the duty cycle:

$$P_{DAV} = I_{OA}{}^2\,R_{ON}\,(\text{Duty Cycle}_A) + I_{OB}{}^2\,R_{ON}\,(\text{Duty Cycle}_B) \tag{5}$$

where the duty cycle is the % time in the current source state. Substituting equations (1) and (5) into (2) yields:

$$T_J = T_A + \theta_{JA}\,[9\,(T_J - 25)\,(0.008) + 9]\,[I_{OA}{}^2\,(\text{Duty Cycle}_A) + I_{OB}{}^2\,(\text{Duty Cycle}_B)] \tag{6a}$$

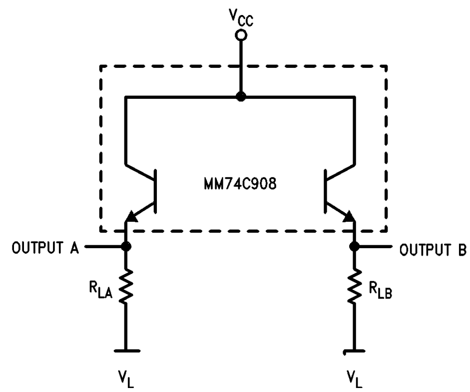
simplifying:

$$T_J = \frac{T_A + 7.2\,\theta_{JA}\,[I_{OA}{}^2\,(\text{Duty Cycle}_A) + I_{OB}{}^2\,(\text{Duty Cycle}_B)]}{1 - 0.072\,\theta_{JA}\,[I_{OA}{}^2\,(\text{Duty Cycle}_A) + I_{OB}{}^2\,(\text{Duty Cycle}_B)]}$$

Equations (1), (4), and (6b) can be used in an iterative method to determine the output current, output resistance and junction temperature.

Applications

(See AN-177 for applications)



TL/F/5912–6

For example, let V_{CC} = 15V, R_{LA} = 100Ω, R_{LB} = 100Ω, V_L = 0V, T_A = 25°C, θ_{JA} = 110°C/W, Duty Cycle$_A$ = 50%, Duty Cycle$_B$ = 75%.

Assuming R_{ON} = 11Ω, then:

$$I_{OA} = \frac{V_{CC} - V_L}{R_{ON} + R_{LA}} = \frac{15}{11 + 100} = 135.1\text{ mA},$$

$$I_{OB} = \frac{V_{CC} - V_L}{R_{ON} + R_{LB}} = 135.1\text{ mA}$$

and

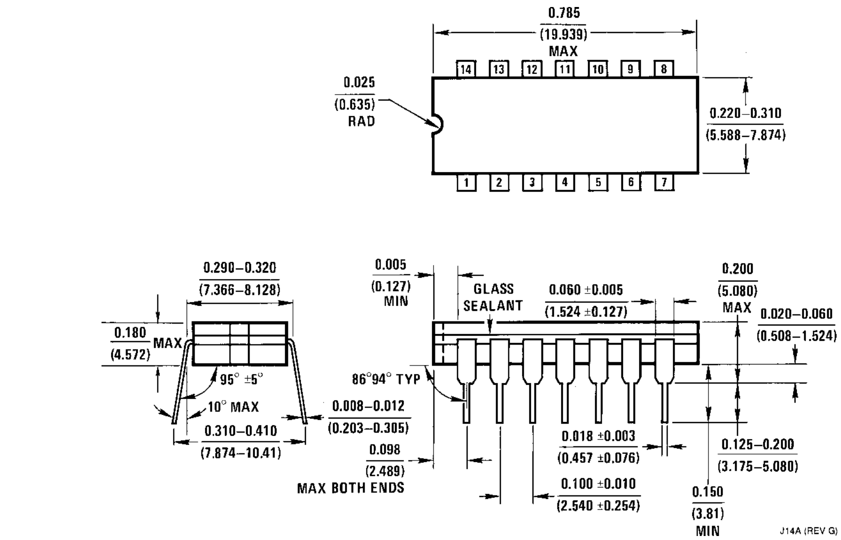
$$T_J = \frac{T_A + 7.2\,\theta_{JA}\,[I_{OA}{}^2\,(\text{Duty Cycle}_A) + I_{OB}{}^2\,(\text{Duty Cycle}_B)]}{1 - 0.072\,\theta_{JA}\,[I_{OA}{}^2\,(\text{Duty Cycle}_A) + I_{OB}{}^2\,(\text{Duty Cycle}_B)]}$$

$$T_J = \frac{25 + (7.2)\,(110)\,[(0.1351)^2\,(0.5) + (0.1351)^2\,(0.75)]}{1 - (0.072)\,(110)\,[(0.1351)^2\,(0.5) + (0.1351)^2\,(0.75)]}$$

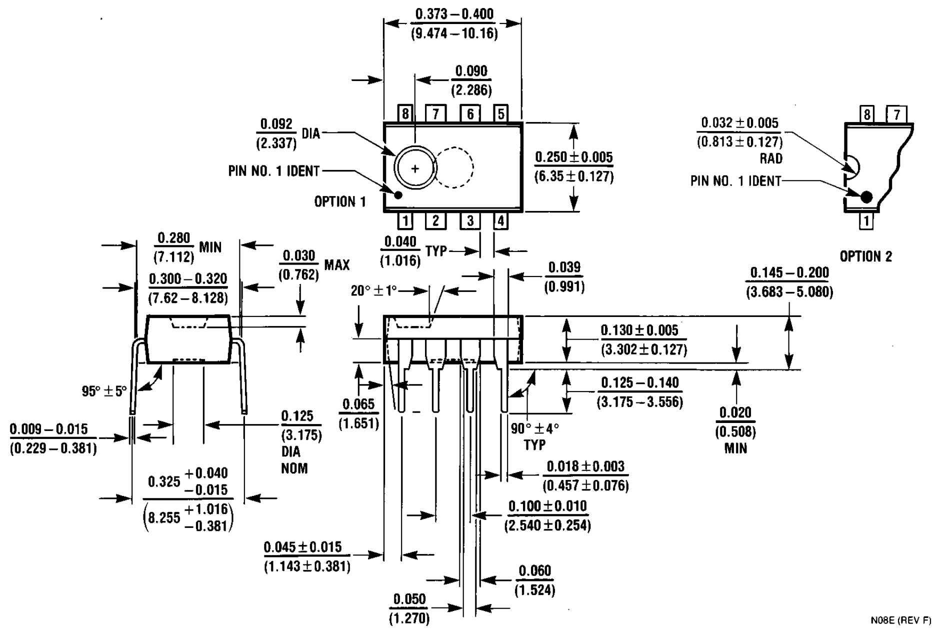
T_J = 52.6°C

and $R_{ON} = 9\,(T_J - 25)\,(0.008) + 9$
$= 9(52.6 - 25)\,(0.008) + 9 = 11\Omega$

Physical Dimensions inches (millimeters)

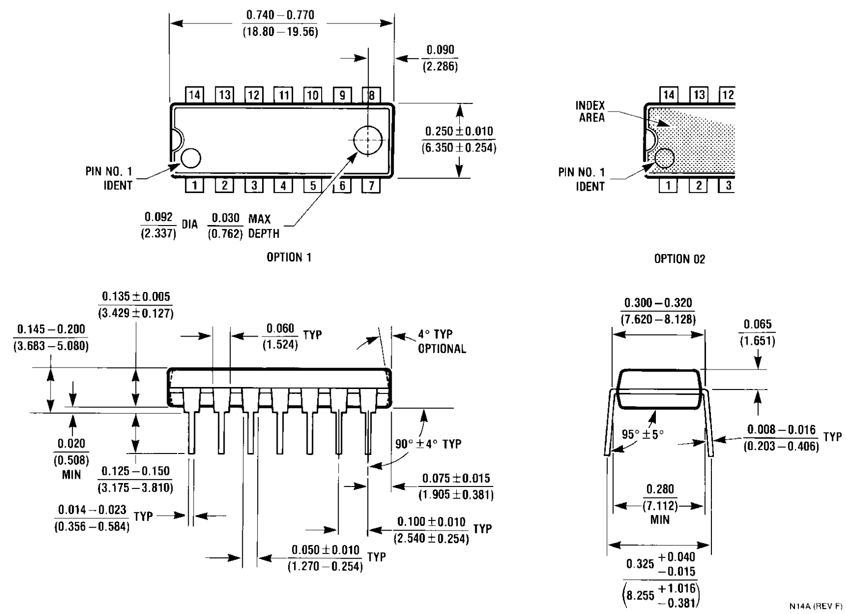


Ceramic Dual-In-Line Package (J)
Order Number MM74C918J
NS Package Number J14A



Molded Dual-In-Line Package (N)
Order Number MM74C908N
NS Package Number N08E

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM74C918N
NS Package Number N14A

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