

September 1983 Revised February 1999

MM74HC00 Quad 2-Input NAND Gate

General Description

The MM74HC00 NAND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to

static discharge by internal diode clamps to $\ensuremath{\text{V}_{\text{CC}}}$ and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 µA maximum (74HC Series)
- Low input current: 1 µA maximum
- Fanout of 10 LS-TTL loads

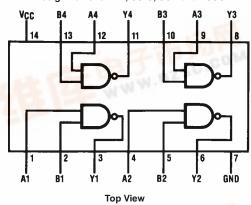
Ordering Code:

Order Number	Package Number	Package Description
MM74HC00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Logic Diagram

Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input Voltage (V _{IN})	-1.5 to V _{CC} +1.5V
DC Output Voltage (V _{OUT})	-0.5 to V_{CC} +0.5 V
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T _L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage	0	V_{CC}	V
(V_{IN}, V_{OUT})			
Operating Temperature Range (T _A)	-40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) $V_{CC} = 2V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: – 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	v _{cc}	T _A = 25°C		$T_A = -40 \text{ to } 85^{\circ}\text{C}$	$T_A = -55 \text{ to } 125^{\circ}\text{C}$	Units
Cynnbon			- 66	Тур		Onics		
V _{IH}	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μΑ
	Current							
I _{CC}	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	6.0V		2.0	20	40	μΑ
	Supply Current	$I_{OUT} = 0 \mu A$						

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

 $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

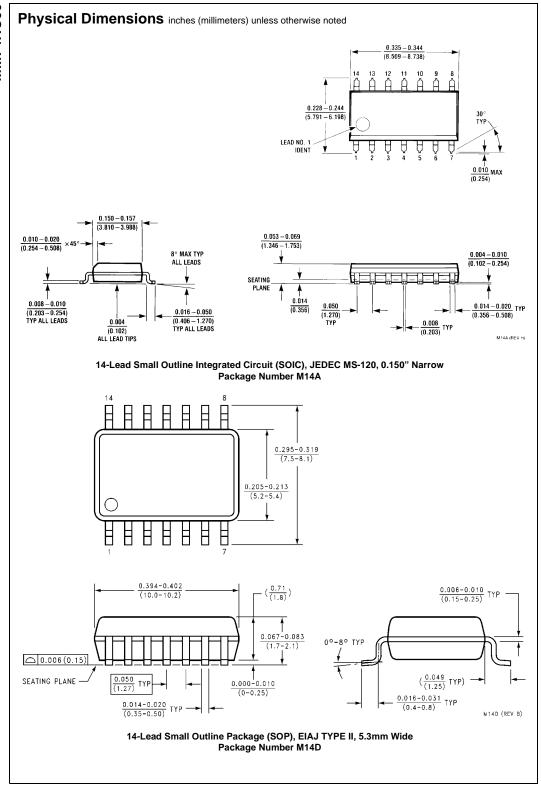
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
t _{PHL} , t _{PLH}	Maximum Propagation		8	15	ns
	Delay				

AC Electrical Characteristics

 $V_{CC} = 2.0 \text{V}$ to 6.0V, $C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)

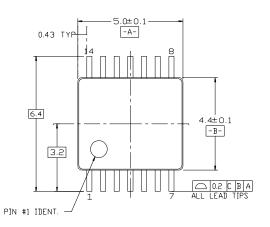
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		$T_A = -40 \text{ to } 85^{\circ}\text{C}$	T _A = -55 to 125°C	Units
Cymbol			•66	Тур	Typ Guaranteed Limits			Onics
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	45	90	113	134	ns
	Delay		4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t _{TLH} , t _{THL}	Maximum Output Rise		2.0V	30	75	95	110	ns
	and Fall Time		4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C _{PD}	Power Dissipation	(per gate)		20				pF
	Capacitance (Note 5)							
C _{IN}	Maximum Input			5	10	10	10	pF
	Capacitance							

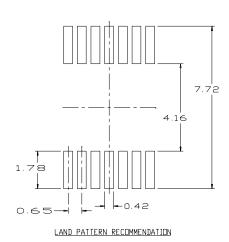
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC}$.

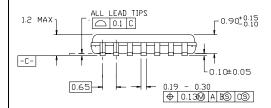


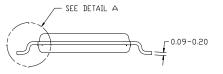
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14LD, TSSOP, JEDEC MO-153, 4.4MM WIDE



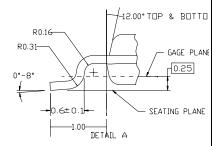






NOTES

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ABJREF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)กคดก (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{\text{J.d92}}{(2.337)} \text{ DIA}$ 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 0.135 ± 0.005 0.300 - 0.320 (3.429 ± 0.127) (7.620 - 8.128)0.145 - 0.200 $\frac{0.060}{(1.524)}$ TYP 4° TYP (1.651) (3.683 - 5.080)* $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 95° ± 5° 0.020 (0.508)0.125 - 0.150 0.075 ± 0.015 0.280 0.014-0.023 TYP (7.112) MIN $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$ 0.325 +0.040 -0.015 (8.255 + 1.016) -0.381

14-Lead Plastic Dual-In Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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- 2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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N14A (REV F)