FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

MM80C95 • MM80C97 • MM80C98
3-STATE Hex Buffers • 3-STATE Hex Inverters

General Description

The MM80C95, MM80C97 and MM80C98 gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The MM80C95 and the MM80C97 convert CMOS or TTL outputs to 3-STATE outputs with no logic inversion, the MM80C98 provides the logical opposite of the input signal. The MM80C95 has common 3-STATE controls for all six devices. The MM80C97 and the MM80C98 have two 3-STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 V_{CC} (typ.)
- TTL compatible: Drive 1 TTL Load

Applications

- Bus drivers: Typical propagation delay into 150 pF load is 40 ns

Ordering Code:

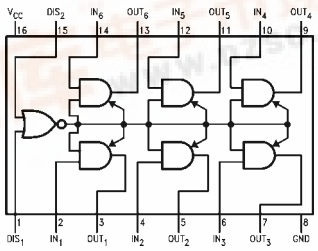
Order Number	Package Number	Package Description
MM80C95N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
MM80C97M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
MM80C97N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
MM80C98N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagrams

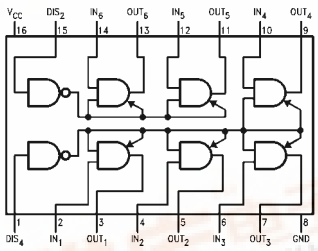
Pin Assignments for DIP

MM80C95



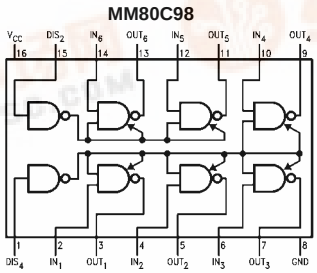
Top View

MM80C97



Top View

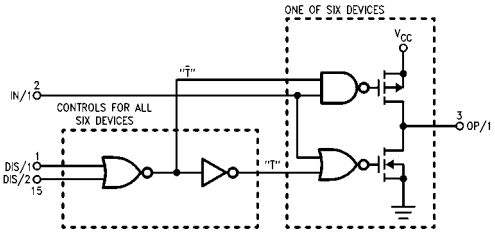
MM80C98



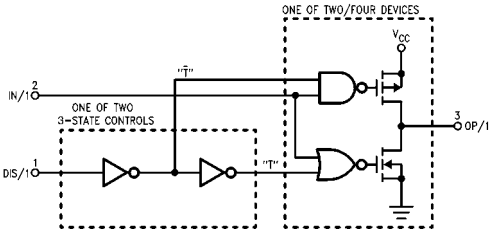
Top View

Schematic Diagrams

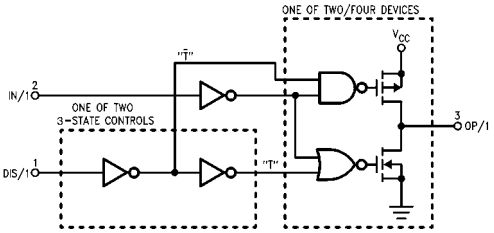
MM80C95 3-STATE



MM80C97 3-STATE



MM80C98 3-STATE



Truth Tables

MM80C95

Disable DIS_1	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM80C97

Disable DIS_4	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
X	1	X	H-z (Note 1)
1	X	X	H-z (Note 2)

MM80C98

Disable DIS_4	Input DIS_2	Input	Output
0	0	0	1
0	0	1	0
X	1	X	H-z (Note 1)
1	X	X	H-z (Note 2)

X = Irrelevant

Note 1: Output 5–6 only

Note 2: Output 1–4 only

Absolute Maximum Ratings (Note 3)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Power Supply Voltage (V_{CC})	18V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 3: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V	4.5			V
		V_{CC} = 10V	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V			0.5	V
		V_{CC} = 10V			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current		−1.0	−0.005		µA
I_{OZ}	Output Current in High	V_{CC} = 15V, V_O = 15V		0.005	1.0	µA
	Impedance State	V_{CC} = 15V, V_O = 0V	−1.0	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V		0.01	15	µA
TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V,	2.4			V
		I_O = −1.6 mA				
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V,			0.4	V
		I_O = 1.6 mA				
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, $V_{IN(1)}$ = 5V	−4.35			mA
		T_A = 25°C, V_{OUT} = 0V				
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V	−20			mA
		T_A = 25°C, V_{OUT} = 0V				
I_{SINK}	Output Sink Current	V_{CC} = 5V, $V_{IN(0)}$ = 0V	4.35			mA
		T_A = 25°C, V_{OUT} = V_{CC}				
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V	20			mA
		T_A = 25°C, V_{OUT} = V_{CC}				

AC Electrical Characteristics (Note 4)

$T_A = 25^\circ C$, $C_L = 50$ pF, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM80C95, MM80C97	$V_{CC} = 5V$		60	100	ns
		$V_{CC} = 10V$		25	40	ns
	MM80C98	$V_{CC} = 5V$		70	150	ns
		$V_{CC} = 10V$		35	75	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM80C95, MM80C97	$V_{CC} = 5V$, $C_L = 150$ pF		85	160	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		40	80	ns
	MM80C98	$V_{CC} = 5V$, $C_L = 150$ pF		95	210	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		45	110	ns
t_{1H}, t_{0H}	Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0")	$R_L = 10k$, $C_L = 5$ pF				
	MM80C95	$V_{CC} = 5V$		80	135	ns
		$V_{CC} = 10V$		50	90	ns
	MM80C97	$V_{CC} = 5V$		70	125	ns
		$V_{CC} = 10V$		50	90	ns
	MM80C98	$V_{CC} = 5V$		90	170	ns
		$V_{CC} = 10V$		70	125	ns
t_{H1}, t_{H0}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	$R_L = 10k$, $C_L = 50$ pF				
	MM80C95	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
	MM80C96	$V_{CC} = 5V$		130	225	ns
		$V_{CC} = 10V$		60	110	ns
	MM80C98	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
C_{IN}	Input Capacitance	Any Input (Note 5)		5.0		pF
C_{OUT}	Output Capacitance 3-STATE	Any Output (Note 5)		11		pF
C_{PD}	Power Dissipation Capacitance	(Note 6)		60		pF

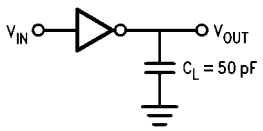
Note 4: AC Parameters are guaranteed by DC correlated testing.

Note 5: Capacitance is guaranteed by periodic testing.

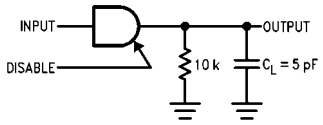
Note 6: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note AN-90.

AC Test Circuits and Switching Time Waveforms

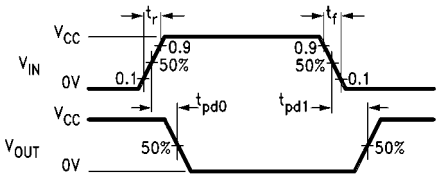
t_{pd0}, t_{pd1}



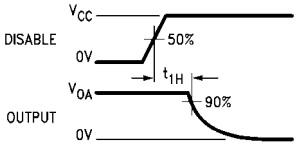
t_{1H} and t_{H1}



CMOS to CMOS

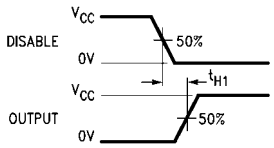


t_{1H}

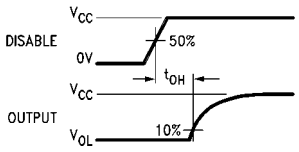


AC Test Circuits and Switching Time Waveforms (Continued)

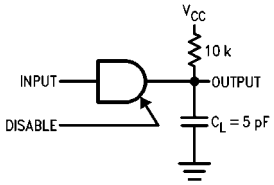
t_{H1}



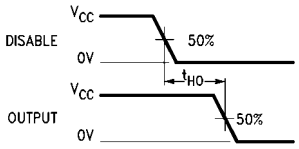
t_{0H}



t_{0H} and t_{H0}



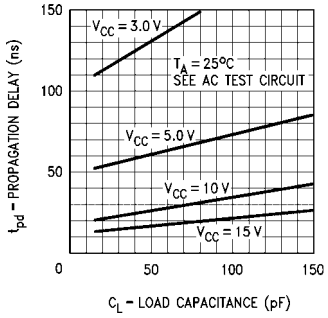
t_{H0}



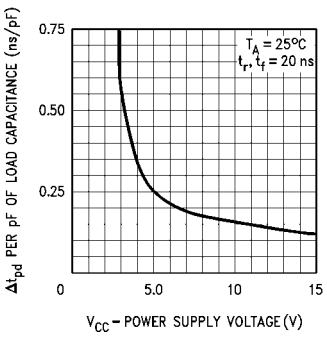
Note: Delays measured with input t_r, $t_f \leq 20$ ns.

Typical Performance Characteristics

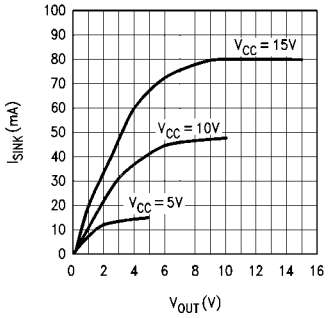
Propagation Delay vs Load Capacitance



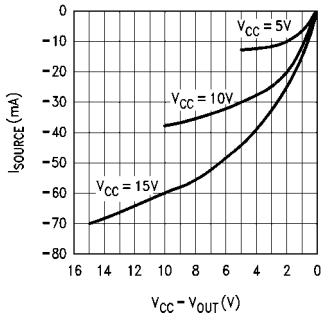
Δt_{pd}/pF vs Power Supply Voltage



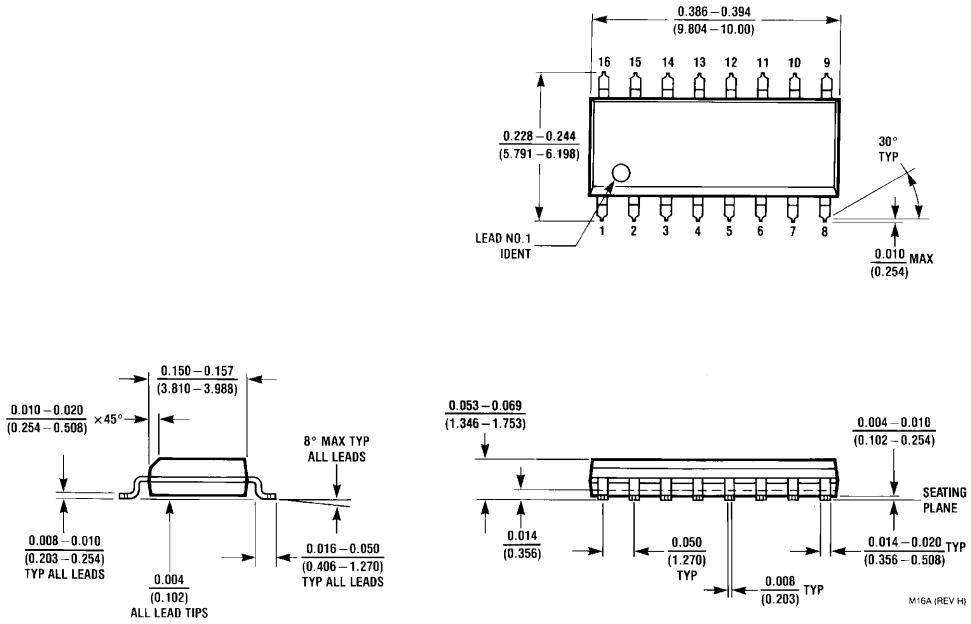
N-Channel Output Drive at 25°C



P-Channel Output Drive at 25°C

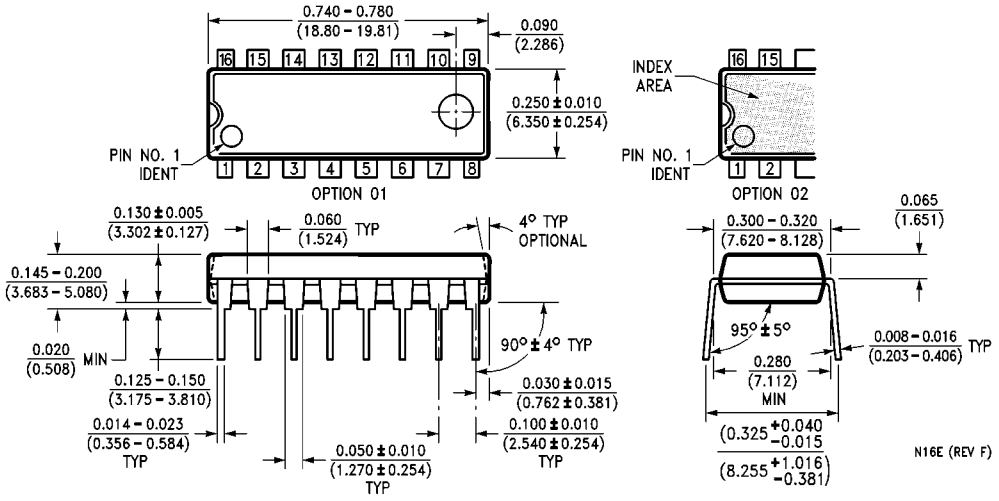


Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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