❑ MN103000

Type	MN103000
Command ROM (×64-Bit)	16 KB
Data RAM (×32-Bit)	16 KB
Minimum Instruction Execution Time	17 ns (at 3.3 V, 60 MHz)
Interrupts	• RESET • IRQ × 8 • NMI • Timer × 28 • SIF × 4 • DMAC × 4 • WDT • A/D • System error
Timer Counter	**Timer Counter 0 to 3: 32-Bit × 1** (Interval Timer, Event Count, Timer Output, Interrupt, Clock Source for Serial I/F, A/D Conversion Trigger) Clock Source: IOCLK, External Clock Input, Underflow of Timer Counter Interrupt Source: Underflow of Timer Counter 0, 1, 2, 3 **Timer Counter 4 to 7: 32-Bit × 1** (Interval Timer, Event Count, Timer Output, Interrupt, Clock Source for Serial I/F) Clock Source: IOCLK, External Clock Input, Underflow of Timer Counter Interrupt Source: Underflow of Timer Counter 4, 5, 6, 7 * Configuration of Each of Timer Counters 0 to 3 and Timer Counters 4 to 7 can be Changed to 8-, 16- and 24-Bit Timer Counters **Timer Counter 8: 16-Bit × 1** (Interval Timer, Event Count, Toggle Output (2 Lines), PWM Output, One-Shot Output, Input Capture (2 Lines), Interrupt, DMA Start, Generation of Timer Synchronous Output Timing) Clock Source: IOCLK, External Clock Input, Underflow of Timer Counter Interrupt Source: Overflow of Timer Counter 8, Coincidence with Compare Capture (2 Lines) or at Capture **Timer Counter 9: 16-Bit × 1** (Interval Timer, Event Count, Toggle Output (2 Lines), PWM Output, High-Speed PWM Output, One-Shot Output, Input Capture (2 Lines), Interrupt, DMA Start, Generation of Timer Synchronous Output Timing) Clock Source: IOCLK, External Clock Input, Underflow of Timer Counter Interrupt Source: Overflow of Timer Counter 9, Coincidence with Compare Capture (2 Lines) or at Capture **Timer Counter 10: 16-Bit × 1** (Interval Timer, Event Count, Toggle Output (3 Lines), PWM Output (2 Lines), One-shot Output, Input Capture (3 Lines), Interrupt, DMA Start, 2-Phase Encode) Clock Source: IOCLK, External Clock Input, 2-Phase Encode, Underflow of Timer Counter Interrupt Source: Overflow of Timer Counter 10, Underflow, Coincidence with Compare Capture (3 Lines) or at Capture **Timer Counter 11: 16-Bit × 1** (Interval Timer, Event Count, Toggle Output (4 Lines), PWM Output, Inter-Offset 3-Phase PWM Output, One-shot Output, Input Capture (4 Lines), Interrupt, DMA Start, 2-Phase Encode) Clock Source: IOCLK, External Clock Input, 2-Phase Encode, Underflow of Timer Counter Interrupt Source: Overflow of Timer Counter 11, Underflow, Coincidence with Compare Capture (4 Lines) or at Capture **Timer Counter 12: 16-Bit × 1** (Interval Timer, Event Count, Toggle Output (4 Lines), PWM Output (3 Lines), One-Shot Output, Input Capture (4 Lines), Interrupt, 2-Phase Encode) Clock Source: IOCLK, External Clock Input, 2-Phase Encode, Underflow of Timer Counter Interrupt Source: Overflow of Timer Counter 12, Underflow, Coincidence with Compare Capture (4 Lines) or at Capture **Watchdog Timer: 16-Bit to 25-Bit × 1**

Serial Interface			**Serial 0, 1: 7-Bit, 8-Bit × 2** (Clock Synchronous mode, Start-Stop Synchronous Mode, I^2C Mode) Clock Source . (Clock Synchronous Mode, Start-Stop Synchronous Mode) IOCLK, the Underflow of Timer Counter, External Clock (I^2C Mode) IOCLK, the Underflow of Timer Counter
I/O Pins	**I/O**	**51**	• Common use 51
	Output	**25**	• Common use 25
	Input	**13**	• Common use 13
A/D Inputs			10-Bit × 8ch
PWM			16-Bit × 5ch
ICR			16-Bit × 15ch (Common with OCR)
OCR			16-Bit × 15ch (Common with ICR)
Timer Synchronous Output			4-Bit (Synchronous Output) × 2ch
DMAC			4ch
Package			QFP160-P-2828B

Electrical Characteristics

Supply Current

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Operating Supply Current	IDD1	VDD, PVDD, AVDD = 3 3 V VI = VDD or VSS Fosc = 15 0 MHz FRQS pin = Hi level Output released			250	mA
Supply current at SLEEP	IDD2	VDD, PVDD, AVDD = 3 465 V VI = VDD or VSS Fosc = 15 0 MHz FRQS pin = Hi level Output released			50	mA
Supply current at HALT	IDD3	VDD, PVDD, AVDD = 3 465 V VI = VDD or VSS Fosc = 15 0 MHz FRQS pin = Hi level Output released			5	mA
Supply current at stopping	IDD4	VDD, PVDD, AVDD = 3 465 V VI = VDD or VSS Fosc = Oscillation stopped Output released			300	µA

(Ta = –20 °C to + 70 °C)

See the next page for pin assignment and electrical characteristics (continue).

Electrical Characteristics (Continue)

A/D Conversion Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute Error		VREF+ = 3 3 V, VREF- = 0 0 V			±7	LSB
A/D conversion relative Error		A/D conversion clock = 5 MHz			±5	LSB
A/D conversion time			2 8			µs

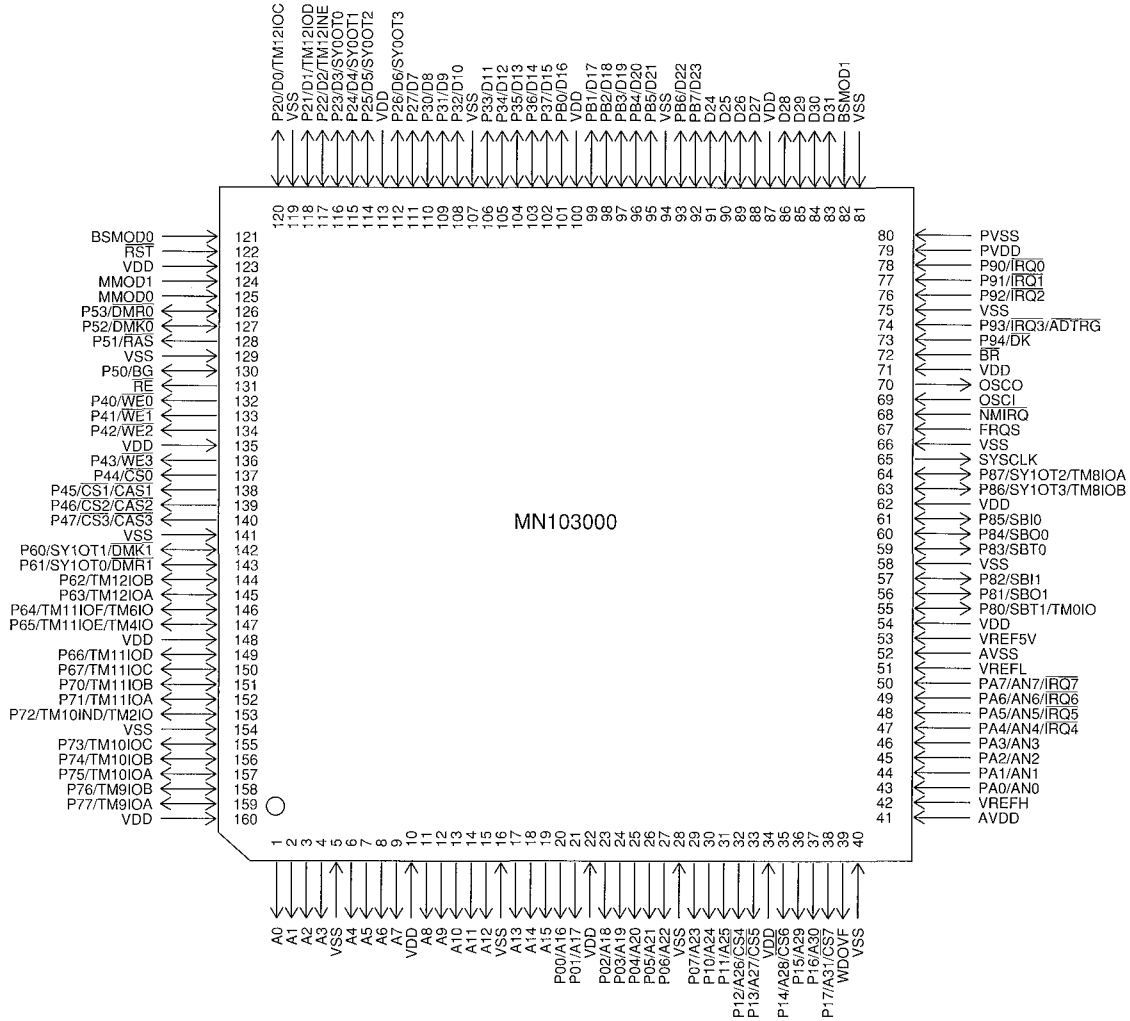
(Ta = –20 °C to +70 °C, AVDD = 3.3 V, AVSS = 0.0 V)

Support Tool

In-Circuit Emulator

PX-ICE103000

Pin Assignment



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