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MN5572

Gray Scale Font Engine

■ Overview

The MN5572 generates shaded gray-scale data from outline (path) data for figures and characters at high speeds. This IC includes built-in input and output FIFO buffers for high-speed processing, and provides three interface circuits, a 32-bit local bus, a 16-bit local bus, and a PCI bus, so that it can be used in a wide range of application products.

Note) PCI bus is a registered trademark of the (US) Peripheral Component Interconnect Association.

■ Features

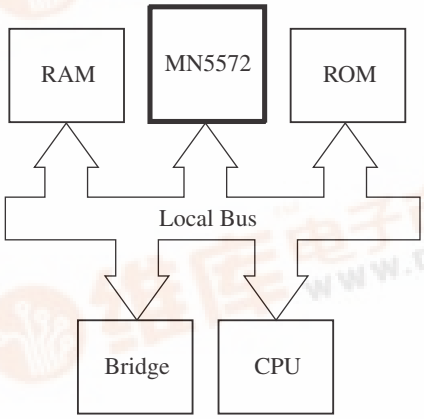
- Gray levels: The number of gray levels can be set to any value between 2 and 128.
- Bit size: The bit size can be set arbitrarily.
- Generation processing speed: More than 20 000 frames/second (A single frame is 32 dots by 32 dots, when the Heisei Gothic (Japanese) font is used as the sample data.)
- Interface specifications: Local bus (16 bits or 32 bits, 33 MHz), PCI bus (32 bits, 33 MHz)
- Operating frequency: 66 MHz (maximum)
- Operating supply voltage: 3.3 V ± 0.3 V (5 V inputs are also supported.)

■ Applications

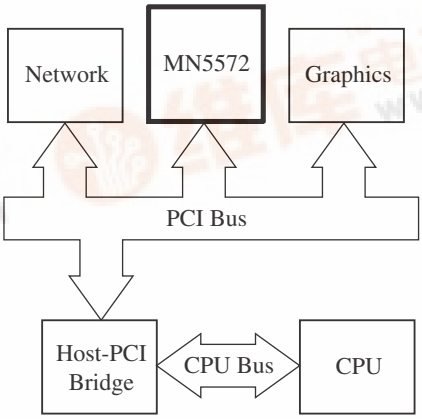
- High-quality character generation in STB, DTV, in-car navigation systems and other products.

■ Block Diagrams

• Local Mode



• PCI Mode



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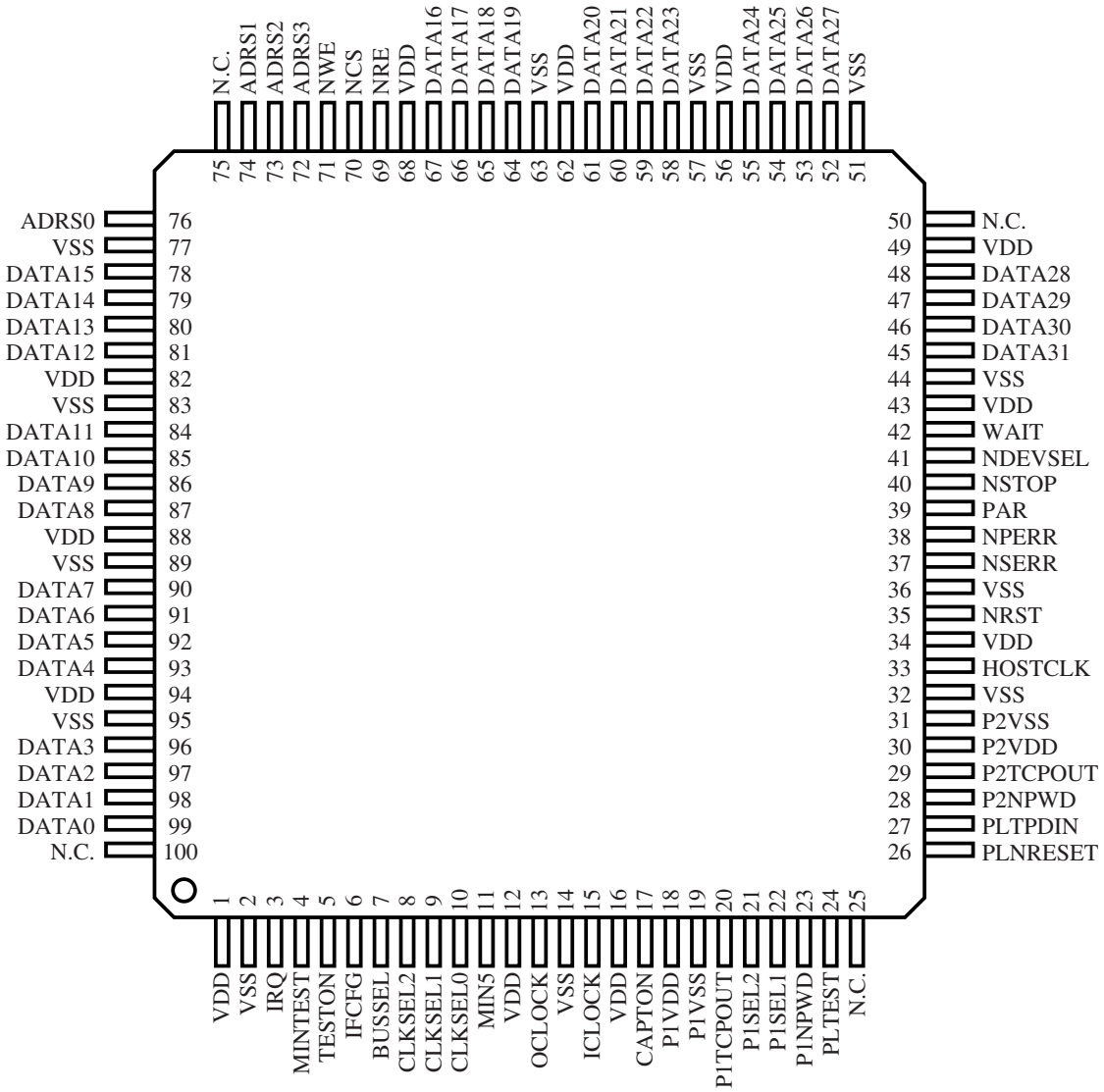
■ Pin Assignments

1. Pin Assignment in Local 32/16 Mode

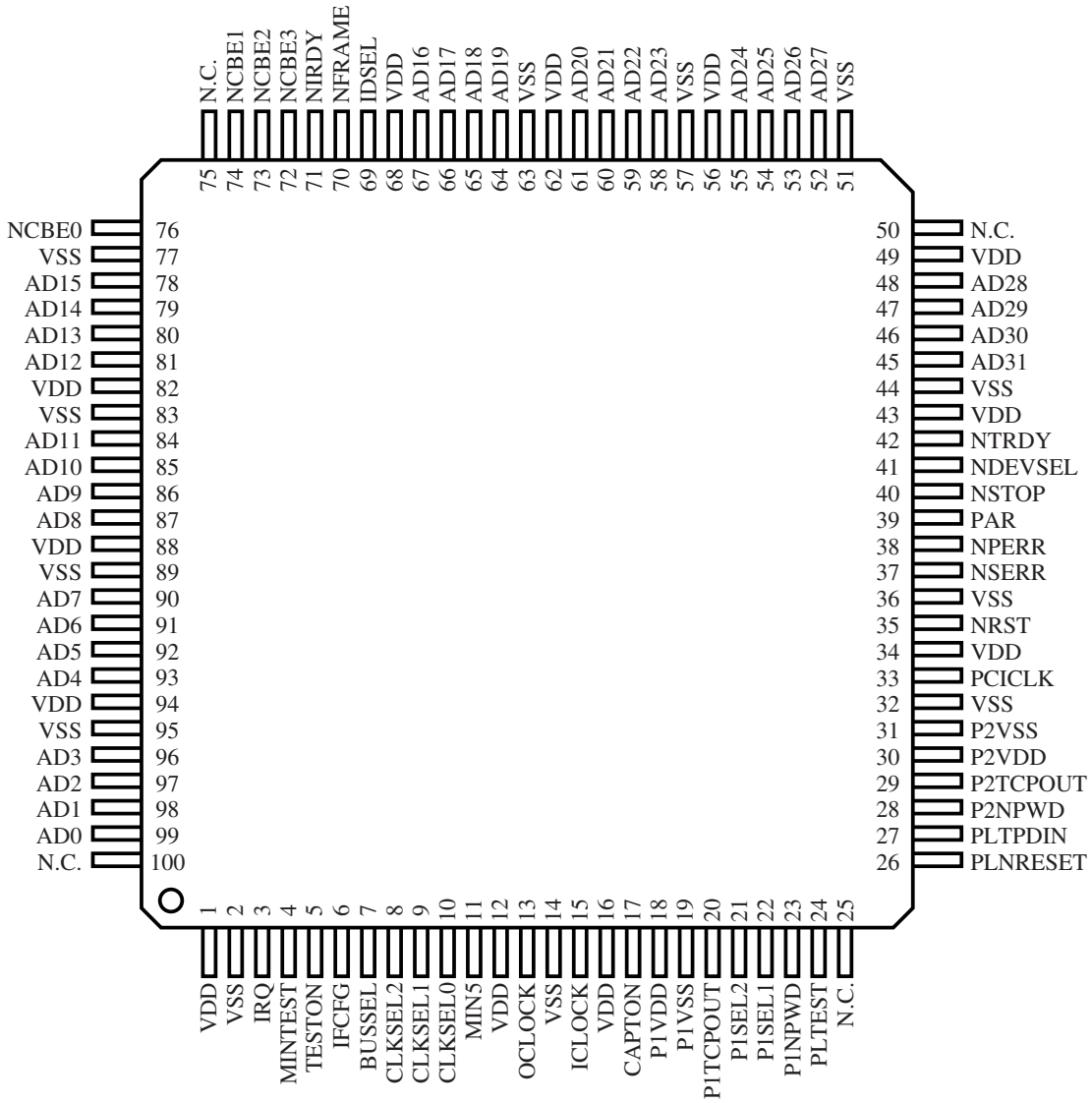


(TOP VIEW)

Note) N.C.: No connection.

■ Pin Assignments (continued)

2. Pin Assignment in PCI Mode



(TOP VIEW)

Note) N.C.: No connection.

■ Pin Descriptions

1. Local 32 mode pin descriptions

Pin Name	I/O	Description
ICLOCK	I	Internal operating clock input
HOSTCLK	I	External interface clock input
NRST	I	Hardware reset (active low)
ADRS[3 : 0]	I	Address input from host
NCS	I	Chip select from host (active low)
NWE	I	Write enable from host (active low)
NRE	I	Read enable from host (active low)
DATA[31 : 16]	I/O	Data I/O to/from host (upper 16 bits)
DATA[15 : 0]	I/O	Data I/O to/from host (lower 16 bits)
WAIT	O	Wait output to host
IRQ	O	Interrupt request output to host
IFCFG	I	Interface mode setting (connect low)
BUSSEL	I	Data bus width setting (connect high)
CLKSEL[2 : 0]	I	Internal/external clock setting
PLNRESET	I	Internal PLL reset (active low)
P1NPWD	I	Low power mode control for internal frequency multiplier PLL (active low)
P1SEL[2 : 1]	I	Frequency selector for internal frequency multiplier PLL
P2NPWD	I	Low power mode control for external phase compensation PLL (active low)
OCLOCK	O	Unused
NSERR	I	Unused
NPERR	I	Unused
PAR	I	Unused
NSTOP	I	Unused
NDEVSEL	I	Unused
MINTEST	I	Testing (Connect low during normal operation.)
TESTON	I	Testing (Connect low during normal operation.)
CAPTON	I	Testing (Connect low during normal operation.)
PLTEST	I	Testing (Connect low during normal operation.)
PLTPDIN	I	Testing (Connect low during normal operation.)
P1TCPOUT	O	Testing
P2TCPOUT	O	Testing
MIN5	I	5 V voltage reference
P1VDD	I	Internal frequency multiplier PLL power supply (3.3 V)
P2VDD	I	External phase compensation PLL power supply (3.3 V)
VDD	I	Power supply (3.3 V)

■ Pin Descriptions (continued)

1. Local 32 mode pin descriptions (continued)

Pin Name	I/O	Description
P1VSS	—	Ground
P2VSS	—	Ground
VSS	—	Ground

2. Local 16 mode pin descriptions

Pin Name	I/O	Description
ICLOCK	I	Internal operating clock input
HOSTCLK	I	External interface clock input
NRST	I	Hardware reset (active low)
ADRS[3 : 0]	I	Address input from host
NCS	I	Chip select from host (active low)
NWE	I	Write enable from host (active low)
NRE	I	Read enable from host (active low)
DATA[31 : 16]	I	Unused
DATA[15 : 0]	I/O	Data I/O to/from host (upper 16 bits)
WAIT	O	Wait output to host
IRQ	O	Interrupt request output to host
IFCFG	I	Interface mode setting (connect low)
BUSSEL	I	Data bus width setting (connect low)
CLKSEL[2 : 0]	I	Internal/external clock setting
PLNRESET	I	Internal PLL reset (active low)
P1NPWD	I	Low power mode control for internal frequency multiplier PLL (active low)
P1SEL[2 : 1]	I	Frequency selector for internal frequency multiplier PLL
P2NPWD	I	Low power mode control for external phase compensation PLL (active low)
OCLOCK	O	Unused
NSERR	I	Unused
NPERR	I	Unused
PAR	I	Unused
NSTOP	I	Unused
NDEVSEL	I	Unused
MINTEST	I	Testing (Connect low during normal operation.)
TESTON	I	Testing (Connect low during normal operation.)
CAPTON	I	Testing (Connect low during normal operation.)
PLTEST	I	Testing (Connect low during normal operation.)
PLTPDIN	I	Testing (Connect low during normal operation.)

■ Pin Descriptions (continued)

2. Local 16 mode pin descriptions (continued)

Pin Name	I/O	Description
P1TCPOUT	O	Testing
P2TCPOUT	O	Testing
MIN5	I	5 V voltage reference
P1VDD	I	Internal frequency multiplier PLL power supply (3.3 V)
P2VDD	I	External phase compensation PLL power supply (3.3 V)
VDD	I	Power supply (3.3 V)
P1VSS	—	Ground
P2VSS	—	Ground
VSS	—	Ground

3. PCI mode pin descriptions

Pin Name	I/O	Description
ICLOCK	I	Internal operating clock input
PCICLK	I	PCI interface clock input
NRST	I	Hardware reset (active low)
NCBE[3 : 0]	I	PCI command/byte enable (active low)
NFRAME	I	PCI cycle frame (active low)
NIRDY	I	PCI initiator ready (active low)
IDSEL	I	PCI initialization device select
AD[31 : 16]	I/O	PCI address/data I/O (upper 16 bits)
AD[15 : 0]	I/O	PCI address/data I/O (lower 16 bits)
NDEVSEL	O	PCI target device select (active low)
NTRDY	O	PCI target ready (active low)
PAR	I/O	PCI parity I/O
NSTOP	O	PCI stop (active low)
NSERR	O	PCI system error
NPERR	O	PCI parity error
IFCFG	I	Interface mode setting (connect high)
BUSSEL	I	Data bus width setting (connect high)
CLKSEL[2 : 0]	I	Internal/external clock select
PLNRESET	I	Internal PLL reset (active low)
P1NPWD	I	Low power mode control for internal frequency multiplier PLL (active low)
P1SEL[2 : 1]	I	Frequency selector for internal frequency multiplier PLL
P2NPWD	I	Low power mode control for external phase compensation PLL (active low)
OCLOCK	O	Unused

■ Pin Descriptions (continued)

3. PCI mode pin descriptions (continued)

Pin Name	I/O	Description
IRQ	O	Unused
MINTEST	I	Testing (Connect low during normal operation.)
TESTON	I	Testing (Connect low during normal operation.)
CAPTON	I	Testing (Connect low during normal operation.)
PLTEST	I	Testing (Connect low during normal operation.)
PLTPDIN	I	Testing (Connect low during normal operation.)
P1TCPOUT	O	Testing
P2TCPOUT	O	Testing
MIN5	I	5 V voltage reference
P1VDD	I	Internal frequency multiplier PLL power supply (3.3 V)
P2VDD	I	External phase compensation PLL power supply (3.3 V)
VDD	I	Power supply (3.3 V)
P1VSS	—	Ground
P2VSS	—	Ground
VSS	—	Ground

■ Functional Descriptions

1. Addressing

The following describes the memory registers used to control this IC.

1.1 Local mode address map

• Memory access

ADRS3	ADRS2	ADRS1	ADRS0	Symbol	Description	R/W
0	0	0	0	POINT	Path (outline) data input port	W
0	0	0	1	RASTER	Gray-scale data output port	R

• IO access

ADRS3	ADRS2	ADRS1	ADRS0	Symbol	Description	R/W
1	0	0	0	COMMAND	Command register	W
1	0	0	1	STATUS	Status register	R
1	0	1	0	MASK	Mask register	R/W
1	0	1	1	FIFO	FIFO status register	R

■ Functional Description (continued)

1. Addressing (continued)

1.2 PCI mode address map

• Memory access

AD11	AD10	AD9	Symbol	Description	R/W
0	0	0	POINT	Path (outline) data input port	W
0	0	1	RASTER	Gray-scale data output port	R

• IO access

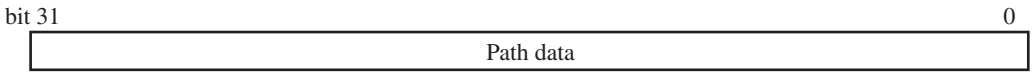
AD4	AD3	AD2	Symbol	Description	R/W
0	0	0	COMMAND	Command register	W
0	0	1	STATUS	Status register	R
0	1	0	MASK	Mask register	R/W
0	1	1	FIFO	FIFO status register	R

2. Memory register functions

2.1 Path (outline) data input port (Point FIFO)

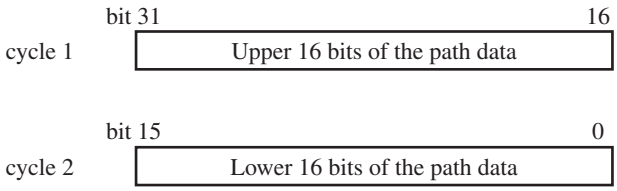
Memory port used for input of the outline font path (outline) data that will be expanded by the MN5572. This port allows 64 double-word values to be written at one time. If more than 64 double-word values must be written, the write operation must be split into multiple operations. The POINT FIFO has a total capacity of 256 double-word values.

• Local 32 and PCI mode



• Local 16 mode

Data is transferred in the order high-order bits first, low-order bits later.

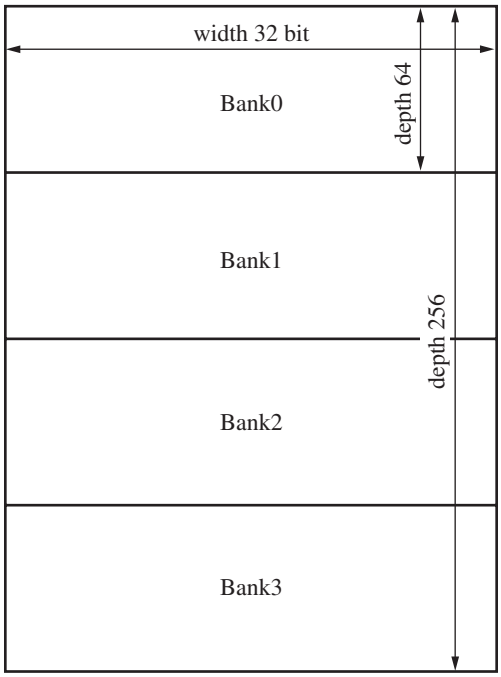


■ Functional Description (continued)

2. Memory register functions (continued)

2.1 Path (outline) data input port (continued)

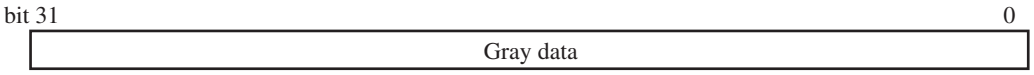
• POINT FIFO memory map



2.2 Gray-scale data output port (RASTER FIFO)

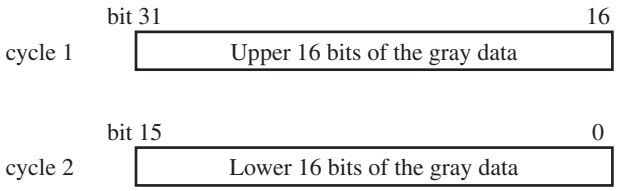
Memory port used for output of the gray-scale data generated by the MN5572. This port allows 64 double-word values to be read at one time. If more than 64 double-word values must be read, the read operation must be split into multiple operations. The RASTER FIFO has a total capacity of 256 double-word values.

• Local 32 and PCI mode



• Local 16 mode

Data is transferred in the order high-order bits first, low-order bits later.

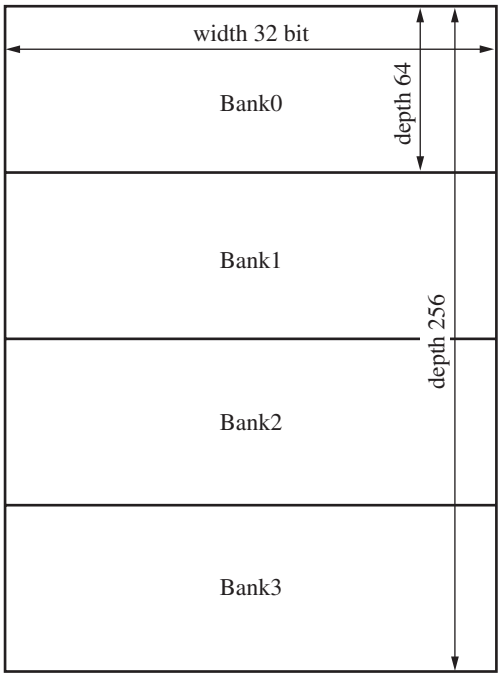


■ Functional Description (continued)

2. Memory register functions (continued)

2.2 Gray-scale data output port (RASTER FIFO) (continued)

• RASTER FIFO memory map



2.3 COMMAND register

Write-only register used to set the IC operating mode.

This is a 16-bit register. Only the low-order 16 bits of the data bus are used.

Hex(DATA[15 : 0])	Command	Function
0x0000	EXEC	Execution mode
0x000F	SRST	Software reset
0x00F0	IRPT	Interrupt
0xAAAA	CKSP	Sleep mode setting
0x5555	CKST	Sleep mode clear

2.4 STATUS register

Read-only register that indicates the IC operating state.

This is a 16-bit register. Only the low-order 16 bits of the data bus are used.

When an interrupt request has occurred, that request can be cleared by reading the status register.

■ Functional Description (continued)

2. Memory register functions (continued)

2.4 STATUS register (continued)

bit 15 14	13 12	11	10 5	4	3	2	1	0
PMS	RMS	REC	RVS	0	MIS	0	CES	CCS

PMS: Indicates the status of the POINT FIFO. After a reset, the status will be FIFO empty.
- 11: FIFO full (Write not allowed)
- 01: FIFO ready (Write allowed)
- 00: FIFO empty (Write wait state)

RMS: Indicates the status of the RASTER FIFO. During a reset, the status will be FIFO empty.
- 11: FIFO full (Read wait state)
- 01: FIFO ready (Read allowed)
- 00: FIFO empty (Read not allowed)

REC: Indicates whether or not the end of a single frame occurs within the 64 double-word values to be read out.
- 1: The readout of a single frame will be completed by reading out the data indicated by RVS.
- 0: The end of a frame does not exist in the data indicated by RVS.

RVS: Indicates the amount of data that can be read out from the RASTER FIFO.
- Up to 64 double-word values (0x00 to 0x3F)

MIS: Indicates the IC internal initialization state.
- An initialization operation is executed automatically after a reset.
- 1: Initializing (Initialization in progress)
- 0: Initialized (Initialization complete)

CES: Indicates the IC internal execution state.
- 0: Run mode

CCS: Indicates the sleep state.
- 1: Sleep mode

2.5 MASK register

Readable/writable register that sets the interrupt generation conditions for the MN5572.
This is a 16-bit register. Only the low-order 16 bits of the data bus are used.

bit 15							8 7							0
PM	—	—	—	—	—	—	RM	—	—	—	—	—	—	TM

PM: Setting this bit enables the MN5572 to generate interrupt requests (IRQ) according to the PMS state.
- 1: Interrupts generated on FIFO empty.
- 0: Interrupt disabled. (default)

RM: Setting these bits enables the MN5572 to generate interrupt requests (IRQ) according to the RMS state.
- 11: Interrupts generated on FIFO full. (default)
- 01: Interrupts generated on FIFO ready.
- 00: Interrupt disabled.

TM: Setting this bit enables the MN5572 to generate interrupt requests (IRQ) according to the state of the MIS flag.
- 1: An interrupt is generated after initialization completes. (default)
- 0: Interrupt disabled.

■ Functional Description (continued)

2. Memory register functions (continued)

2.6 FIFO register (continued)

Readable register that indicates the state of the MN5572 POINT and RASTER FIFOs.
This is a 16-bit register. Only the low-order 16 bits of the data bus are used.

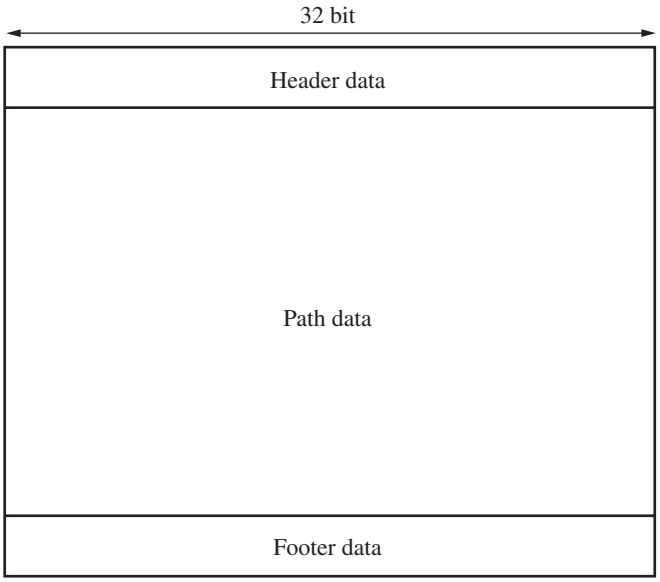
bit 15 – 12	11 – 8	7 – 4	3 – 0
PRBANK	PWBANK	RRBANK	RWBANK

- The 4 bits in PRBANK and PWBANK indicate the status for bank 0 to bank 3 of the POINT FIFO.
  When a given bit in PRBANK is 1, the data in the corresponding bank has not been read out.
  When a given bit in PWBANK is 1, the data for the corresponding bank can be written.
- The 4 bits in RRBANK and RWBANK indicate the status for bank 0 to bank 3 of the RASTER FIFO.
  When a given bit in RRBANK is 1, the data in the corresponding bank can be read out.
  When a given bit in RWBANK is 1, the data in the corresponding bank has not been written.

3. Input data format

This section describes the format of the path (outline) data accepted by the MN5572.

- Overall structure



- Header data structure

bit 31	30 – 28	27	26	25 – 24	23 – 16	15 – 8	7 – 0
0	tag	eof	vth	bpp	max. cov	bbox. x	bbox. y

- Path data structure

bit 31	30 – 28	27 – 14	13 – 0
0	tag	vect. x	vect. y

- Footer data structure

bit 31	30 – 28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	tag	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

■ Functional Description (continued)

3. Input data format (continued)

• Parameters

tag	Data attribute 000 : header 001 : quadratic's or cubic's control point 1 010 : cubic's control point 2 011 : end of data 100 : begin contour 101 : end of line 110 : end of quadratic 111 : end of cubic
eof	Fill rule setting 0 : Fill the inside of the curve when the outline intersects. 1 : Do not fill the inside of the curve when the outline intersects.
vth	Threshold setting used when expanding binary data. 0 : off 1 : on
bpp	Output bit size setting per pixel 00 : 1 bits 01 : 2 bits 10 : 4 bits 11 : 8 bits
max. cov	Setting of gray levels in an expanded frame 0x01h to 0x7Fh (2 levels) (128 levels)
bbox. x	Expanded frame output data width (X) 0x00h to 0x1Fh (1 pixel) (32 pixels)
bbox. y	Expanded frame output data width (Y) 0x00h to 0x1Fh (1 pixel) (32 pixels)
vect. x	Path data coordinate (X)
vect. y	Path data coordinate (Y)

■ Functional Description (continued)

4. Output data format

This section describes the format of the gray-scale data output by the MN5572.

• When bpp = 11 (Here, bbox.x = n and bbox.y = m.)

	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
0	pix[0]		pix[1]		pix[2]		pix[3]		line 0
1	pix[4]		pix[5]		pix[6]		pix[7]		
2	pix[8]		pix[9]		pix[10]		pix[11]		
	.....		.....		.....		.....		
	pix[n-2]		pix[n-1]		pix[n]		—		
	pix[0]		pix[1]		pix[2]		pix[3]		line 1
	pix[4]		pix[5]		pix[6]		pix[7]		
	pix[8]		pix[9]		pix[10]		pix[11]		
	.....		.....		.....		.....		
	pix[n-2]		pix[n-1]		pix[n]		—		
	⋮		⋮		⋮		⋮		⋮
	pix[0]		pix[1]		pix[2]		pix[3]		line m
	pix[4]		pix[5]		pix[6]		pix[7]		
	pix[8]		pix[9]		pix[10]		pix[11]		
	.....		.....		.....		.....		
	pix[n-2]		pix[n-1]		pix[n]		—		

• When bpp = 10 (Here, bbox.x = n and bbox.y = m.)

	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
0	pix[0]	pix[1]	pix[2]	pix[3]	pix[4]	pix[5]	pix[6]	pix[7]	line 0
1	pix[8]	pix[9]	pix[10]	pix[11]	pix[12]	pix[13]	pix[14]	pix[15]	
	.....	.....	.....	.....	.....	.....	.....	.....	
	pix[n-4]	pix[n-3]	pix[n-2]	pix[n-1]	pix[n]	—	—	—	
	pix[0]	pix[1]	pix[2]	pix[3]	pix[4]	pix[5]	pix[6]	pix[7]	line 1
	pix[8]	pix[9]	pix[10]	pix[11]	pix[12]	pix[13]	pix[14]	pix[15]	
	.....	.....	.....	.....	.....	.....	.....	.....	
	pix[n-4]	pix[n-3]	pix[n-2]	pix[n-1]	pix[n]	—	—	—	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	pix[0]	pix[1]	pix[2]	pix[3]	pix[4]	pix[5]	pix[6]	pix[7]	line m
	pix[8]	pix[9]	pix[10]	pix[11]	pix[12]	pix[13]	pix[14]	pix[15]	
	.....	.....	.....	.....	.....	.....	.....	.....	
	pix[n-4]	pix[n-3]	pix[n-2]	pix[n-1]	pix[n]	—	—	—	

■ Functional Description (continued)

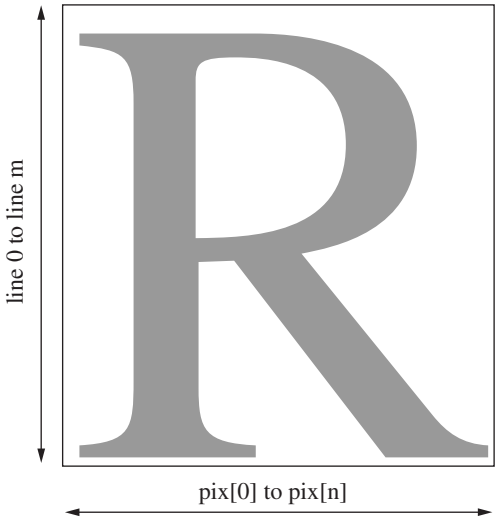
4. Output data format (continued)

• When bpp = 01 (Here, bbox.x = 26 and bbox.y = m.)

	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0	
0	pix[0]	pix[1]	pix[2]	pix[3]	pix[4]	pix[5]	pix[6]	pix[7]	pix[8]	pix[9]	pix[10]	pix[11]	pix[12]	pix[13]	pix[14]	pix[15]	line 0
1	pix[16]	pix[17]	pix[18]	pix[19]	pix[20]	pix[21]	pix[22]	pix[23]	pix[24]	pix[25]	pix[26]	—	—	—	—	—	
2	pix[0]	pix[1]	pix[2]	pix[3]	pix[4]	pix[5]	pix[6]	pix[7]	pix[8]	pix[9]	pix[10]	pix[11]	pix[12]	pix[13]	pix[14]	pix[15]	line 1
3	pix[16]	pix[17]	pix[18]	pix[19]	pix[20]	pix[21]	pix[22]	pix[23]	pix[24]	pix[25]	pix[26]	—	—	—	—	—	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	pix[0]	pix[1]	pix[2]	pix[3]	pix[4]	pix[5]	pix[6]	pix[7]	pix[8]	pix[9]	pix[10]	pix[11]	pix[12]	pix[13]	pix[14]	pix[15]	line m
	pix[16]	pix[17]	pix[18]	pix[19]	pix[20]	pix[21]	pix[22]	pix[23]	pix[24]	pix[25]	pix[26]	—	—	—	—	—	

• When bpp = 00 (Here, bbox.x = 29 and bbox.y = m.)

	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0	
0	← pix[0 : 29] →	—	line 0
1	← pix[0 : 29] →	—	line 1
2	← pix[0 : 29] →	—	line 2
	⋮	⋮	⋮
	← pix[0 : 29] →	—	line m



■ Operation

1. Pin settings

This section describes the pin setting conditions that control the operating state of the MN5572.

1. 1. Clock settings

The interface clock and the internal operating clock are set using the clock setting pins, CLKSEL[2:0].
The application must provide the same external clock signal to the HOSTCLK (PCICLK) and ICLOCK pins.

CLKSEL2	CLKSEL1	CLKSEL0	Interface block clock	Internal operating clock
0	0	0	HOSTCLK (PCICLK) phase compensation applied	Multiplier of ICLOCK
0	0	1	HOSTCLK (PCICLK) phase compensation applied	ICLOCK
0	1	0	HOSTCLK (PCICLK) phase compensation applied	ICLOCK duty compensation applied.
0	1	1	HOSTCLK (PCICLK) phase compensation applied	ICLOCK

1. 2. Phase compensation circuit settings

The interface clock phase compensation circuit is set from external pins. These settings are required when the PCI interface is used.

Pin Name	Setting	Notes
PLNRESET	This pin should be held low (reset) when power is applied, and the held high at other times.	
HOSTCLK(PCICLK)	Input frequency: 13 MHz to 33 MHz	
P2NPWD	Connect high.	When the circuit is not used, this pin may be held low to save power.

1. 3. Frequency multiplier circuit settings

The internal operating clock frequency multiplier circuit can be set by external pins.

• When the clock setting pins CLKSEL[1:0] are 00 (Multiplied clock setting)

Pin Name	Setting	Notes
PLNRESET	This pin should be held low (reset) when power is applied, and the held high at other times.	
ICLOCK	Input frequency	
P1NPWD	Connect high.	When the circuit is not used, this pin may be held low to save power.
P1SEL[2 : 1]	Multiplier setting	

P1SEL2	P1SEL1	Multiplier	ICLOCK frequency	Internal operating frequency
0	0	forbidden	—	—
0	1	2	26 MHz to 33 MHz	52 MHz to 66 MHz
1	0	4	13 MHz to 16.5 MHz	52 MHz to 66 MHz

■ Operation

1. Pin settings (continued)

1. 3. Frequency multiplier circuit settings (contined)

• When the clock setting pins CLKSEL[1:0] are 01 (Duty compensated clock setting)

Pin Name	Setting	Notes
PLNRESET	This pin should be held low (reset) when power is applied, and the held high at other times.	
ICLOCK	Input frequency	
P1NPWD	Must be held high.	When the circuit is not used, this pin may be held low to save power.
P1SEL[2 : 1]	Multiplier setting	

P1SEL2	P1SEL1	Multiplier	ICLOCK frequency	Internal operating frequency
0	0	forbidden	—	—
0	1	2	26 MHz to 33 MHz	26 MHz to 40 MHz
1	0	4	13 MHz to 20 MHz	26 MHz to 40 MHz

2. Operating Procedures

This section presents the operating procedures for using this IC.

2. 1. Operating Procedures Overview

This section presents an overview of the processing used to operate this IC.

• Initialization

Initialization is the processing performed after either the input of either a hardware reset (NRST) or the execution of a software reset. Initialization clears the IC internal memory and sets up the operating conditions.

• Path data write

The path data write operation consists of the input processing for the path data used by the IC to generate multi-level gray-scale data.

• Gray-scale data readout

The gray-scale data readout operation consists of the output processing for the multi-level gray-scale data generated by this IC.

• Interrupt signal wait

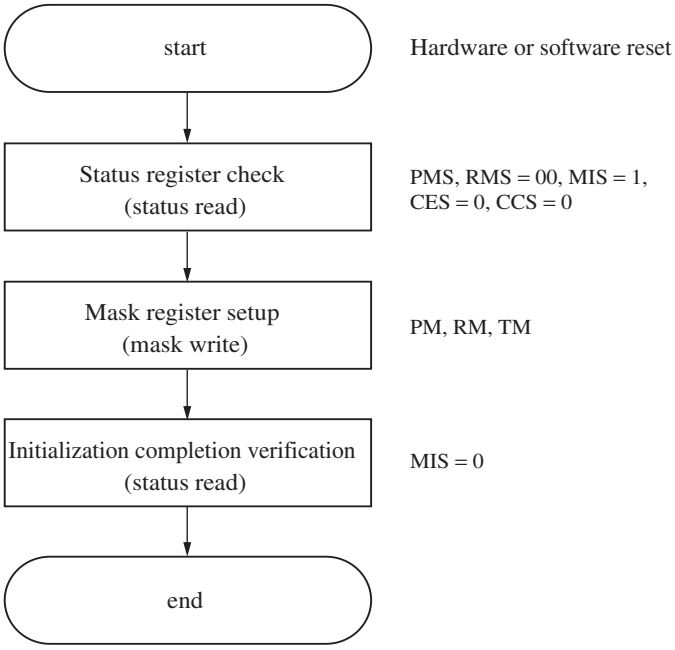
The interrupt signal wait operation is the standby processing performed by the external CPU until this IC issues an external interrupt signal when interrupt controlled processing is used.

■ Operation

2. Operating Procedures (continued)

2. 2. Initialization processing example

• Initialization processing flowchart



• Initialization processing flowchart example description

The IC registers are initialized by a reset due to either a hardware reset (HRST) or a software reset. And then memory initialization processing starts automatically.

- Status register check
  The values of each parameter are verified by reading the status register.
- Mask register setup
  Sets the conditions for the interrupt signal (IRQ) generated by the IC.
  If the mask is not set here, interrupts are processed under the initial conditions.
- Initialization completion verification
  Completion of the memory initialization processing started automatically after the reset is cleared, is verified by monitoring a status register parameter (MIS).

Note) When the mask register TM field is set to 1:

In this case, the IC will notify the application that memory initialization processing has completed by issuing an interrupt signal (IRQ).

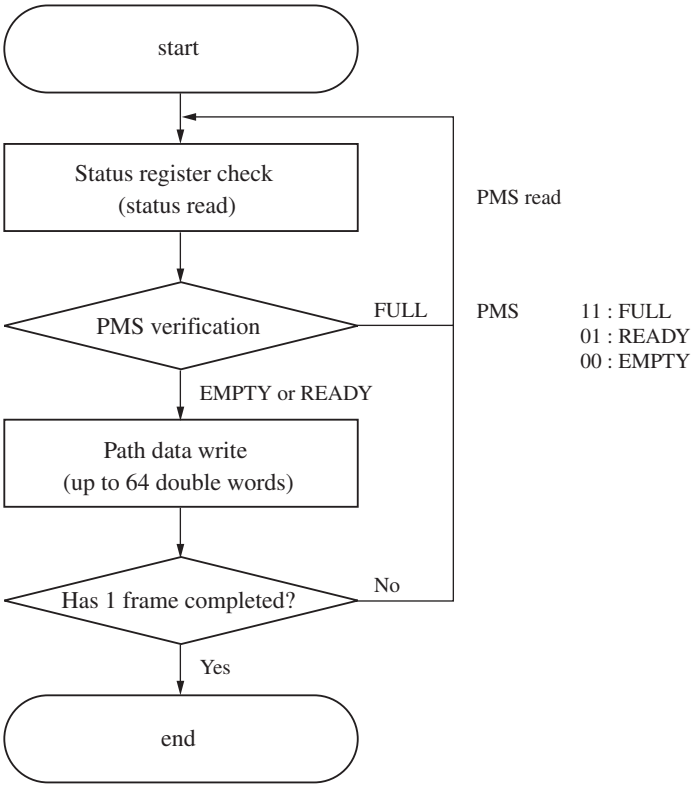
In this case, the interrupt is issued after a wait, and then it should be verified that MIS has become 0 by reading the status register.

■ Operation

2. Operating Procedures (continued)

2. 3. Path data write operation example

• Path data write operation flowchart



• Path data write operation flowchart description

This operation writes the path data to be processed by the IC.

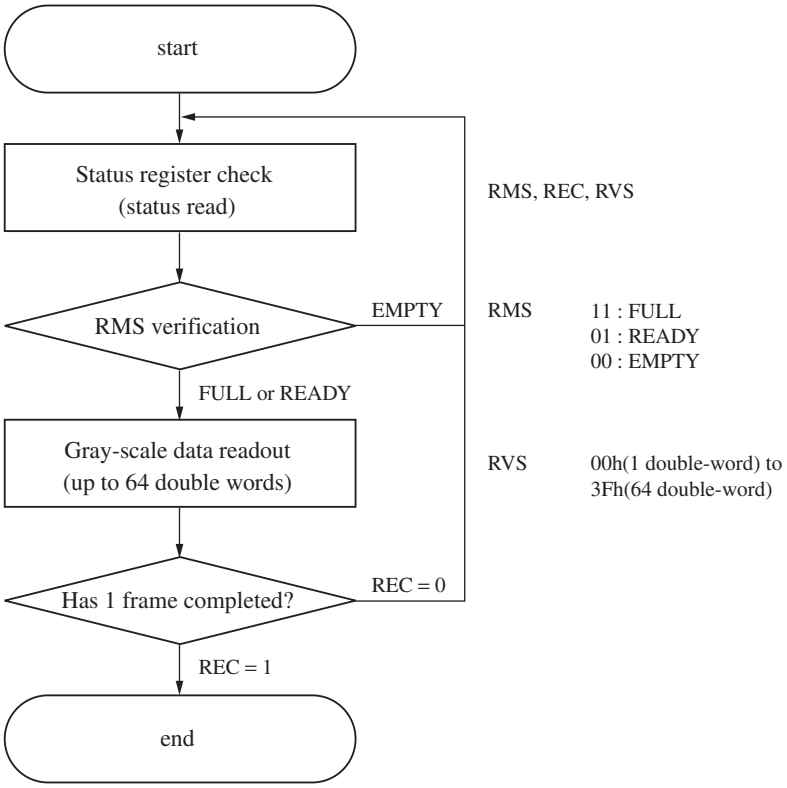
- Status register check
  The status register is read and checked.
- PMS verification
  The operation performed will be determined by the value of the status register PMS field.
  If the PMS field indicates that the FIFO is full, it means that there is no free space in the IC internal memory and the status register must be checked again after a wait.
  If the PMS field indicates empty or ready, a write operation can be started.
- Path data write
  The path data for a single figure or font character is input to the path data input port (POINT FIFO).
  The maximum amount of path data that can be input at one time is 64 double words. If the data exceeds this amount, the data must be divided up into 64 double word units and those units must be processed individually.
  Fewer than 64 double words can be input if that data includes the path data end code (tag = 011).
- Has 1 frame completed?
  If input of the path data for a single figure or font character has completed, the processing terminates. If the path data is being processed in multiple units, or if there is data that must be input, the status register must be checked again and another write operation must be performed.

■ Operation

2. Operating Procedures (continued)

2. 4. Gray-scale data readout processing

• Gray-scale data readout processing flowchart



• Gray-scale data readout processing flowchart description

This operation reads out the gray-scale data created by the IC.

- Status register check
  The status register is read and checked.
- RMS verification
  The operation performed will be determined by the value of the status register RMS field.
  If the RMS field indicates that the FIFO is empty, it means that the IC has not yet completed generation of the gray-scale data and the status register must be checked again after a wait.
  If the RMS field indicates ready, a read operation can be started.
  If the RMS field indicates full, the IC will have to interrupt its gray-scale data generation processing. Therefore, the available data should be read out as quickly as possible.
- Gray-scale data readout
  The multi-valued gray-scale data for a single figure or font character is output from the IC gray-scale data output port (RASTER FIFO).
  The maximum amount of gray-scale data that can be output at a time is 64 double words. The amount of gray-scale data that can actually be output is indicated by RVS. If the amount of gray-scale data to be output exceeds 64 double words, the data will be broken up into 64 double words units and processed internally.
  If the REC field in the status register is 1, the multi-valued gray-scale data for a single figure or font character can be completely read out by reading out the amount of data indicated by RVS.

■ Operation

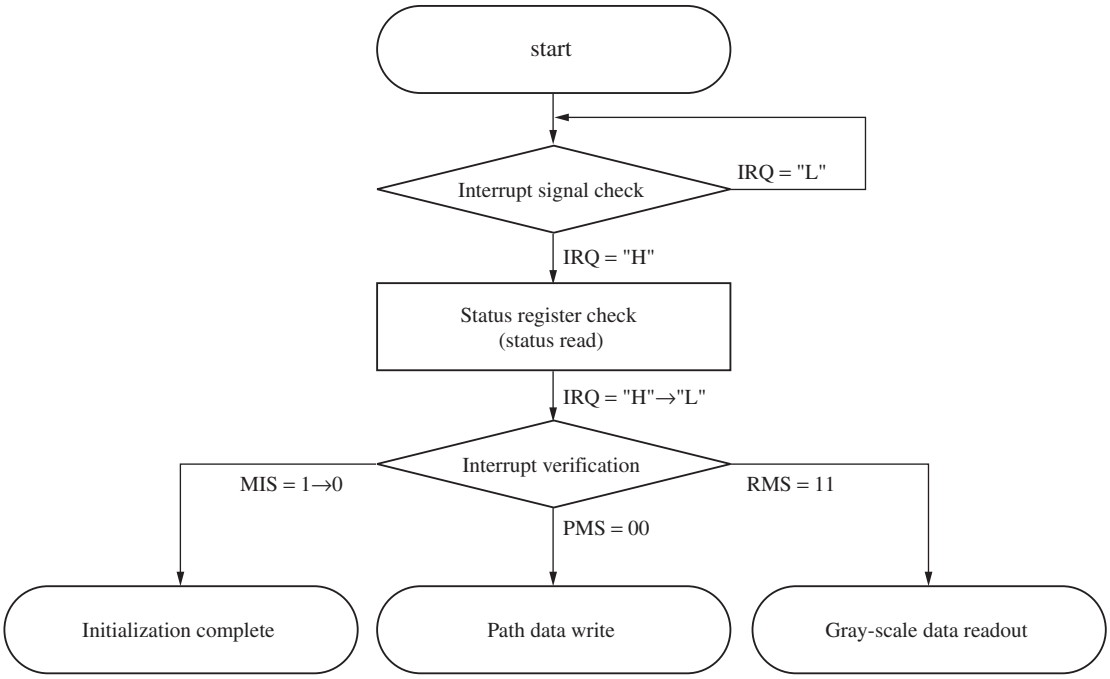
2. Operating Procedures (continued)

2. 4. Gray-scale data readout processing (continued)

- Gray-scale data readout processing flowchart (continued)
  - Has 1 frame completed?
    Processing terminates if the gray-scale data readout operation has completed the output of the gray-scale data for a single figure or font character. The IC divides the gray-scale data into units internally, and if there is still data that must be output (REC = 0), another read operation must be performed again by checking the status register.

2. 5. Interrupt signal wait processing

- Interrupt signal wait processing flowchart



- Interrupt signal wait processing flowchart description
  The IC internal state changes can be verified from the generated interrupt signal.

  - Interrupt signal check
    The interrupt signal (IRQ) is monitored until the interrupt generation conditions set in the IC's mask register are met and the IC asserts (sets to the high level) the interrupt signal.
  - Status register check
    The status register is read and checked.
    After the status register is read, the IC deasserts the interrupt signal (IRQ).
  - Interrupt verification
    The reason the interrupt was generated is verified from the values of the MIS, PMS, and RMS fields in the status register.
    This determines what processing must be performed next.

Note: Interrupt signal wait processing can not be used in PCI mode.
In that case, the IC internal state changes should be determined by periodically reading the status register.

■ Operation

3. Sleep Mode Setup

This section presents the procedure used to set the IC to sleep mode.

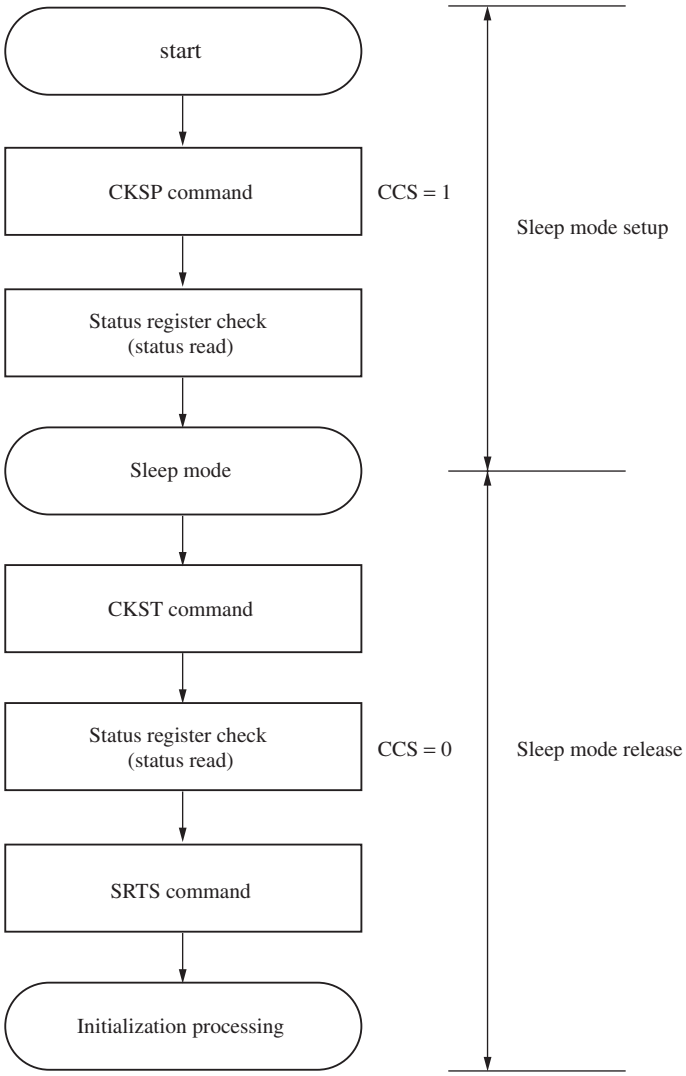
3. 1. Sleep mode overview

This IC operating clock can be stopped and the IC set to sleep mode by issuing a CKSP command to the command register.

If the IC is processing path data internally, a CKSP command should only be issued after that processing has completed. IC internal data is not guaranteed after a CKSP command is issued.

Sleep mode is released by issuing a CKST command to the command register. After clearing sleep mode, normal mode operation can be restored by initializing the IC internally with the SRST command.

• Sleep mode setup and release flow chart

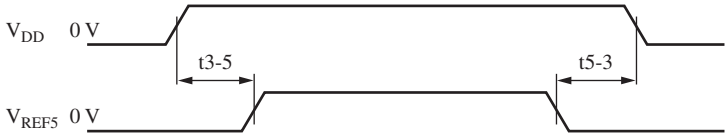


■ Electrical Characteristics

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	– 0.3 to +4.6	V
5 V reference voltage †1	V_{REF5}	– 0.3 to +5.7	V
Input pin voltage (other than TYPE ∗ pins)	V_I	– 0.3 to V_{DD}+0.3	V
Input pin voltage (TYPE-A)	V_{I5}	– 0.3 to +6.0 †2	V
Input pin voltage (TYPE-B)	V_{I5}	– 0.3 to V_{REF5}+0.3 †2	V
Output pin voltage (other than TYPE ∗ pins)	V_O	– 0.3 to V_{DD}+0.3	V
Output pin voltage (TYPE-D)	V_{O5}	– 0.3 to V_{REF5}+0.3 †2	V
Output current (TYPE-HL4 pins)	I_O	±12	mA
Output current (TYPE-HL8 pins)	I_O	±24	mA
Power dissipation	P_D	720	mW
Operating temperature	T_{opr}	–40 to +70	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) 1. †1: The power on and off sequences must meet the following stipulations.



t3-5 and t5-3 must be 0 or longer than 0.

Both V_{DD} and V_{REF5} must transit smoothly.

†2: When $V_{DD} \leq 1.4$ V, the range is – 0.3 V to +4.6 V.

2. TYPE-A pins : P1NPWD, P2NPWD, NCBE0 to NCBE3, NRST, IDSEL, IFCFG, NIRDY, P1SEL1, P1SEL2, BUSSEL, CAPTON, CLKSEL0 to CLKSEL2, ICLOCK, NFRAME, PCICLK, TESTON, PLTPDIN, PLNRESET

   TYPE-B pins : AD0 to AD31, IRQ, PAR, NPERR, NSERR, NSTOP, NTRDY, NDEVSEL

   TYPE-D pins : AD0 to AD31, IRQ, PAR, NPERR, NSERR, NSTOP, NTRDY, NDEVSEL

   TYPE-HL4 pins : IRQ, OCLOCK

   TYPE-HL8 pins : AD0 to AD31, PAR, NPERR, NSERR, NSTOP, NTRDY, NDEVSEL

3. The absolute maximum ratings are limiting values under which the chip will not be destroyed. Operation is not guaranteed within these ranges.

4. All of the VDD and VSS pins must be connected to power supply and ground, respectively.

2. Recommended Operating Conditions at V_{SS} = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		3.0	3.3	3.6	V
5 V reference voltage	V_{REF5}		4.75	5.0	5.25	V
Ambient temperature	T_a		0	—	70	°C
Input rise time	t_r		0	—	100	ns
Input fall time	t_f		0	—	100	

■ Electrical Characteristics (continued)

3. DC Characteristics

at V_{DD} = 3.0 V to 3.6 V, V_{REF5} = 4.75 V to 5.25 V, V_{SS} = 0.00 V, f_{TEST} = 66 MHz, T_a = 0°C to +70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent supply current	I_{DDS}	V_I (pull up)= OPEN V_I (pull down) = OPEN Either the V_{DD} or the V_{SS} level must be applied to all other input pins and I/O pins in the high-impedance state.	—	—	200	µA
5 V reference supply (VREF5) input leakage current	I_{REF}		—	—	±20	µA
Operating supply current	I_{DDO}	$V_I = V_{DD}$ or V_{SS} f = 66 MHz V_{DD} = 3.3 V, outputs open	—	90	180	mA
CMOS level inputs with built-in pull-down resistors: MINTEST						
High-level input voltage	V_{IH}		$V_{DD} \times 0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.3$	V
Pull-down resistor	R_{IL}	$V_I = V_{DD}$	10	30	90	kΩ
Input leakage current	I_{LIL}	$V_I = V_{SS}$	—	—	±10	µA
LVTTL level inputs with built-in pull-down resistors: PLTEST						
High-level input voltage	V_{IH}		2.0	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	0.8	V
Pull-down resistor	R_{IL}	$V_I = V_{DD}$	10	30	90	kΩ
Input leakage current	I_{LIL}	$V_I = V_{SS}$	—	—	±10	µA
TTL level inputs: P1NPWD, P2NPWD, NCBE0 to NCBE3, NRST, IDSEL, IFCFG, NIRDY, P1SEL1, P1SEL2, BUSSEL, CAPTON, CLKSEL0 to CLKSEL2, ICLOCK, NFRAME, PCICLK, TESTON, PLTPDIN, PLNRESET						
High-level input voltage	V_{IH}		2.0	—	5.25	V
Low-level input voltage	V_{IL}		0	—	0.8	V
Input leakage current	I_{LI}	V_I = 5.25 V or V_{SS}	—	—	±10	µA
Push-pull outputs : OCLOCK						
High-level output voltage	V_{OH}	I_{OH} = −4.0 mA $V_I = V_{DD}$ or V_{SS}	V_{DD}− 0.6	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 4.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V

■ Electrical Characteristics (continued)

3. DC Characteristics (continued)

at V_{DD} = 3.0 V to 3.6 V, V_{REF5} = 4.75 V to 5.25 V, V_{SS} = 0.00 V, f_{TEST} = 66 MHz, T_a = 0°C to +70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TTL level I/O pins: IRQ						
High-level input voltage	V_{IH}		2.0	—	V_{REF5}	V
Low-level input voltage	V_{IL}		0	—	0.8	V
High-level output voltage	V_{OH}	I_{OH} = −4.0 mA $V_I = V_{DD}$ or V_{SS}	2.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 4.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage current	I_{LO}	V_O = high-impedance state V_I = 5.25 V or V_{SS} V_O = 5.25 V or V_{SS}	—	—	±10	µA
TTL level I/O pins: AD0 to AD31, PAR, NPERR, NSERR, NSTOP, NTRDY, NDEVSEL						
High-level input voltage	V_{IH}		2.0	—	V_{REF5}	V
Low-level input voltage	V_{IL}		0	—	0.8	V
High-level output voltage	V_{OH}	I_{OH} = −8.0 mA $V_I = V_{DD}$ or V_{SS}	2.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 8.0 mA $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage current	I_{LO}	V_O = high-impedance state V_I = 5.25 V or V_{SS} V_O = 5.25 V or V_{SS}	—	—	±10	µA

4. PLL Characteristics

V_{SS} = 0.0 V, V_{DD} = 3.3 V, Ta = 25 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock generator (PLL): ICLOCK						
PLL oscillation frequency	f_{ICLOCK}	Multiplier: 2 f_{ICLOCK} = 26 MHz to 40 MHz Multiplier: 4 f_{ICLOCK} = 13 MHz to 20 MHz Multiplier: 6 f_{ICLOCK} = 9 MHz to 13 MHz	50	—	80	MHz

V_{SS} = 0.0 V, V_{DD} = 3.3 V, Ta = 25 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock generator (PLL): PCICLK						
PLL oscillation frequency	f_{PCICLK}	f_{PCICLK} = 13 MHz to 33 MHz	26	—	66	MHz

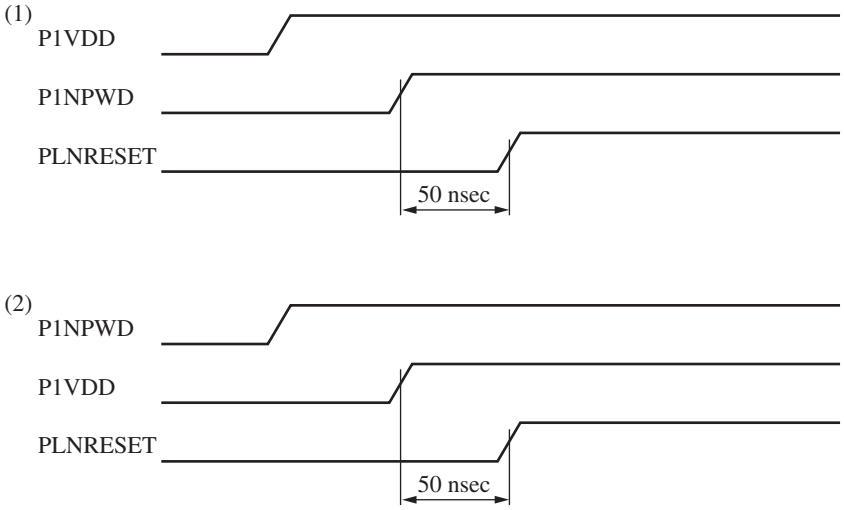
■ Electrical Characteristics (continued)

4. PLL Characteristics (continued)

<PLL Reset Timing: ICLOCK>

You should insert a delay of at least 50 ns after the rise of either P1VDD or P1NPWD, whichever occurs later, and then bring PLNRESET up to the high level.

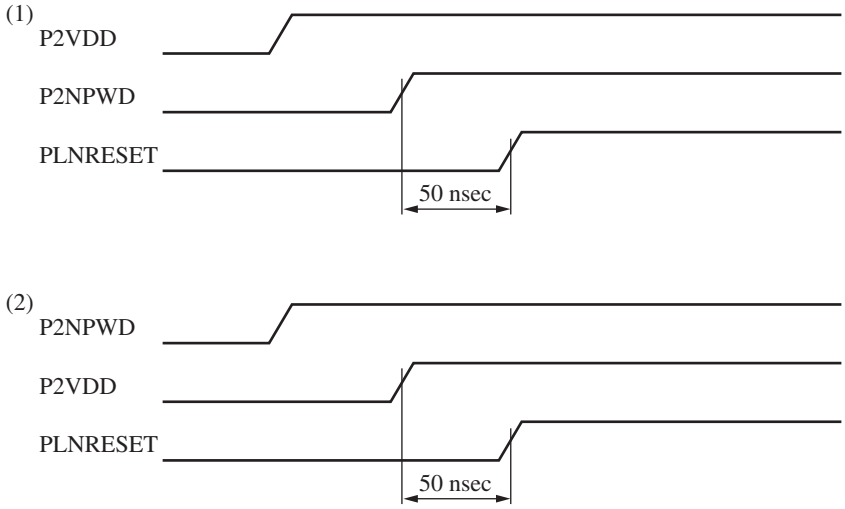
Also, if P1VDD is high, you should raise PLNRESET when P1NPWD is set low.



<PLL Reset Timing: PCICLK>

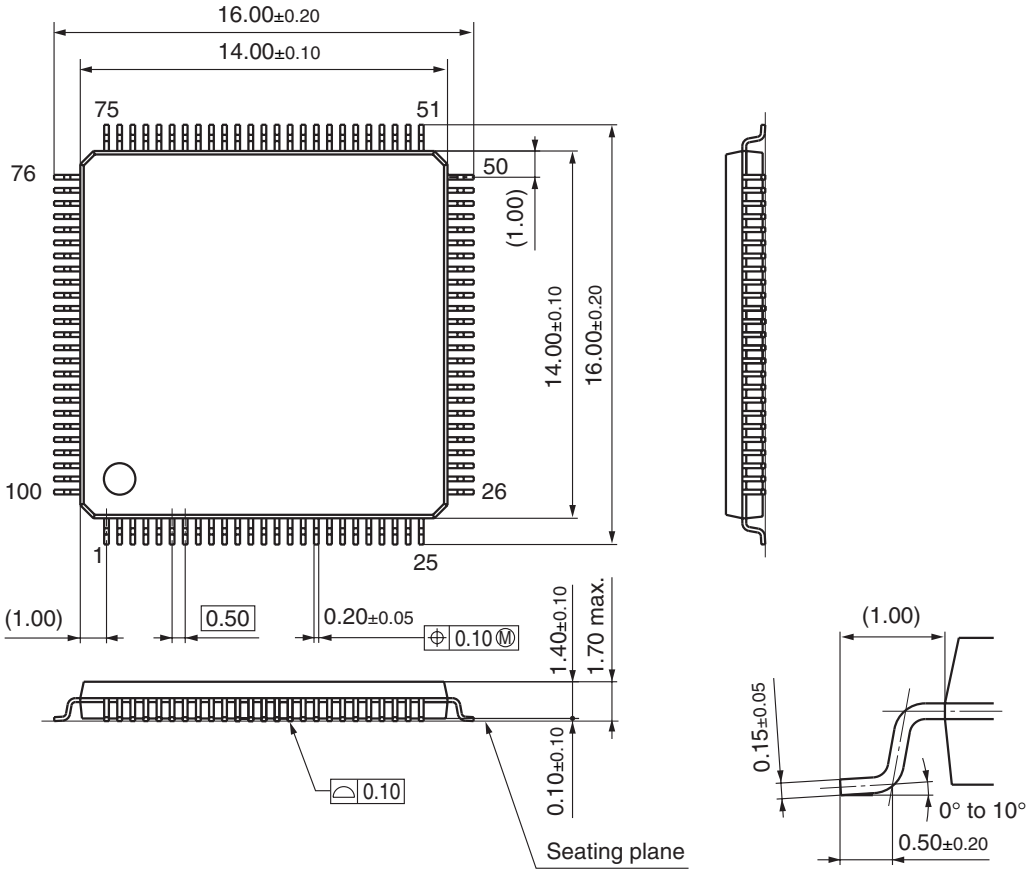
You should insert a delay of at least 50 ns after the rise of either P2VDD or P2NPWD, whichever occurs later, and then bring PLNRESET up to the high level.

Also, if P2VDD is high, you should raise PLNRESET when P2NPWD is set low.



■ Package Dimensions (Unit: mm)

• LQFP100-P-1414 (Lead-free package)



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