

For Communications Equipment

Panasonic

MN6155

PLL LSI with Built-In Prescaler

■ Overview

The MN6155 is a CMOS LSI for a phase-locked loop (PLL) frequency synthesizer with serial data parameter input.

It consists of a two-coefficient prescaler, variable frequency divider, phase comparator, and charge pump.

It offers high-speed operation on a low power supply voltage (1.0 to 1.4 V) and low power consumption (1.65 mW for $V_{DD}=1.1$ V, $F_{IN}=R_{IN}=90$ MHz).

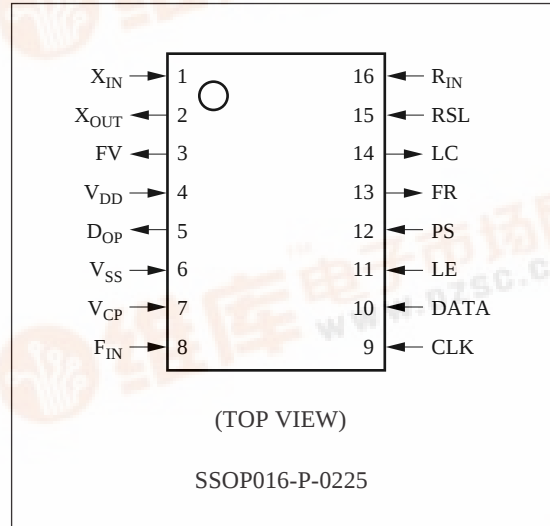
Other features include intermittent operation by the power save (PS) control signal and high-speed pull-in that rapidly corrects the phase differences occurring at the start of operation.

It also offers two choices for the reference signal: self-excited operation using the built-in inverter amplifier or use of an external, separately excited oscillator.

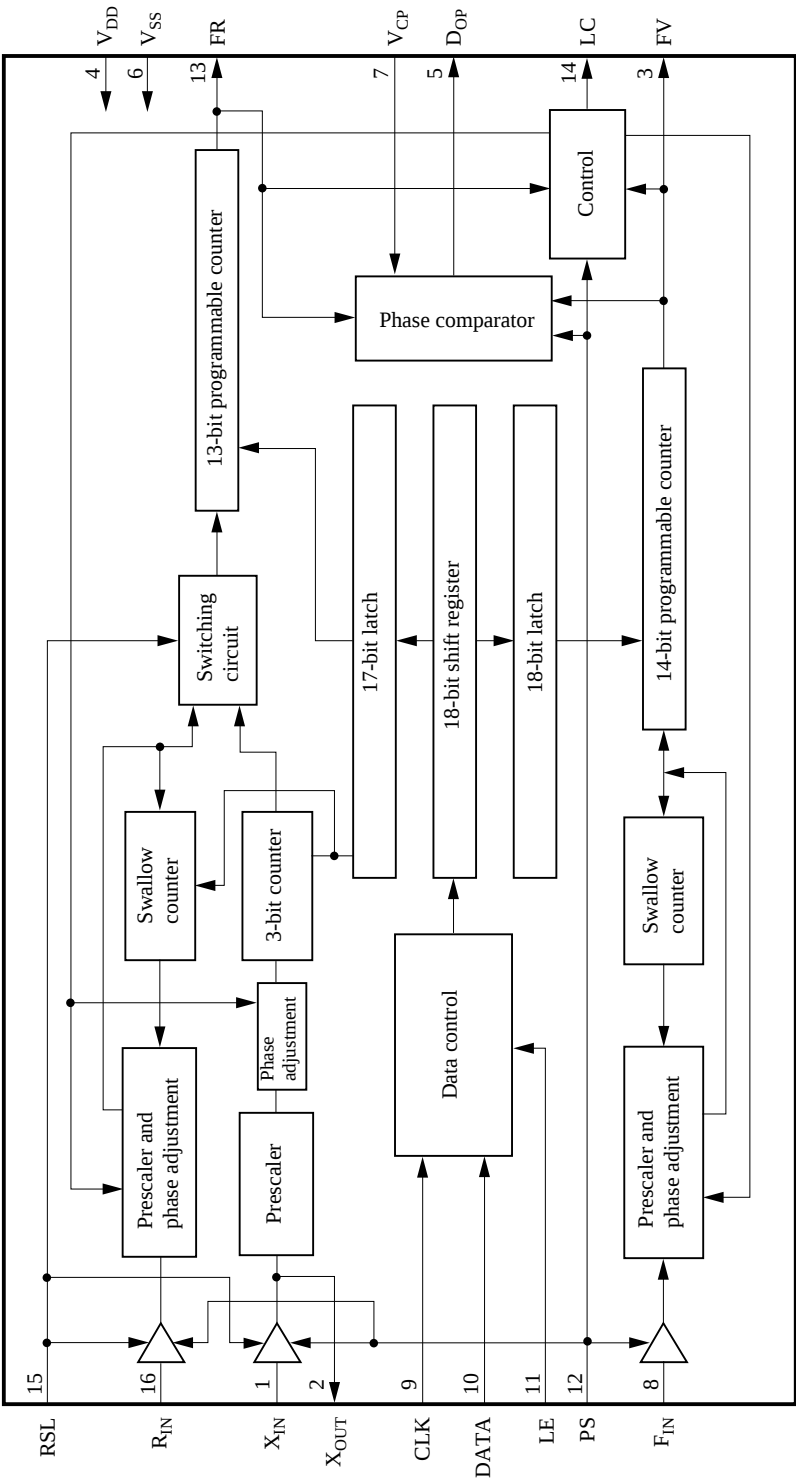
■ Features

- Low power supply voltage: $V_{DD}=1.0$ to 1.4 V
- Low power consumption: 1.65mW ($V_{DD}=1.10\text{V}$, $F_{IN}=90\text{MHz}$, $R_{IN}=90\text{MHz}$)
- High-speed operation: $F_{IN}=90\text{MHz}$, $R_{IN}=90\text{MHz}$ ($V_{DD}=1.1\text{V}$)
- Frequency dividing ratios in reference frequency dividing stage
 - 6 to 131,070 for RSL at "H" level (even number setting is available)
 - 272 to 131,071 for RSL at "L" level
- Frequency dividing ratios for comparator stage: 272 to 262,143
- Power supply pin for built-in charge pump
 - $V_{CP}=2.5$ to 3.2V
- Output monitor pins for both comparator and reference frequency dividing stages

■ Pin Assignment



■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	X_{IN}	Crystal oscillator connection pins: X_{IN} = Oscillator circuit input pin; (X_{IN} is attached to a pull-up resistor when the PS or RSL pin is at "L" level.) X_{OUT} = Oscillator circuit output pin.
2	X_{OUT}	
3	FV	Frequency divider output signal in comparator stage. Phase comparator input monitor.
4	V_{DD}	Power supply
5	D_{OP}	Low-pass filter connection pin. Use a passive filter.
6	V_{SS}	Ground
7	V_{CP}	Power supply pin for built-in charge pump
8	F_{IN}	Frequency divider input pin in comparator stage.
9	CLK	Shift register clock input pin. The chip latches data at the rising edge of the CLK signal.
10	DATA	Shift register data input pin. The final two bits in the data select the write latch: "11" for R-latch; "01" for N-latch.
11	LE	Load enable signal input pin. This is the latch-write-enable signal. It is at "H" level for write.
12	PS	Power save control signal input pin. "H" level input starts the frequency divider and places the chip in operational mode. "L" level input places the chip in standby mode, which saves power. The chip switches the internal charge pump output to the H-z state and the loop is opened.
13	FR	Reference frequency divider output signal. Phase comparator input monitor.
14	LC	Charge pump control signal output pin. When frequency divider operation is stopped, this pin is at "L" level, the internal charge pump output is in the high-impedance state, and the loop is opened.
15	RSL	Reference signal selection pin. "H" level selects self-excited oscillator (X_{IN} and X_{OUT}). "L" level selects external oscillator (R_{IN}).
16	R_{IN}	External reference oscillation input pin. This pin is attached to a pull-up resistor when the PS pin is at "L" level or the RSL pin is at "H" level.

■ MN6155 Frequency Dividing Data Settings

1) Comparator side frequency dividing data

$$FV = F_{IN} \div \{(16 \times N) + A\}$$

2) Reference side frequency dividing data

a) Low-speed operation (RSL pin at "H" level, using X_{IN})

$$FR = X_{IN} \div R$$

b) High-speed operation (RSL pin at "L" level, using R_{IN})

$$FR = R_{IN} \div \{(16 \times NR) + AR\}$$

where

F_{IN} : Comparator side frequency

R_{IN} : High-speed reference frequency

X_{IN} : Low-speed reference oscillator frequency

FV : Comparator frequency divider stage output frequency

FR : Reference frequency divider stage output frequency

N : Setting for 14-bit programmable counter on comparator side

A : Setting for 4-bit swallow counter on comparator side

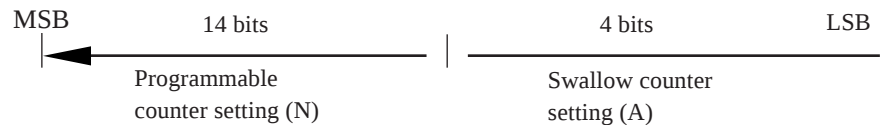
R : Setting for 17-bit programmable counter on low-speed reference side

NR : Setting for 13-bit programmable counter on high-speed reference side

AR : Setting for 4-bit swallow counter on low-speed reference side

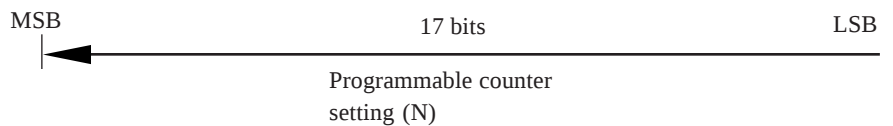
(Note that N should be greater than A ; NR , greater than AR .)

● N-Side Latch Data

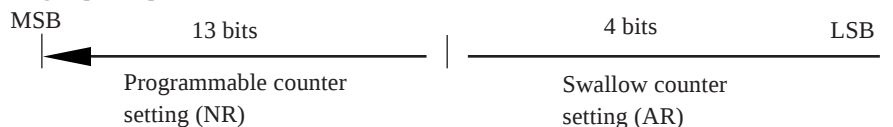


● R-Side Latch Data

Low-speed operation



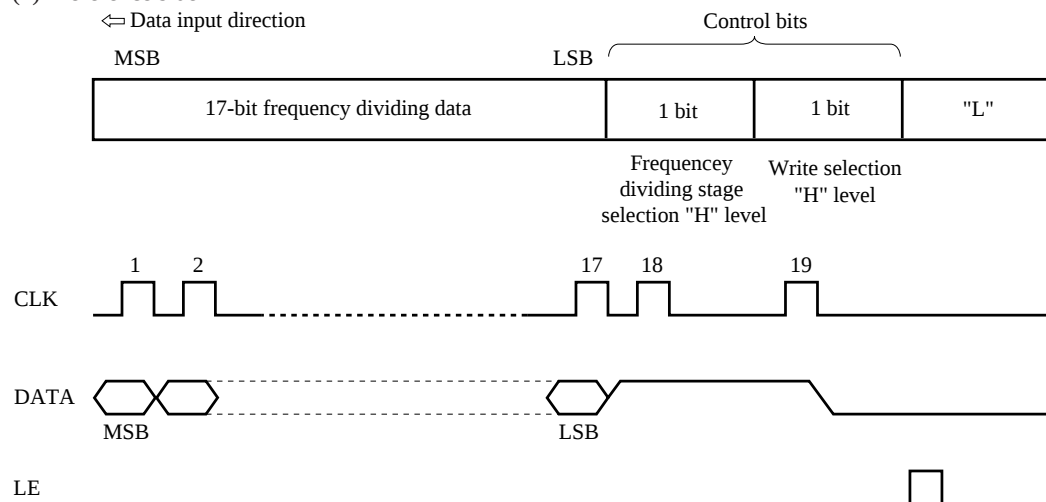
High-speed operation



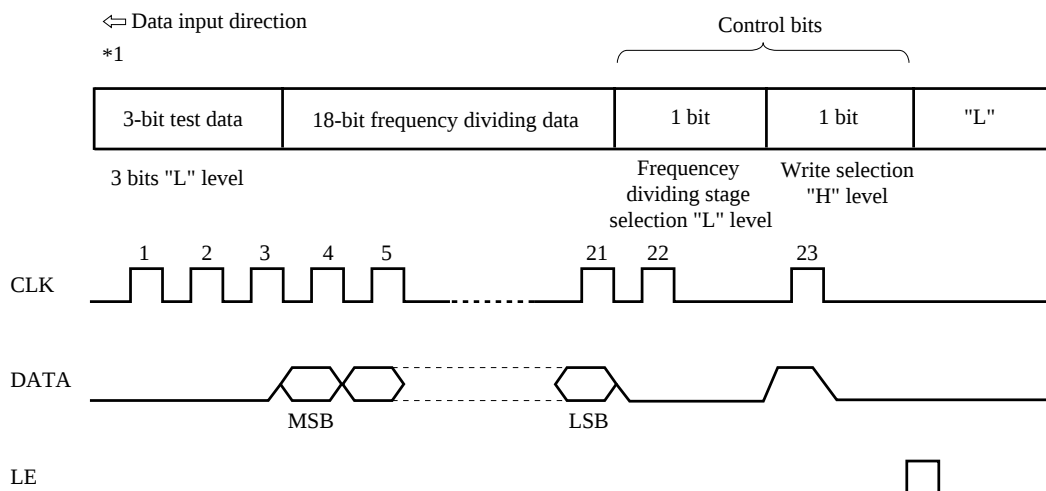
■ Note on Setting Frequency Dividing Data Input

1) Frequency dividing data input

(1) Reference side



(2) Comparating side



Notes

- *1: Preceding the input of the frequency dividing data for the comparating side, input test pattern consisting of three "L" level bits to produce normal operation. Never use any other pattern.
- When the power is first applied, internal operation remains in an unstable state until data is written. To eliminate the risk of excessive current consumption, keep the PS pin at "L" level.
- When the power is first applied, the data settings are indeterminate. Always write data to the chip before starting operation.
- Enter the data to fill the entire latch:
Reference side: 19 bits (17 bits for the frequency divider setting and 2 for control bits)
Comparating side: 23 bits (3 bits for the test pattern, 18 bits for the frequency divider setting, and 2 for control bits)
- Drive the LE pin at "L" level while writing the data.
- "H" level input from the LE pin causes the chip to read the data only when the CLK pin and the DATA pin are both at "L" level.
- Writes are possible when the PS pin is either "H" or "L" level.
- Input the data MSB first.
- The data are inputted at the rising edge of the CLK signal.

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	− 0.3 to +3.0	V
Power supply voltage	V_{CP}	− 0.3 to +4.0	
Input pin voltage	V_I	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	
Output pin voltage	V_O	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	
Power dissipation	P_D	20	mW
Operating ambient temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−55 to +125	

■ Operating Conditions

$V_{SS}=0V$, $T_a=-10$ to $+60^{\circ}C$

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Power supply voltage	V_{DD}		1.0	1.1	1.4	V
Power supply voltage	V_{CP}		2.5	3.0	3.2	V

■ Electric Characteristics

$V_{CP}=2.5V$, $T_a=-10$ to $+60^{\circ}C$

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Power supply pin	V_{DD}	$V_{DD}=1.1V$				
Power supply current	I_{DD}	$F_{IN}=90MHz$, $R_{IN}=90MHz$, PS="H", RSL="L"			2.3	mA
	I_{Dstop}	PS="L" (Power Save operation)			3	μA

Input Pins CLK, DATA, LE, and PS $V_{DD}=1.0$ to $1.4V$

"H" level input voltage	V_{IH}		$V_{DD} - 0.2$		V_{DD}	V
"L" level input voltage	V_{IL}		V_{SS}		0.2	
Input leakage current	I_{LI}				± 1.0	μA

Input Pins F_{IN} , R_{IN} $V_{DD}=1.0$ to $1.4V$

Input voltage	V_{IN}		0.4			V_{p-p}
Input current	I_{IF}	Pull-up resistor is present (PS="L")	−10			μA
Input leakage current	I_{LIF}	$V_{IN}=0$ or V_{DD} (PS="H")			± 20	μA
Maximum operating frequency	F_{INMAX} R_{INMAX}	$V_{IN}=0.4 V_{p-p}$	90			MHz
Minimum operating frequency	F_{INMIN} R_{INMIN}	$V_{IN}=0.4 V_{p-p}$			1.0	MHz

Input Pin X_{IN} $V_{DD}=1.0$ to $1.4V$

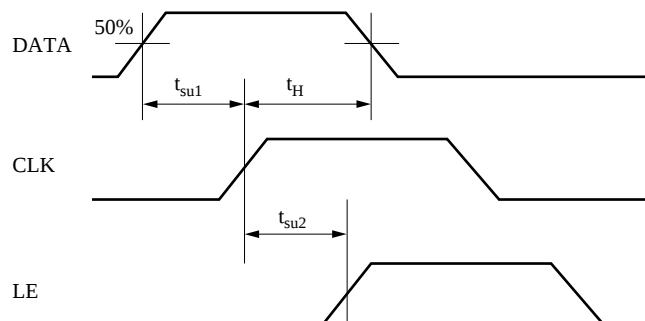
Input voltage	V_{IN}		0.4			V_{p-p}
Input current	I_{IX}	Pull-up resistor is present (PS="L")	− 0.1		−1.5	mA
Input leakage current	I_{LIX}	$V_{IN}=0$ or V_{DD}			5.0	μA
Maximum operating frequency	X_{INMAX}	$V_{IN}=0.4 V_{p-p}$	15			MHz

■ Electrical Characteristics (continued)

$V_{CP}=2.5V$, $T_a=-10$ to $+60^{\circ}C$

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Crystal Oscillator Pins X_{IN} , X_{OUT} V_{DD} =1.0 to 1.4V						
Crystal oscillator frequency	f_{Xtal}		15			MHz
Output Pins FV , FR , LC V_{DD} =1.0 to 1.4V						
"H" level output voltage	V_{OH}	$I_{OH}= -10\mu A$	$V_{DD}- 0.3$		V_{DD}	V
"L" level output voltage	V_{OL}	$I_{OL}=10\mu A$	V_{SS}		0.3	
Output Pin X_{OUT} V_{DD} =1.0 to 1.4V						
"H" level output voltage	V_{XOH}	$I_{XOH}= -100\mu A$	$V_{DD}- 0.3$		V_{DD}	V
"L" level output voltage	V_{XOL}	$I_{XOL}=100\mu A$	V_{SS}		0.3	
Output Pin D_{OP} V_{DD} =1.0 to 1.4V						
"H" level output voltage	I_{DOH}	$V_{Dop}=V_{CP} - 0.3V$	-100			μA
"L" level output voltage	I_{DOL}	$V_{Dop}=0.3V$	-100			
Output leakage current	I_{LOH}	$V_{Dop}=V_{CP}$			2.0	
Output leakage current	I_{LOL}	$V_{Dop}=0.0V$			-2.0	
V_{DD} =1.0 to 1.4V						
Setup time *1	t_{sul}		500			ns
	t_{su2}		500			ns
Hold time *1	t_H		500			ns

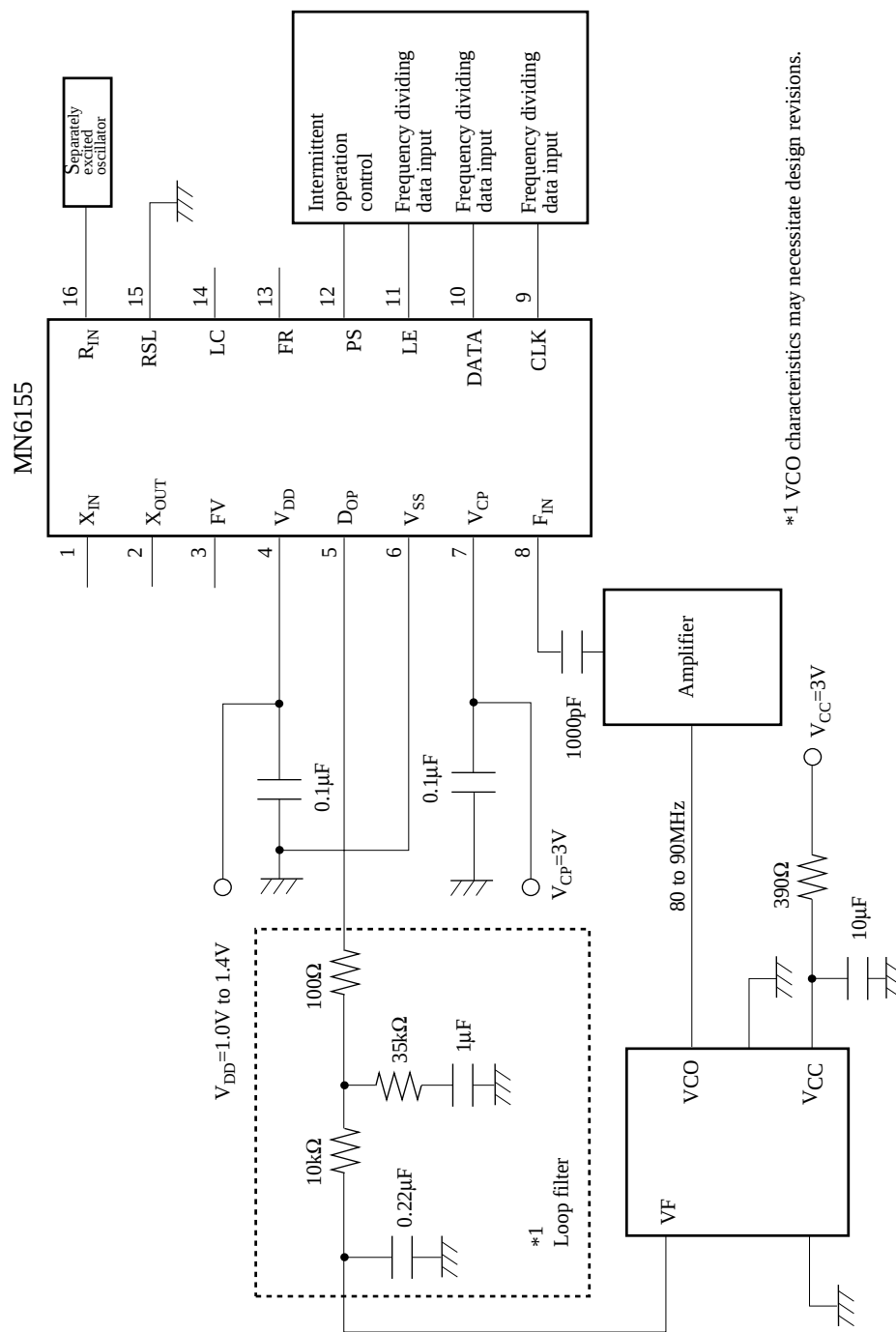
Note*1: The following timing chart shows the setup and hold times.



Usage Note

Be particularly careful with this product as it is more sensitive on the static electricity damage than most of our other products.

■ Application Circuit Example



*1 VCO characteristics may necessitate design revisions.

■ Package Dimensions (Unit: mm)

SSOP016-P-0225

