MN65761T

Low Power 9-Bit CMOS A/D Converter for Image Processing

■ Overview

The MN65761T is a high-speed 9-bit CMOS analog-to-digital converter for image processing applications.

It uses a half flash structure based on chopper comparators and achieves both high speed and low power consumption with multiplexing.

It provides separate power supply pins for the circuits driving the low-voltage digital output pins.

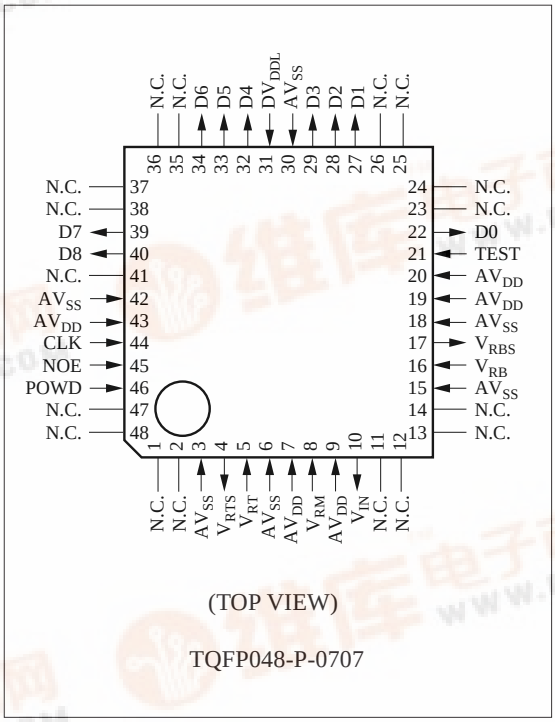
■ Features

- Maximum conversion rate: 18 MSPS (min.)
- Linearity error: ±1.3 LSB (typ.)
- Differential linearity error: ±0.6 LSB (typ.)
- Power supply voltage: 3.6 V or 2.6 V
- Power consumption: 60 mW (typ.) (f_{CLK}=18 MHz)

■ Applications

- Digital television receivers
- Digital video equipment
- Digital image processing equipment

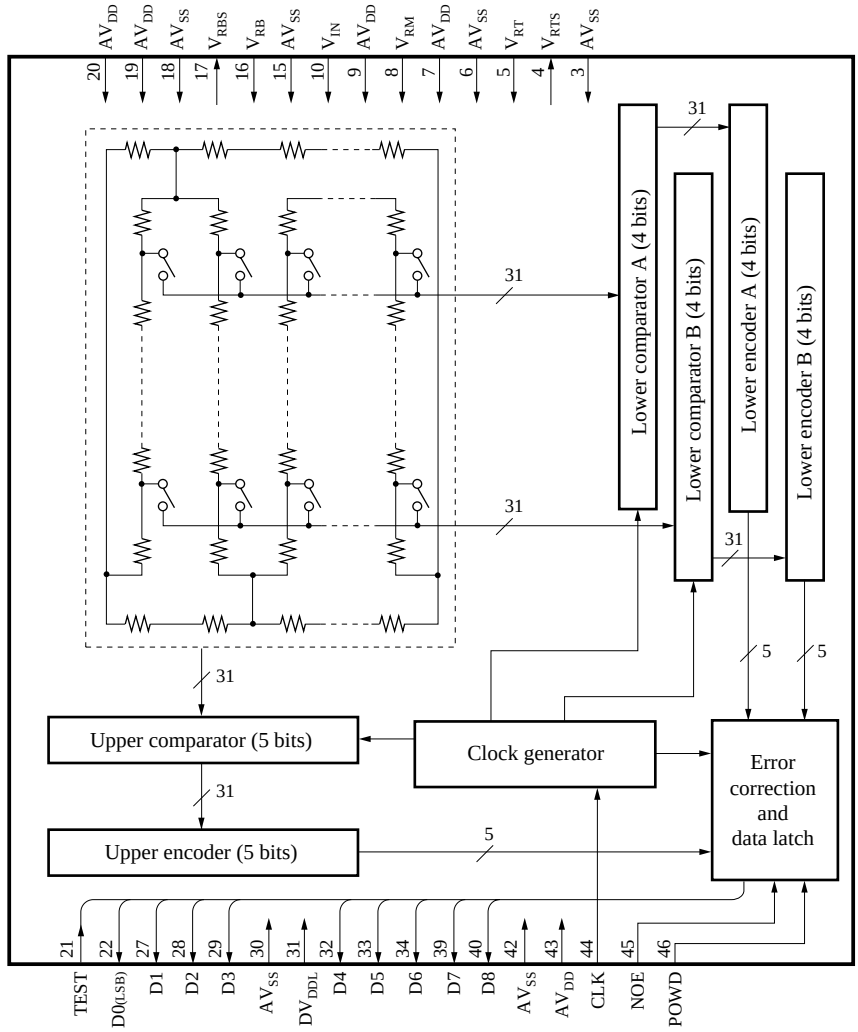
■ Pin Assignment



(TOP VIEW)

TQFP048-P-0707

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	N.C.	No connection
2	N.C.	No connection
3	AV_{SS}	Ground for analog circuits
4	V_{RTS}	Reference voltage power supply (TOP)
5	V_{RT}	Reference voltage input (TOP)
6	AV_{SS}	Ground for analog circuits
7	AV_{DD}	Power supply for analog circuits
8	V_{RM}	Intermediate reference voltage
9	AV_{DD}	Power supply for analog circuits
10	V_{IN}	Analog signal input
11	N.C.	No connection
12	N.C.	No connection
13	N.C.	No connection
14	N.C.	No connection
15	AV_{SS}	Ground for analog circuits
16	V_{RB}	Reference voltage input (BOTTOM)
17	V_{RBS}	Reference voltage power supply (BOTTOM)
18	AV_{SS}	Ground for analog circuits
19	AV_{DD}	Power supply for analog circuits
20	AV_{DD}	Power supply for analog circuits
21	TEST	Test mode selection
22	D0	Digital code output (LSB)
23	N.C.	No connection
24	N.C.	No connection
25	N.C.	No connection
26	N.C.	No connection
27	D1	Digital output
28	D2	Digital output
29	D3	Digital output
30	AV_{SS}	Ground for analog circuits
31	DV_{DDL}	Power supply for low-voltage digital outputs
32	D4	Digital output
33	D5	Digital output
34	D6	Digital output
35	N.C.	No connection
36	N.C.	No connection
37	N.C.	No connection
38	N.C.	No connection
39	D7	Digital output
40	D8	Digital output (MSB)

■ Pin Descriptions (continued)

Pin No.	Symbol	Function Description
41	N.C.	No connection
42	AV_{SS}	Ground for analog circuits
43	AV_{DD}	Power supply for analog circuits
44	CLK	Sampling clock
45	NOE	Digital output enable
46	POWD	Power down mode selection
47	N.C.	No connection
48	N.C.	No connection

■ Absolute Maximum Ratings Ta=25˚C

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +7.0	V
Power supply voltage for digital output circuits	DV_{DDL}	– 0.3 to V_{DD} +0.3	V
Input voltage	V_I	– 0.3 to V_{DD} +0.3	V
Output voltage	V_O	– 0.3 to V_{DD} +0.3	V
Operating ambient temperature	T_{opr}	–20 to +70	˚C
Storage temperature	T_{stg}	–55 to +125	˚C

■ Recommended Operating Conditions $V_{DD}=AV_{DD}=3.6V$, $DV_{DDL}=2.6V$, $V_{SS}=AV_{SS}=0V$, Ta=25˚C

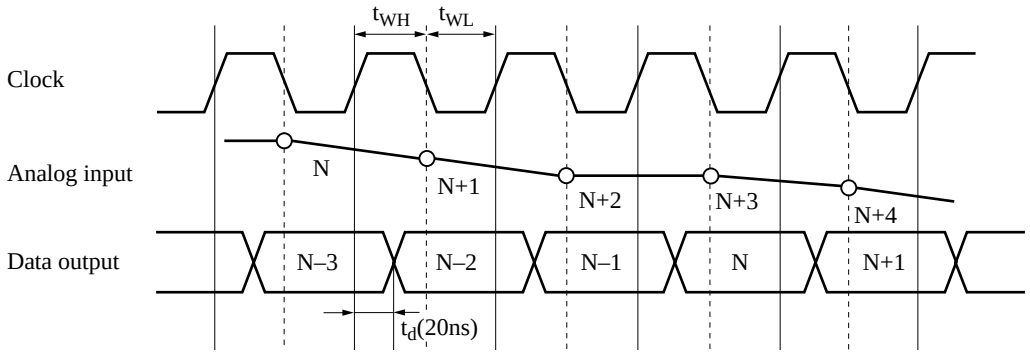
Parameter		Symbol	min	typ	max	Unit
Power supply voltage		V_{DD}	3.15	3.60	3.70	V
Power supply voltage for digital output circuits		DV_{DDL}	2.50	2.60	3.70	V
Digital input voltage	"H" level	V_{IH}	$AV_{DD} \times 0.55$		AV_{DD}	V
	"L" level	V_{IL}	AV_{SS}		$AV_{DD} \times 0.20$	V
Reference voltage	"H" level	V_{RT}		3.30	AV_{DD}	V
	"L" level	V_{RB}	AV_{SS}	1.30		V
Clock	"H" level pulse width	t_{WH}	25			ns
	"L" level pulse width	t_{WL}	25			ns
Analog input voltage		V_{AIN}	AV_{SS}		AV_{DD}	V

■ Electrical Characteristics $V_{DD}=AV_{DD}=3.6V$, $DV_{DDL}=2.6V$, $AV_{SS}=0V$, Ta=25˚C

Parameter		Symbol	Conditions	min	typ	max	Unit
Power consumption		P_C	f_{CLK}=18 MSPS (not including reference current)		60	100	mW
Resolution		RES	$V_{DD}=3.5V$, $DV_{DDL}=2.5V$		9		bit
Linearity error		E_L	f_{CLK}=18MSPS, $V_{DD}=3.5V$		±1.3	±2.5	LSB
Differential linearity error		E_D	$V_{RT}=3.3V$, $DV_{DDL}=2.5V$ $V_{RB}=1.3V$, CLK_{Duty}=50±5%		±0.6	±1.0	LSB
Maximum conversion rate		$F_{C(max.)}$	$V_{DD}=3.5V$, $DV_{DDL}=2.5V$	18			MSPS
Clock frequency		f_{CLK}	$V_{DD}=3.5V$, $DV_{DDL}=2.5V$	1		18	MHz
Analog input dynamic range		D_R	$V_{DD}=3.5V$, $DV_{DDL}=2.5V$	2		$V_{RT}-V_{RB}$	V
Output current	"H" level	I_{OH}	$V_{OH}=DV_{DDL}-0.8V$			–1.5	mA
	"L" level	I_{OL}	$V_{OL}=0.4V$	1.5			mA
Output delay time		t_d	Ta=70˚C, C_L=100Ω+10pF	10	20	35	ns
Analog input capacitance		C_I	V_{IN} pin		26		pF

■ Timing Chart

The chip samples the analog input at the falling edge of the clock signal and provides the corresponding digital output 2.5 clock cycles later at the rising edge of the clock signal.



Note: The circles indicate analog signal sampling points.

■ Package Dimensions (Unit:mm)

TQFP048-P-0707