

MN6576H

Low Power 9-Bit CMOS A/D Converter for Image Processing

Overview

The MN6576H is a high-speed 9-bit CMOS analog-to-digital converter for image processing applications.

It uses a half flash structure based on chopper comparators and achieves both high speed and low power consumption with multiplexing.

It provides separate power supply pins for the circuits driving the low-voltage digital output pins.

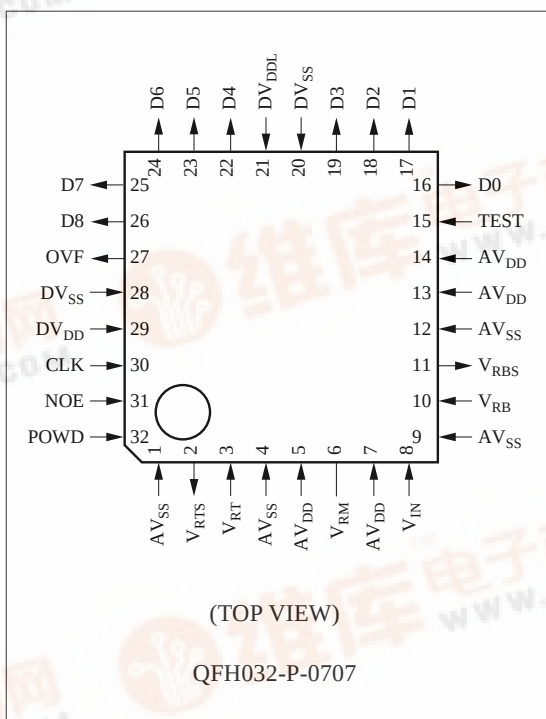
Features

- Maximum conversion rate: 16 MSPS (min.)
- Linearity error: ± 2.5 LSB (typ.)
- Differential linearity error: ± 0.6 LSB (typ.)
- Power supply voltage: 5.0 V or 3.3 V
- Power consumption: 120 mW (typ.) ($f_{CLK}=16$ MHz)

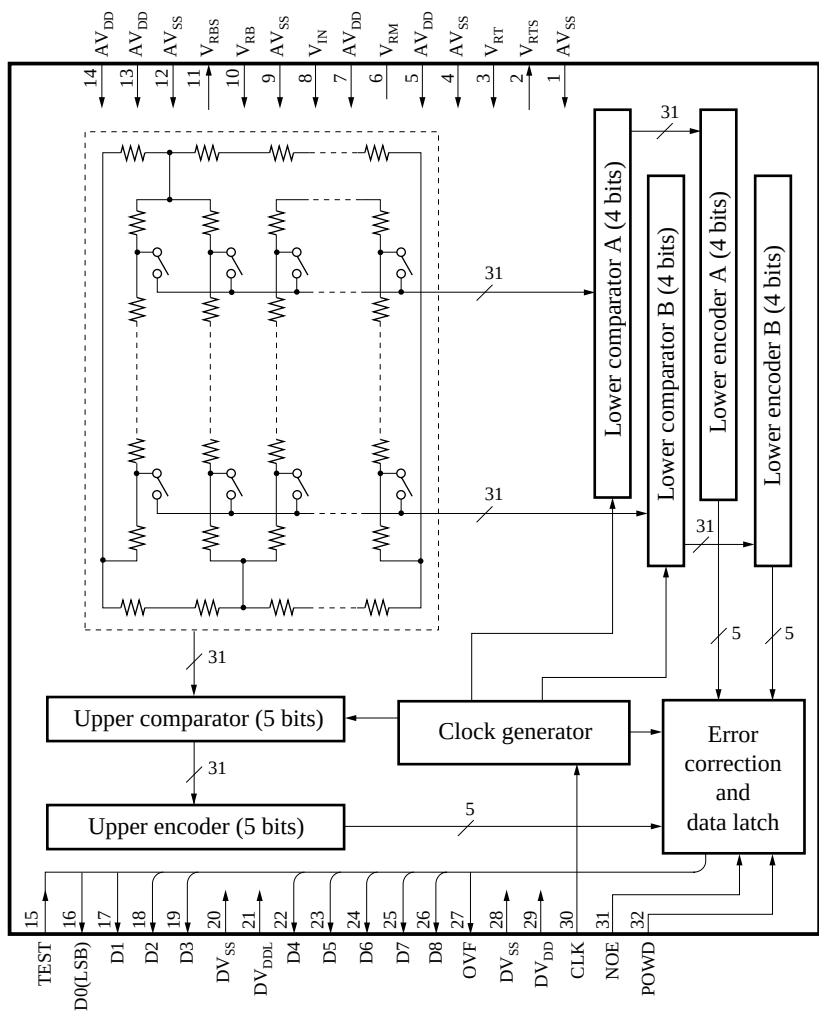
Applications

- Digital television receivers
- Digital video equipment
- Digital image processing equipment

Pin Assignment



■ Block Diagram



Pin Descriptions

Pin No.	Symbol	Function Description
1	AV_{SS}	Ground for analog circuits
2	V_{RTS}	Reference voltage power supply (TOP)
3	V_{RT}	Reference voltage input (TOP)
4	AV_{SS}	Ground for analog circuits
5	AV_{DD}	Power supply for analog circuits
6	V_{RM}	Intermediate reference voltage
7	AV_{DD}	Power supply for analog circuits
8	V_{IN}	Analog signal input
9	AV_{SS}	Ground for analog circuits
10	V_{RB}	Reference voltage power supply (BOTTOM)
11	V_{RBS}	Reference voltage input (BOTTOM)
12	AV_{SS}	Ground for analog circuits
13	AV_{DD}	Power supply for analog circuits
14	AV_{DD}	Power supply for analog circuits
15	TEST	Test mode selection
16	D0	Digital code output (LSB)
17	D1	Digital code output
18	D2	Digital code output
19	D3	Digital code output
20	DV_{SS}	Ground for digital circuits
21	DV_{DDL}	Power supply for low-voltage digital outputs
22	D4	Digital code output
23	D5	Digital code output
24	D6	Digital code output
25	D7	Digital code output
26	D8	Digital code output (MSB)
27	OVF	Overflow output
28	DV_{SS}	Ground for digital circuits
29	DV_{DD}	Power supply for digital circuits
30	CLK	Sampling clock
31	NOE	Output enable
32	POWD	Power down mode selection

■ Absolute Maximum Ratings $T_a=25^{\circ}\text{C}$

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	- 0.3 to +7.0	V
Power supply voltage for digital output circuits	DV_{DDL}	- 0.3 to $V_{DD}+0.3$	V
Input voltage	V_I	- 0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	- 0.3 to $V_{DD}+0.3$	V
Operating ambient temperature	T_{opr}	-20 to +70	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to +125	$^{\circ}\text{C}$

■ Recommended Operating Conditions $V_{DD}=AV_{DD}=DV_{DD}=4.5\text{V}$, $DV_{DDL}=3.0\text{V}$, $V_{SS}=AV_{SS}=DV_{SS}=0\text{V}$, $T_a=25^{\circ}\text{C}$

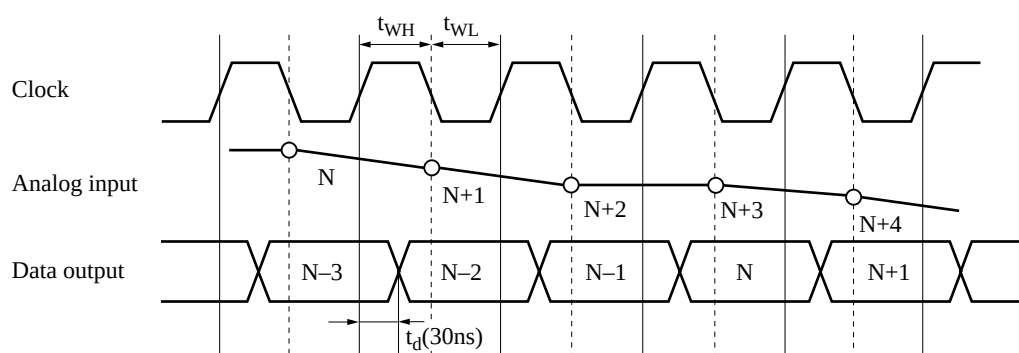
Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V_{DD}	4.50	5.00	5.25	V
Power supply voltage for digital output circuits	DV_{DDL}	3.0		3.6	V
Digital input voltage	"H" level	V_{IH}	2.4	V_{DD}	V
	"L" level	V_{IL}	V_{SS}	0.8	V
Reference voltage	"H" level	V_{RT}	3.0	V_{DD}	V
	"L" level	V_{RB}	V_{SS}	2.0	V
Clock	"H" level pulse width	t_{WH}	25		ns
	"L" level pulse width	t_{WL}	25		ns
Analog input voltage	V_{AIN}	V_{SS}		V_{DD}	V

■ Electrical Characteristics $V_{DD}=AV_{DD}=DV_{DD}=4.5\text{V}$, $DV_{DDL}=3.0\text{V}$, $AV_{SS}=DV_{SS}=0\text{V}$, $T_a=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Power consumption	P_C	$V_{DD}=5.0\text{V}$, $DV_{DDL}=3.3\text{V}$, $f_{CLK}=16\text{MSPS}$ (not including reference current)		120	150	mW
Resolution	RES			9		bit
Linearity error	E_L	$f_{CLK}=16\text{MSPS}$		± 2.5	± 3.5	LSB
Differential linearity error	E_D	$V_{RT}=3.3\text{V}$ $V_{RB}=1.3\text{V}$		± 0.6	± 1.0	LSB
Maximum conversion rate	$F_{C(max.)}$		16			MSPS
Clock frequency	f_{CLK}		1		16	MHz
Analog input dynamic range	D_R		2		$V_{RT}-V_{RB}$	V
Output current	"H" level	I_{OH} $V_{OH}=DV_{DDL}-0.8\text{V}$, $V_{DD}=5.0\text{V}$, $DV_{DDL}=3.3\text{V}$			-2	mA
	"L" level	I_{OL} $V_{OL}=0.4\text{V}$, $V_{DD}=5.0\text{V}$ $DV_{DDL}=3.3\text{V}$	2			mA
Output delay time	t_d	$V_{DD}=5.0\text{V}$, $DV_{DDL}=3.3\text{V}$, $C_L=10\text{pF}$	10	30	45	ns
Analog input capacitance	C_I	$V_{DD}=5.0\text{V}$		26		pF

■ Timing Chart

The chip samples the analog input at the falling edge of the clock signal and provides the corresponding digital output 2.5 clock cycles later at the rising edge of the clock signal.



Note: The circles indicate analog signal sampling points.

■ Package Dimensions (Unit:mm)

QFH032-P-0707

