MN6732741

Signal-processing IC for surveillance cameras and cameras for PC input

■ Overview

The MN6732741 is camera signal-processing IC appropriate for a wide variety of applications, including surveillance cameras and cameras used for input to personal computers. In addition to the basic functions of luminance and chrominance signal processing, it also integrates the ALC, AWB, and AGC functions that were previously implemented using microcontroller signal processing. Furthermore, it also integrates on a single chip, including SSG, CG, and I²C-bus functions.

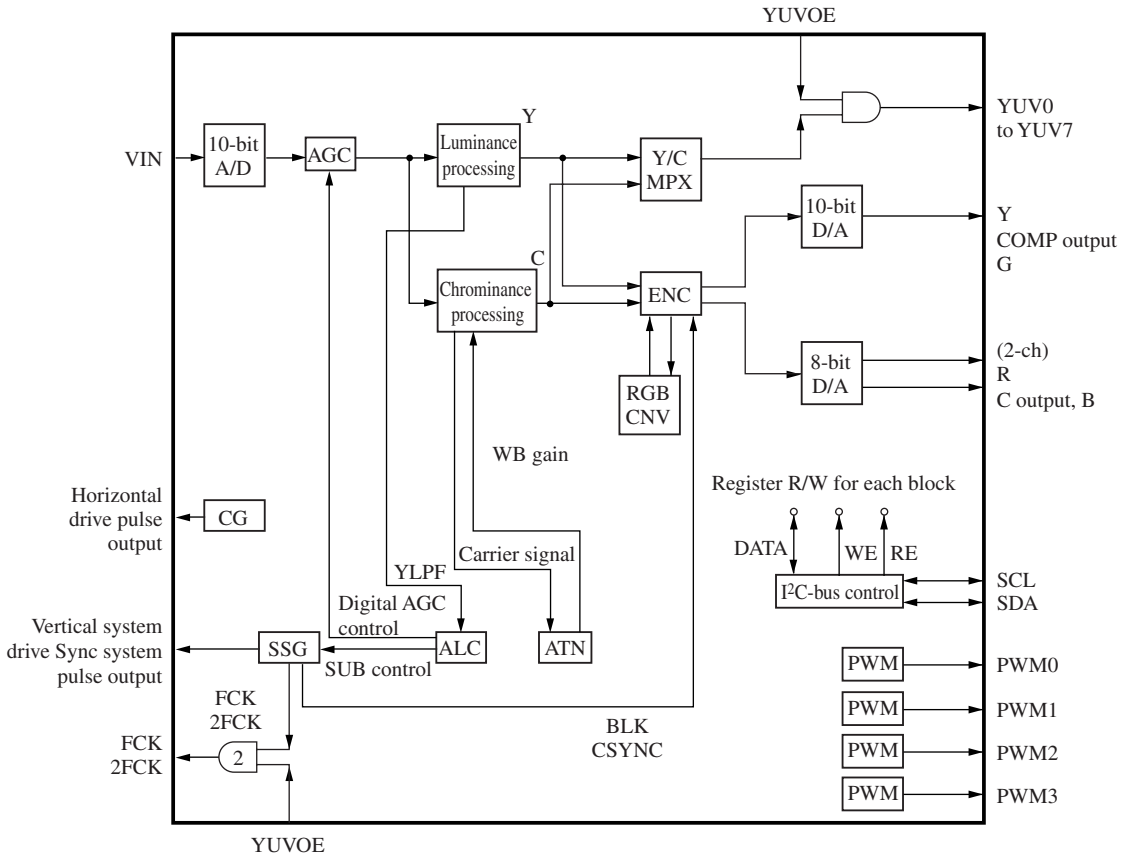
■ Features

- Input: Analog signal (A/D converter input)
- Outputs: Digital output
  - 8-bit YUV signal
  - Analog outputs
    - Luminance signal
    - Chrominance signal
    - Composite video signal output
    - RGB output
- Operating supply voltage: 3.3 V ± 0.3 V
- Operating clock frequency: 9.5 MHz to 28.7 MHz
- Main functions
  - 10-bit A/D converter
  - Single-channel 10-bit D/A converter
  - Two-channel 8-bit D/A converter
  - Supports analog AGC (NN2038 or NN2039)
  - CG and SSG circuits
  - Supports 510 and 768 horizontal lines (NTSC and PAL)
  - Supports VGA progressive scan readout CCDs (complementary color filters)
  - Also supports black-and-white CCD signal processing
  - CCD white defect/black defect correction circuit
  - Digital AGC gain: up to 24 dB
  - Left/right reversing function
  - Variable gamma correction ($\gamma = 0.3$ to 1)
  - ZV port standard mode, BT656 standard mode
  - Modes: LL, SYNC, VD2, and HD/VD external synchronization support
  - Built-in I²C-bus circuit
  - ALC and AGC (Also supports external AGC)
  - Two white balance modes (manual and ATW) with ATW lock function
  - Automatic OB correction function

■ Applications

- Surveillance cameras, PC input cameras, multimedia cameras

■ Block Diagram



■ Function Descriptions (by circuit block)

1. ADC

Converts the post-CDS CCD signal to a 10-bit digital signal.

2. PATGEN

Generates test pattern signals. This circuit generates horizontal and vertical patterns with a color bar (3 colors) format. Since it simulates the output of the CCD 4-color complementary color filters, it conveniently allows problems in the analog block, from the CCD to the A/D converter, and IC internal problems, to be isolated. It can also be used to temporarily halt CCD image output and generate a blue background signal.

3. AGC (AGC, pixel mixing, mirror reversal, and OB clamping functions)

Performs AGC control (up to +24 dB) digitally by linking with the ALC. Since the IC also provides an interface output to an external analog AGC (NN2038 or NN2039), over 24 dB of gain can be provided.

When a VGA CCD is used, since progressive scan is used, the photodiode mixing operation used with earlier interlaced CCDs is not required. The AGC circuit includes an internal pixel mixing circuit, and is designed for both progressive and interlaced scan at the circuit level.

In the mirror mode provided by 510 H and 768 H CCDs, it is possible to generate a reversed video signal by controlling RAM. OB correction is also performed in this block, and this function has both a digital mode, in which processing is performed internally to the IC, and an analog mode that controls the external CDS and AGC IC clamp voltage.

■ Function Descriptions (by circuit block) (continued)

4. ALC

The ALC block controls the exposure electronically by inputting the luminance signal, taking an averaged but center weighted exposure reading over the whole image, and comparing that to the target value. That result is used to control the CCD's electronic shutter.

In ELC mode, since the step size of the electronic shutter accumulation time is discrete, the AGC system is used in conjunction with the ALC function to create a smoothly operating control system. This block also performs a 3-field averaging flicker correction operation as well.

5. Luminance system

After generating the luminance signal from the complementary color filter CCD output using a low-pass filter, this block generates the horizontal and vertical aperture signals and performs coring/low-luminance suppression, gamma correction, and blanking processing.

This block includes a defect correction circuit that corrects for defective pixels in the CCD. One of two outline correction levels can be selected with the APGAIN pin.

The IC also includes a defect correction circuit that corrects for missing pixels in the CCD. The gamma correction is continuously variable from $\gamma = 0.3$ to 1. The luminance signal low-pass filter can be bypassed to allow this device to handle black-and-white CCDs.

6. Chrominance system

This block performs white balance processing, carrier balance, color temperature correction, and low-luminance/high-luminance chrominance suppression processing.

7. AWB

This block generates the auto white balance control signal. This white balance function operates so that the state of the immediately prior and proper illumination level will be held in case of low illumination levels.

8. ENC

This block converts between NTSC and PAL. A digital technique in which $4f_{SC}$ is created from FSC is adopted, and the clock system is unified into a single system. To create the composite video signal, clock rate conversion is also applied to the Y signal and the signals are mixed digitally. The sync signal can also be mixed digitally.

9. RGBCNV

The YUV signal generated from the luminance and chrominance signals is converted to RGB using a matrix. However, since the band of the UV signal is dropped to around 800 kHz at a relatively early stage relative to the chrominance signal, this is not a signal in which all three channels have the same wide band as the Y signal, such as the signals used in 3-CCD video cameras.

10. YCMPX

This block takes the FCK rate luminance and UV signals and outputs them as an 8-bit time-division multiplexed signal with a 2FCK rate.

In BT656 standard mode, SAV and EAV are embedded in the signal.

11. D/A converters

One D/A converter block converts the digital input to analog output. There are three channels, and one channel with a 10-bit resolution is provided for each of the composite, Y, and G signals. The circuit is designed so that the sync can be mixed digitally.

The remaining D/A converter is a two-channel 8-bit device used for the chrominance, R, and B signals.

12. PWM

Provides an independently controllable 4-channel PWM output circuit that can be used to control analog circuits peripheral to the IC. These outputs can be used, for example, for VREF adjustment of D/A converter.

13. CG

This circuit generates the high-speed pulse signals (H1, H2, DS1, and DS2) used by the CCD.

This block's logic system power supply is isolated from the other IC internal logic circuits to minimize noise.

■ Function Descriptions (by circuit block) (continued)

14. SSG

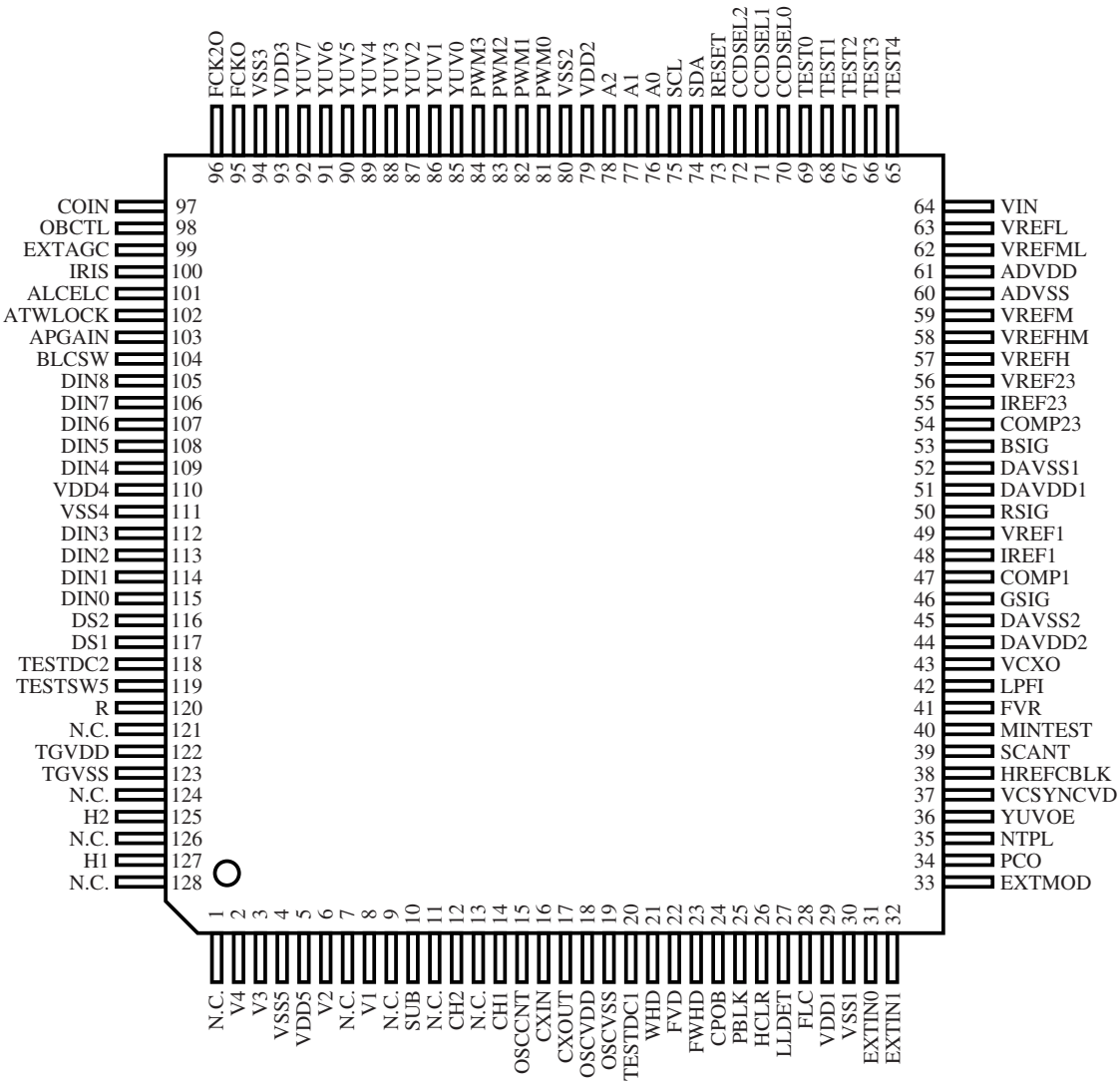
This block generates both low-speed pulse signals used by the CCD and various kinds of pulse signals used for signal processing. (However, note that VBSGEN locking is not supported.)

15. I²C-bus

When power is first applied, the contents of an external EEPROM are read out and used to set the IC internal registers.

Since this circuit does not support multi-master operation, no external devices will have become bus master when power is first applied. This I²C-bus also can be used by external devices to read or write the IC internal registers. (Note that certain limitations apply.)

■ Pin Arrangement



(TOP VIEW)

■ Pin Descriptions

Pin No.	Pin	I/O	Description
1	N.C.	—	—
2	V4	O	ϕV4 charge pulse
3	V3	O	ϕV3 charge pulse
4	VSS5	VSS	Digital system ground
5	VDD5	VDD	Digital system power supply (3.3 V)
6	V2	O	ϕV2 charge pulse
7	N.C.	—	—
8	V1	O	ϕV1 charge pulse
9	N.C.	—	—
10	SUB	O	Vertical removal pulse
11	N.C.	—	—
12	CH2	O	V3 charge pulse
13	N.C.	—	—
14	CH1	O	V1 charge pulse
15	OSCCNT	O	Oscillator control test
16	CXIN	I	Synchronization oscillator (crystal oscillator)
17	CXOUT	O	Synchronization oscillator (crystal oscillator)
18	OSCVDD	VDD	Oscillator cell power supply
19	OSCVSS	VSS	Oscillator cell ground
20	TESTDC1	I	Test input (Normally connect to low.)
21	WHD	O	WHD signal that is in proper phase relative to the sync signal
22	FVD	O	VD signal that is in proper phase relative to the sync signal
23	FWHD	O	WHD for TG drive
24	CPOB	O	A/D converter input signal clamp pulse, or D/A converter output clamp pulse
25	PBLK	O	Pre-blanking pulse
26	HCLR	O	Horizontal reference signal
27	LLDET	I	Power supply synchronization switching signal Low: internal synchronization, High: LL synchronization
28	FLC	I	Flicker correction (pulled up). High: Flicker correction on
29	VDD1	VDD	Digital system power supply (3.3 V)
30	VSS1	VSS	Digital system ground
31	EXTIN0	I	External sync signal input 1
32	EXTIN1	I	External sync signal input 2
33	EXTMOD	I	Monitor/automotive mode switch (pulled up) High: Automotive mode (HDVD/SYNC synchronization mode)
34	PCO	O	Phase comparator output
35	NTPL	I	NTSC/PAL switching. Low: NTSC, High: PAL (pulled down)

■ Pin Descriptions (continued)

Pin No.	Pin	I/O	Description
36	YUVOE	I	Digital output system output enable
37	VCSYNCVD	O	VCSYNC output/VD output (VGA mode CSYNC/IT mode register switching)
38	HREFCBLK	O	HREF output/CBLK output (VGA mode HREF/IT mode register switching)
39	SCANT	I	Test input (Normally connect to low.)
40	MINTEST	I	Test input (Normally connect to low.)
41	FVR	I	Frequency control DC input
42	LPFI	I	Low-pass filter analog switch input
43	VCXO	O	Analog switch output. LC oscillator
44	DAVDD2	VDD	D/A converter power supply
45	DAVSS2	VSS	D/A converter ground
46	GSIG	O	Video signal output (composite/luminance signal/G signal) (Connect R_L between this pin and DAVSS2.)
47	COMP1	I	Phase compensation (Connect a 1 µF capacitor between this pin and DAVSS2.)
48	IREF1	I	Bias current setting resistor connection (Connect R_{IREF} between this pin and DAVSS2.)
49	VREF1	I	Reference voltage input
50	RSIG	O	Video signal output (R signal)
51	DAVDD1	VDD	D/A converter power supply
52	DAVSS1	VSS	D/A converter ground
53	BSIG	O	Video signal output (Chrominance signal/B signal)
54	COMP23	I	Phase compensation (Connect a 1 µF capacitor between this pin and DAVSS1.)
55	IREF23	I	Bias current setting resistor connection (Connect RIREF between this pin and DAVSS1.)
56	VREF23	I	Reference voltage input
57	VREFH	I	High-level reference voltage input
58	VREFHM	I	Mid-level reference voltage (Connect this pin to ADVSS through a capacitor.)
59	VREFM	I	Mid-level reference voltage (Connect this pin to ADVSS through a capacitor.)
60	ADVSS	VSS	A/D converter ground
61	ADVDD	VDD	A/D converter power supply
62	VREFML	I	Mid-level reference voltage (Connect this pin to ADVSS through a capacitor.)
63	VREFL	I	Low-level reference voltage input
64	VIN	I	Analog signal input
65	TEST4	I	Test input (Normally connect to low.)
66	TEST3	I	Test input (Normally connect to low.)
67	TEST2	I	Test input (Normally connect to low.)
68	TEST1	I	Test input (Normally connect to low.)
69	TEST0	I	Test input (Normally connect to low.)
70	CCDSEL0	I	CCD switching
71	CCDSEL1	I	CCD switching

■ Pin Descriptions (continued)

Pin No.	Pin	I/O	Description
72	CCDSEL2	I	CCD switching
73	RESET	I	Logic system initial reset
74	SDA	I/O	I^2C-bus (data)
75	SCL	I/O	I^2C-bus (clock)
76	A0	I	EEPROM address setting (pulled down)
77	A1	I	EEPROM address setting (pulled down)
78	A2	I	EEPROM address setting (pulled down)
79	VDD2	VDD	Digital system power supply (3.3 V)
80	VSS2	VSS	Digital system ground
81	PWM0	O	PWM signal output
82	PWM1	O	PWM signal output
83	PWM2	O	PWM signal output
84	PWM3	O	PWM signal output
85	YUV0	O	Digital Y/UV output (LSB)
86	YUV1	O	Digital Y/UV output
87	YUV2	O	Digital Y/UV output
88	YUV3	O	Digital Y/UV output
89	YUV4	O	Digital Y/UV output
90	YUV5	O	Digital Y/UV output
91	YUV6	O	Digital Y/UV output
92	YUV7	O	Digital Y/UV output (MSB)
93	VDD3	VDD	Digital system power supply (3.3 V)
94	VSS3	VSS	Digital system ground
95	FCKO	O	FCK output
96	FCK2O	O	2FCK output
97	COIN	I	Synchronization oscillator cell (LC oscillator)
98	OBCTL	O	OB automatic correction output
99	EXTAGC	O	External AGC control
100	IRIS	O	Mechanical iris fixation (PWM output)
101	ALCELC	I	Fixed/ELC switching. Low: ELC, High: Fixed
102	ATWLOCK	I	ATW/Stop. Low: Normal, High: ATWLOCK
103	APGAIN	I	Aperture gain switching. Low: Register value High: One half of the register value
104	BLCSW	I	Backlighting correction. Low: Normal, High: ATWLOCK
105	DIN8	I	Digital signal input (MSB)
106	DIN7	I	Digital signal input
107	DIN6	I	Digital signal input
108	DIN5	I	Digital signal input

■ Pin Descriptions (continued)

Pin No.	Pin	I/O	Description
109	DIN4	I	Digital signal input
110	VDD4	VDD	Digital system power supply (3.3 V)
111	VSS4	VSS	Digital system ground
112	DIN3	I	Digital signal input
113	DIN2	I	Digital signal input
114	DIN1	I	Digital signal input
115	DIN0	I	Digital signal input (LSB)
116	DS2	O	CDS pulse 1
117	DS1	O	CDS pulse 2
118	TESTDC2	I	Test input (Normally connect to low.)
119	TESTSW5	I	Test input (Normally connect to low.)
120	R	O	ϕR pulse
121	N.C.	—	—
122	TGVDD	VDD	TG power supply
123	TGVSS	VSS	TG ground
124	N.C.	—	—
125	H2	O	ϕH1 transfer pulse
126	N.C.	—	—
127	H1	O	ϕH2 transfer pulse
128	N.C.	—	—

■ Electrical Characteristics

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (digital)	V_{DD}	– 0.3 to +4.6	V
Supply voltage (analog)	AV_{DD}	– 0.3 to +4.6	V
Input voltage	V_I	– 0.3 to V_{DD}+0.3	V
Output voltage	V_O	– 0.3 to V_{DD}+0.3	V
Output current	I_O	±48	mA
Power dissipation	P_D	750	mW
Operating temperature	T_{opr}	–20 to +70	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) 1. The absolute maximum ratings are limit values for stresses applied to the chip so that the chip will not be destroyed. Operation is not guaranteed within these ranges.

2. Always apply the identical potential to the following pins: VDD1, VDD2, VDD3, VDD4, VDD5, VDDTG, ADVDD, DAVDD1, and DAVDD2.
Always apply the identical potential to the following pins: VSS1, VSS2, VSS3, VSS4, VSS5, VSSTG, ADVSS, DAVSS1, and DAVSS2.

■ Electrical Characteristics (continued)

2. Recommended Operating Conditions at V_{SS} = TGV_{SS} = $OSCV_{SS}$ = ADV_{SS} = DAV_{SS} = 0 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage (digital)	V_{DD}	Digital system power supply	3.0	3.3	3.6	V
	TGV_{DD}	TG power supply	3.0	3.3	3.6	
	$OSCV_{DD}$	Oscillator power supply	3.0	3.3	3.6	
Supply voltage (analog)	ADV_{DD}	A/D converter power supply	—	3.3	—	V
	DAV_{DD}	D/A converter power supply	—	3.3	—	
Operating frequency	f_{osc}	duty 50%	9.5	—	28.7	MHz

3. DC Characteristics at V_{DD} = TGV_{DD} = $OSCV_{DD}$ = 3.0 V to 3.6 V, ADV_{DD} = DAV_{DD} = 3.0 V to 3.6 V, V_{SS} = TGV_{SS} = $OSCV_{SS}$ = ADV_{SS} = DAV_{SS} = 0 V, T_a = -20°C to +70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating supply current	I_{DD}	V_{DD} = TGV_{DD} = $OSCV_{DD}$ = 3.6 V,	—	80	120	mA
	DAI_{DD}	ADV_{DD} = DAV_{DD} = 3.6 V,	—	23	33	
	ADI_{DD}	f_{CLK} = 28.7 MHz, T_a = 25°C	—	20	40	

1) Input pins 1-1: Standard input pins
LLDET, EXTIN0, EXTIN1, YUVOE, CCDSEL0 to CCDSEL2, RESET, COIN, ALCELC, ATWLOCK, APGAIN, BLCSW, DIN8 to DIN0, TESTDC2, TESTSW5

Input voltage	High level	V_{IH}		$V_{DD}\times0.8$	—	V_{DD}	V
	Low level	V_{IL}		0	—	$V_{DD}\times0.2$	
Input leakage current		I_{LIPD}	$V_I = V_{DD}$ or V_{SS}	−5	—	5	µA

2) Input pins 1-2: Pulled-up input pins FLC, EXTMOD

Input voltage	High level	V_{IH}		$V_{DD}\times0.8$	—	V_{DD}	V
	Low level	V_{IL}		0	—	$V_{DD}\times0.2$	
Input leakage current		I_{LIPD}	$V_I = V_{DD}$	−10	—	10	µA
Pull-up resistance		R_{PU1}	V_{DD} = 3.3 V, $V_I = V_{SS}$	10	30	90	kΩ

3) Input pins 1-3: Pulled-down input pins TESTDC1, NTPL, SCANT, A0 to A2, MINTEST, TEST4 to TEST0

Input voltage	High level	V_{IH}		$V_{DD}\times0.8$	—	V_{DD}	V
	Low level	V_{IL}		0	—	$V_{DD}\times0.2$	
Input leakage current		I_{LIPD}	$V_I = V_{SS}$	−10	—	10	µA
Pull-down resistance		R_{PD1}	$V_I = V_{DD}$	10	30	90	kΩ

4) Output pins 1-1 V4 to V1, SUB, CH2, CH1, OSCCNT, WHD, CPOB, PBLK, HCLR, PCO, PWM0 to PWM3, OBCTL, EXTAGC, IRIS

Output voltage	High level	V_{OH}	I_O = −1 mA	$V_{DD}-0.6$	—	—	V
	Low level	V_{OL}	I_O = 1 mA	—	—	0.4	

5) Output pins 1-2 YUV0 to YUV7

Output voltage	High level	V_{OH}	I_O = −2 mA	$V_{DD}-0.6$	—	—	V
	Low level	V_{OL}	I_O = 2 mA	—	—	0.4	

■ Electrical Characteristics (continued)

3. DC Characteristics at V_{DD} = TGV_{DD} = $OSCV_{DD}$ = 3.0 V to 3.6 V, ADV_{DD} = DAV_{DD} = 3.0 V to 3.6 V, V_{SS} = TGV_{SS} = $OSCV_{SS}$ = ADV_{SS} = DAV_{SS} = 0 V, T_a = -20°C to +70°C (continued)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
6) Output pins 1-3 VCSYNCVD, HREFCBLK							
Output voltage	High level	V_{OH}	I_O = −4 mA	V_{DD} − 0.6	—	—	V
	Low level	V_{OL}	I_O = 4 mA	—	—	0.4	
7) Output pins 1-4 FVD, FWHD, FCKO, FCK2O							
Output voltage	High level	V_{OH}	I_O = −8 mA	V_{DD} − 0.6	—	—	V
	Low level	V_{OL}	I_O = 8 mA	—	—	0.4	
8) Output pins 1-5 DS2, DS1, R, H2, H1							
Output voltage	High level	V_{OH}	I_O = −16 mA	V_{DD} − 0.6	—	—	V
	Low level	V_{OL}	I_O = 16 mA	—	—	0.4	
9) I/O pins 1 SDA, SCL							
TTL Schmitt trigger input voltage	Input threshold voltage	V_{T+}	V_{DD} = 3.0 V to 3.6 V V_{ref5} = 4.75 V to 5.25 V	—	1.6	2.2	V
		V_{T-}	(V_{ref5} is an external reference voltage.)	0.6	1.2	—	
Output voltage	Low level	V_{OL}	I_O = 4 mA	—	—	0.4	V
Output leakage current		I_{LO}	V_O = V_{DD} or V_{SS}	−10	—	10	µA
10) Oscillator pins 1 CXIN, CXOUT							
Standard oscillator frequency		f_{OSC}	V_{DD} = 3.3 V, with an external crystal	15	—	30	MHz
Internal feedback resistance		R_{FB}	V_{DD} = 3.3 V V_I (X_I) = V_{DD} or V_{SS}	0.73	2.2	6.6	kΩ
Output current	High level	I_{OH}	V_{DD} = 3.3 V V_I = V_{SS} , V_O = V_{SS}	–57.5	–23	–9.2	mA
	Low level	I_{OL}	V_{DD} = 3.3 V V_I = V_{DD} , V_O = V_{DD}	9.6	24	60	

4. AC Characteristics

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Input pins 2-1 CXIN							
Clock waveform	Period	t_{cyc}	See figure 1	34.8	—	105.3	ns
	Clock duty	d_{clk}	See figure 1 d_{clk} = t_{hi} /t_{cyc}	—	50	—	%

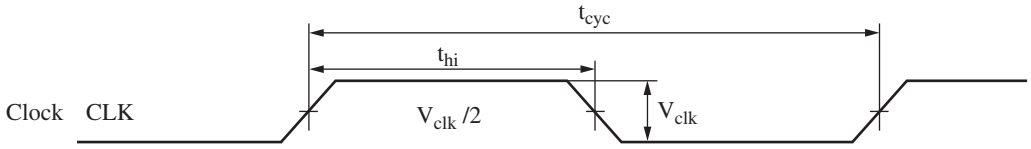


Figure 1. Clock waveform

■ Electrical Characteristics (continued)

5. A/D converter at V_{DD} = TGV_{DD} = $OSCV_{DD}$ = 3.3 V, ADV_{DD} = DAV_{DD} = 3.3 V, V_{SS} = TGV_{SS} = $OSCV_{SS}$ = ADV_{SS} = DAV_{SS} = 0 V, T_a = 25°C

Pins: VIN, VREFH, VREFL, VREFM, VREFML, VREFHM

Parameter	Symbol	Condition	Min	Typ	Max	Unit
1) A/D converter recommended operating conditions						
Analog input voltage	V_{AIN}	VIN	VREFL	—	VREFH	V
Analog input pin capacitance	C_{AI}	VIN	—	330	—	pF
High-level reference voltage	V_{REFH}	VREFH	—	2.5	—	V
Low-level reference voltage	V_{REFL}	VREFL	—	0.5	—	V
Reference resistance (VREFL to VREFH)	R_{REF}		—	440	—	Ω
2) A/D converter characteristics						
Resolution	R_{ES}		—	—	10	bit
Nonlinearity error	INL	f_{ADCK} = 14.3 MHz	—	±5.0	±7.5	LSB
Differential nonlinearity error	DNL	V_{REFH} = 2.5 V V_{REFL} = 0.5 V	—	±2.0	±6.5	LSB
Analog input dynamic range	V_{AIN}		—	—	V_{REFH} – V_{REFL}	V[p-p]

6. D/A converter at V_{DD} = TGV_{DD} = $OSCV_{DD}$ = 3.3 V, ADV_{DD} = DAV_{DD} = 3.3 V, V_{SS} = TGV_{SS} = $OSCV_{SS}$ = ADV_{SS} = DAV_{SS} = 0 V, T_a = 25°C

1) Pins: VREF23, IREF23, COMP23, BSIG, RSIG

Parameter	Symbol	Condition	Min	Typ	Max	Unit
(1) D/A converter recommended operating conditions						
Reference voltage	VREF	R_L = 75 Ω RIREF23 = 820 Ω	—	1.37	—	V
External phase compensation capacitor	C_{COMP}	Connected between COMP23 and AV_{DD}.	—	1.0	—	µF
External output resistors	R_L	Connect output resistors between each of the BSIG and RSIG pins and AV_{SS}.	—	75	—	Ω
External bias current setting resistor	R_{IREF}	Connect this resistor between IREF23 and AV_{SS}.	—	820	—	Ω
(2) D/A converter characteristics						
Resolution	R_{ES}		—	—	8	bit
Nonlinearity error	INL	R_L = 75 Ω VREF23 = 1.37 V RIREF23 = 820 Ω	—	—	±2.5	LSB
Differential nonlinearity error	DNL		—	—	±2.5	LSB
Full-scale voltage	V_{OFS}		—	1.0	—	V
Zero-scale voltage	V_{OZS}		—	0	—	V

■ Electrical Characteristics (continued)

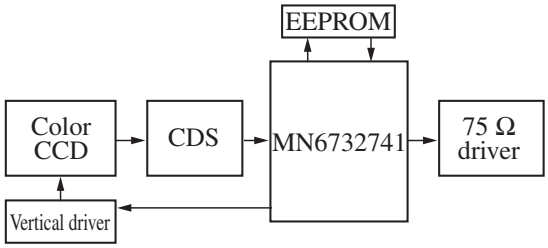
6. D/A converter at V_{DD} = TGV_{DD} = $OSCV_{DD}$ = 3.3 V, ADV_{DD} = DAV_{DD} = 3.3 V, V_{SS} = TGV_{SS} = $OSCV_{SS}$ = ADV_{SS} = DAV_{SS} = 0 V, T_a = 25°C (continued)

2) Pins: VREF1, IREF1, COMP1, GSIG

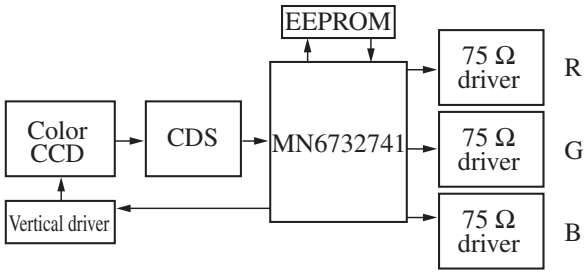
Parameter	Symbol	Condition	Min	Typ	Max	Unit
(1) D/A converter recommended operating conditions						
Reference voltage	VREF	R_L = 75 Ω RIREF1 = 1.13 kΩ	—	1.5	—	V
External phase compensation capacitor	C_{COMP}	Connect between COMP1 and AV_{DD}.	—	1.0	—	µF
External output resistor	R_L	Connect an output resistor between GSIG and AV_{SS}.	—	75	—	Ω
External bias current setting resistor	R_{IREF}	Connect this resistor between IREF1 and AV_{SS}.	—	1.13	—	kΩ
(2) D/A converter characteristics						
Resolution	R_{ES}		—	—	10	bit
Nonlinearity error	INL	R_L = 75 Ω VREF1 = 1.5 V RIREF1 = 1.13 kΩ	—	—	±2.5	LSB
Differential nonlinearity error	DNL		—	—	±2.5	LSB
Full-scale voltage	V_{OFS}		—	1.0	—	V
Zero-scale voltage	V_{OZS}		—	0	—	V

■ Application System Examples

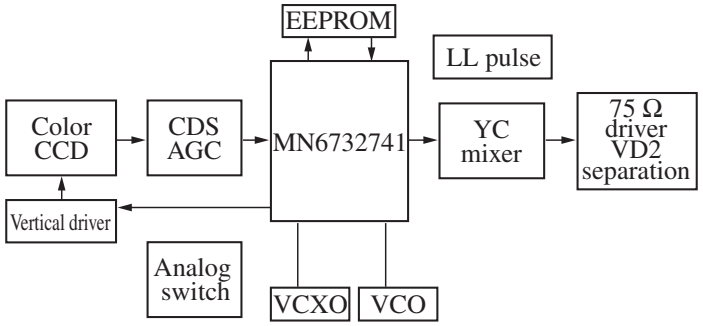
1. Example A (Minimum configuration)
   - Internal synchronization
   - Composite video output



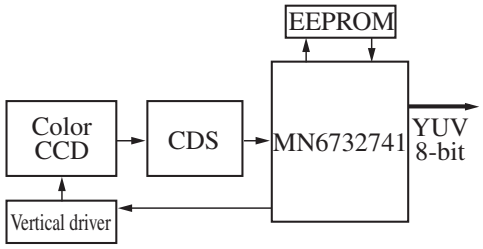
2. Example B
   - Internal synchronization
   - RGB output



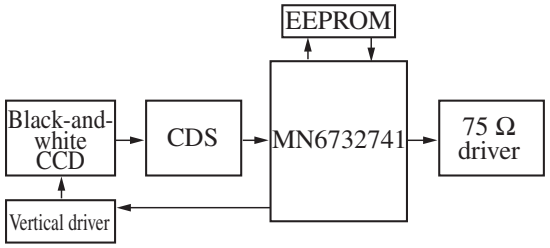
3. Example C (Surveillance camera)
   - External synchronization
   - YC output



4. Example D (PC camera)
   - Internal synchronization
   - Digital output

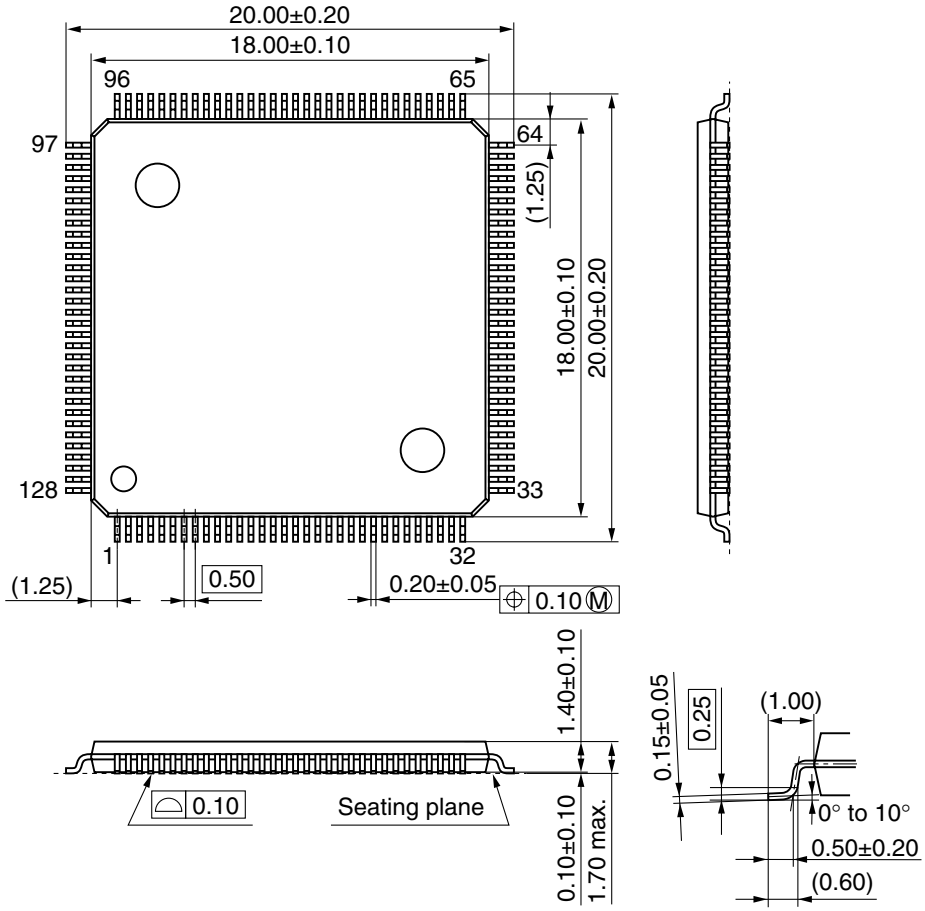


5. Example E
   - Internal synchronization
   - Y output



■ Package Dimensions (Units: mm)

• LQFP128-P-1818C



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