MN88831

PCM Audio Decoder LSI for Satellite Broadcasting Tuners (Includes Built-In Digital Filter and D/A Converter)

■ Overview

The MN88831 greatly streamlines set design by incorporating a satellite broadcasting PCM audio decoder, a switched capacitor D/A converter, and analog post filter to a single chip.

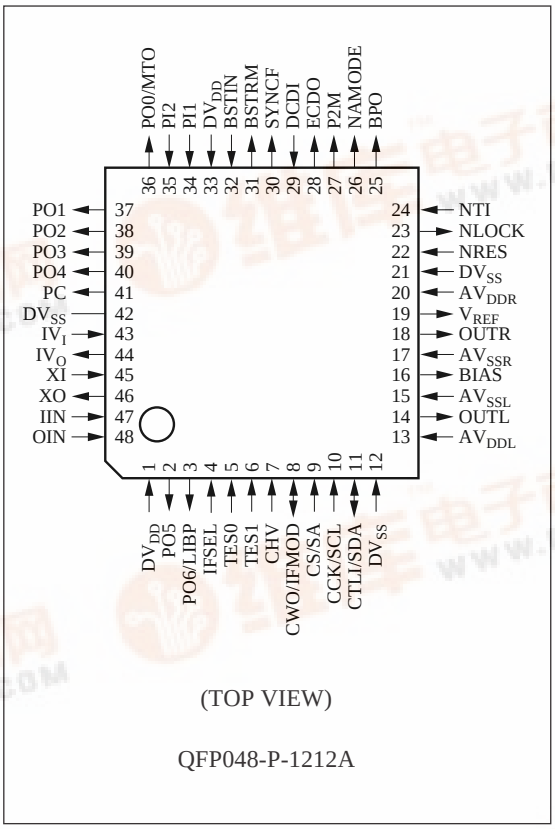
■ Features

- Built-in digital filter using 8-fold oversampling
- Built-in tertiary Δ-∑ noise shaping D/A converter
- Reduced jitter noise through use of switched capacitor configuration
- Built-in analog post filter
- Built-in digital de-emphasis circuit
- Choice of microcomputer interfaces with selector pin: 3-wired serial interface or I²C interface
- Muting function supporting following settings
  - Pay-per-view flag detection
  - Error frequency detection
  - Detection of control code bit-7
- Built-in general-purpose microcomputer I/O port
- Bit stream input pin supporting 0.4 V_{P-P} input

■ Applications

- Satellite broadcasting tuners (BS, CS)

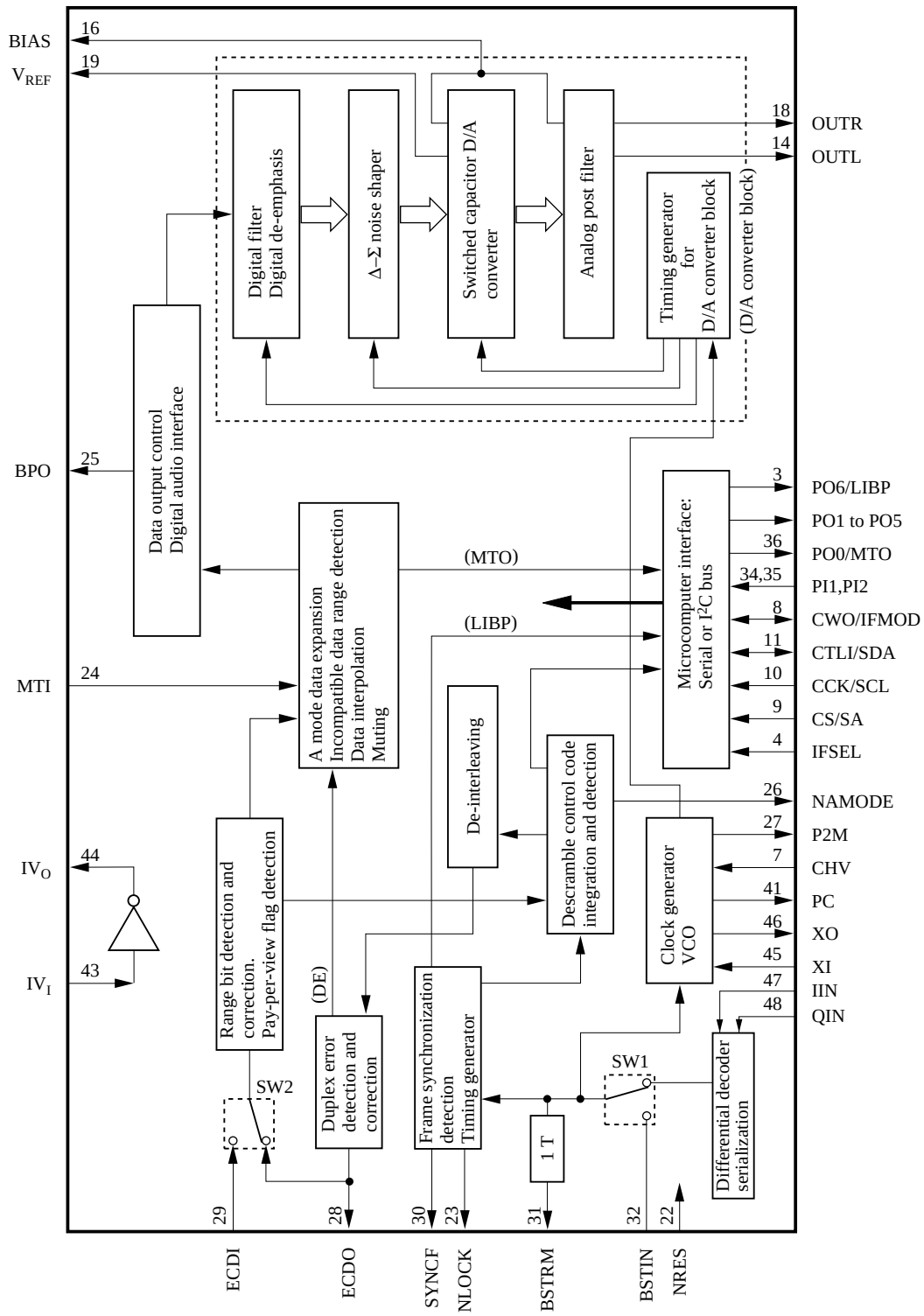
■ Pin Assignment



(TOP VIEW)

QFP048-P-1212A

■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	– 0.3 to 7.0	V
Input voltage	V_I	– 0.3 to V_{DD} +0.3	V
Output voltage	V_O	– 0.3 to V_{DD} +0.3	V
Output current	I_O	25	mA
Power dissipation	P_D	480	mW
Operating temperature	T_{opr}	–20 to +70	˚C
Storage temperature	T_{stg}	–55 to +125	˚C

Notes:

1. The above ratings represent the maximum values that may be applied without damaging the chip, not the limits for guaranteed operation.

2. If the chip is to be used in the presence of strong electric fields—under a CRT tube, for example—apply shielding to the package surface to ensure proper operation.

3. The power dissipation is for an ambient temperature (Ta) of 70˚C.

4. The voltages applied to the pins CCK/SCL, CTLI/SDA, CWO/IFMOD, PO0/MTO, PO1–PO5, and PO6/LIBP must be within the range between –0.3V and 5.5V when the power is off.

■ Operating Conditions

$DV_{SS}=AV_{SS}=0V$

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Power supply voltage for digital circuits	DV_{DD}	(*1)	4.5	5.0	5.5	V
Power supply voltage for analog circuits	AV_{DD}	(*2)	4.5	5.0	5.5	V
XI clock frequency	f_{XI}	CHV="H" (256fs mode)		12.288		MHz
XI clock frequency	f_{XI}	CHV="L" (384fs mode)		18.432		MHz
XI clock input amplitude	—	C cut input	0.8		3.0	V_{P-P}
BSTIN input amplitude	—	C cut input	0.35	0.5		V_{P-P}
Ambient temperature during operation	Ta		–20		+70	˚C

Notes:

1. *1 & *2:

   For the logic portions of the microcomputer interface, DV_{DD} min = 4.0V.

   AV_{DD} covers both AV_{DDL} and AV_{DDR}.

   AV_{SS} covers both AV_{SSL} and AV_{SSR}.

   Analog characteristics are only guaranteed for DV_{DD} = AV_{DD} = 5.0V.

2. Always use low-impedance external connections for V_{DD} and V_{SS}.
   Always connect the two through a bypass capacitor of at least 0.01 µF to ensure proper operation.

3. Keep the NRES pin (pin No. 22) at "L" level to prevent operation error of the CTLI/SDA pin in the I^2C interface at voltages lower than the guaranteed operating power supply voltage.

■ Electrical Characteristics

(1) DC characteristics

AV_{DD}=DV_{DD}=4.5 to 5.5V, AV_{SS}=DV_{SS}=0V, Ta= –20 to +70˚C

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Power supply current	I_{DD1}	No load, V_{DD}=5.5V 384fs		56	80	mA
	I_{DD2}	No load, V_{DD}=5.5V 256fs		56	80	mA
Digital input pins 1 (*1)						
"H" level input voltage	V_{IH1}		0.7 × DV_{DD}		DV_{DD}	V
"L" level input voltage	V_{IL1}		DV_{SS}		0.3 × DV_{DD}	V
Digital input pins 2 (*2)						
"H" level input voltage	V_{IH2}		0.8 × DV_{DD}		DV_{DD}	V
"L" level input voltage	V_{IL2}		DV_{SS}		0.2 × DV_{DD}	V
Digital output pins 1 (*3)						
"H" level output voltage	V_{OH1}	I_{OH1}= –1mA	DV_{DD} – 0.8			V
"L" level output voltage	V_{OL1}	I_{OL1}=+1mA			0.5	V
Digital output pins 2 (*4)						
"L" level output voltage	V_{OL2}	I_{OL2}=+1mA			0.5	V
High-impedance output leakage current	I_{LO}	V_O=High-impedance state V_I=0V to DV_{DD}			±10	µA
Digital output pins 3 (*5)						
"L" level output voltage	V_{OL3}	I_{OL3}=+1mA			0.5	V
High-impedance output leakage current	I_{LO2}	V_I=0V to DV_{DD} V_{NRES}=0V to 0.5V			±50	µA
Analog output pins						
VREF pin output pin	V_{REF}			0.45 × AV_{DD}		V
BIAS pin output pin	V_{BIAS}			0.5 × AV_{DD}		V
IVI-IVO inverter						
Inverter input threshold voltage	V_{TI}		0.5 × DV_{DD} ± 0.75			V

Notes:

*1: IFSEL, TES0, TES1, CHV, MTI, ECDI, PI1, PI2, IIN, QIN, CWO/IFMOD (C3, C4 only), IVI (C5 only)

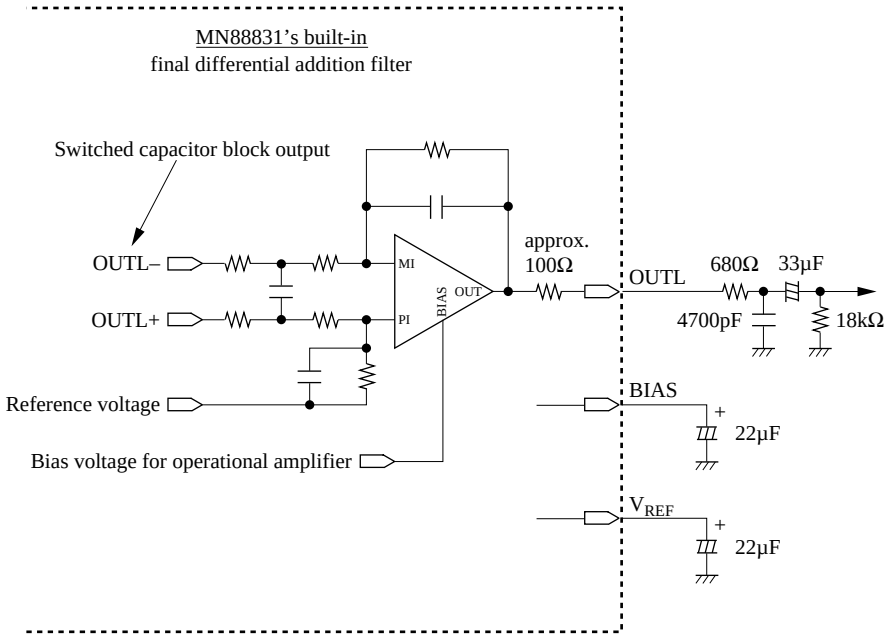
*2: CS/SA, CCK/SCL, NRES, CTLI/SDA (C6, C7 only)

*3: NLOCK, BPO, NAMODE, P2M, ECDO, SYNCF, BSTRM, PC

*4: PO0/MTO, PO1 to PO6, CWO/IFMOD, PC (C12 only)

*5: CTLI/SDA

■ Application Circuit Example



Structure of Analog Post Filter and Sample Analog Connections

■ Package Dimensions (Unit: mm)

QFP048-P-1212A